AN ADVANCED LARGE-SIGNAL OPERATIONAL AMPLIFIER MACROMODEL FOR WATAND COMPUTER SIMULATION

BY

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ABSTRACT

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A general-purpose large-signal macromodel of an operational amplifier is presented. The model simulates the following characteristics: input impedance, voltage and current offsets, input bias current, gain versus frequency, slew rate limiting, output voltage and current limiting, and output impedance. The parameters used in the model can be taken from a typical data sheet and the user's circuit.

The model is designed to meet the requirements of flexibility, maximum speed, and minimum storage with the WATAND package. The macromodel is accurate for general purpose large- and small-signal applications. Comparisons of model performance with data obtained experimentally are presented.

The capabilities of the model are demonstrated with five examples. An inverting amplifier example shows gain versus frequency and large-signal input response. The slew rate characteristic and output voltage limiting are shown with a monostable multivibrator. A single supply non-inverting amplifier is tested. The fourth example is a triangular wave generator which consists of a comparator and an integrator. The last example is a band-pass R-active filter. The frequency response of this model is tested.

ACKNOWLEDGEMENTS

I would like to express my deep appreciation to my thesis advisor, Dr. Philip Munro, for his guidance and help in this thesis. I would also like to thank Dr. Jane Kestner in the department of psychology who carefully corrected my writing. Many thanks to my wife, May, for her support.

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CHAPTER I

INTRODUCTION

1.1 OBJECTIVE

Computer-aided design (CAD) has become an important tool for circuit analysis and design. With CAD simulation programs, engineers can simulate a circuit, change the components, alter elements' values, vary parameters, and observe the change at any point in the circuit. Circuit simulation has largely replaced "breadboarding' in circuit analysis and design.

The integrated circuit operational amplifier (op amp) is very popular and widely used in electronic circuits. When a circuit is designed containing op amps, the characteristics of op amps are frequently assumed to be ideal, i.e., gain and input impedance are infinite and output impedance is zero. In many cases, this assumption is not adequate. For example, in large-signal response, the output voltage is limited by the slew rate, the maximum change rate in the output. The present built-in op amp in WATAND [1] is a linear element which has ideal op amp characteristics. An existing user-defined op amp model for WATAND [2] also is not adequate for large-signal response. An improved model is necessary when analyzing some circuits containing op amps.

1.2 THE WATAND SOFTWARE PACKAGE

WATAND (WATerloo ANalysis and Design), developed at the Electrical Department of the University of Waterloo [1,3], is an interactive, user-oriented system for simulating linear and non-linear electronic circuits. WATAND has a large number of built-in linear and non-linear elements, such as resistors, capacitors, inductors, diodes, transistors, the linear op amp, etc. Besides these built-in elements, user-defined elements and subcircuits can be defined and used (see Refs. [1,2,4] for examples). The WATAND package uses piecewise linear (PWL) methods to represent nonlinear characteristics. This method allows a user to define the tradeoff between execution time and accuracy [5]. This package was designed to meet the requirement of maximum flexibility, minimum storage, and maximum speed. The WATAND version used in this thesis is version 1.10-00.

1.3 MACROMODEL REVIEW

Several op amp macromodels have been published. Boyle, et al. [6] use a simplification technique to describe the input characteristics by using simple ideal elements to replace numerous real elements. The other characteristics are modeled by a "build-up" technique. In this technique, a circuit is proposed to meet certain external circuit specifications without necessarily resembling the original circuitry. This macromodel models the input and output

characteristics, differential- and common-mode gain versus frequency characteristics, offset characteristics, and large-signal characteristics.

Glesner and Weisang *[7]* present a macromodel obtained by using the "build-up" technique. This model contains only linear elements and uses RC circuits to simulate the frequency related characteristics of the op amp. Besides those characteristics contained in Boyle's model, the thermal behavior is also considered in this macromodel.

Sanchez-Sinencio and Majewski *[8]* use the "build-up" technique in their macromodel. The model is developed for frequency domain applications and not for nonlinear transient operation. The large-signal response in frequency domain analysis can be simulated in this model. It has many mathematical and frequency dependent equations which can not be used directly in WATAND.

Weil and McNamee [9] use 13 diodes to model the nonlinear characteristics of op amp. The "build-up" technique is used in this model. Those op amp characteristics contained in Boyle's model can be simulated in this model.

1.4 OVERVIEW

The following chapters develop a general macromodel for an integrated circuit operational amplifier. Chapter II briefly describes the op amp's functional blocks and properties which are used in the macromodel. The step by

step development of the op amp macromodel is contained in Chapter III. Chapter IV describes the method for using #DEfine and a user written Fortran subroutine to build the op amp macromodel into WATAND. Five examples of the application of the op amp macromodel are contained in Chapter V. These examples are used to test the op amp macromodel's function and are compared to experiment.

CHAPTER II

OPERATIONAL AMPLIFIER

2.1 INTRODUCTION

For the design of the operational amplifier (op amp) macromodel, the op amp's characteristics - input impedance, input offset voltage, open-loop voltage gain, etc. - are considered, therefore these op amp characteristics are discussed in this chapter. The op amp is a direct-coupled high-gain amplifier. It amplifies the difference of the two input voltages and can be ideally characterized by the function

$$V_o = A_{ol}(V_1 - V_2), \qquad (2.1)$$

where A_{ol} is the open-loop gain of op amp and V_1 and V_2 are input voltages. A block diagram of a basic op amp is usually as shown in Fig. 2-1 [10]. The differential amplifier in the input stage transfers the differential input voltages to differential currents. These differential currents, I_{c1} and I_{c2}, are then converted to a single-ended current, I_{out}, in the current mirror block. The inferstage changes this current back into voltage, v'_{out}. The internal capacitor, C_c, is used to keep the op amp stable. The output stage contains unity-gain emitter followers. This stage amplifies the output current and provides low impedance drive to the load. The properties of the op amp are described in the following sections.

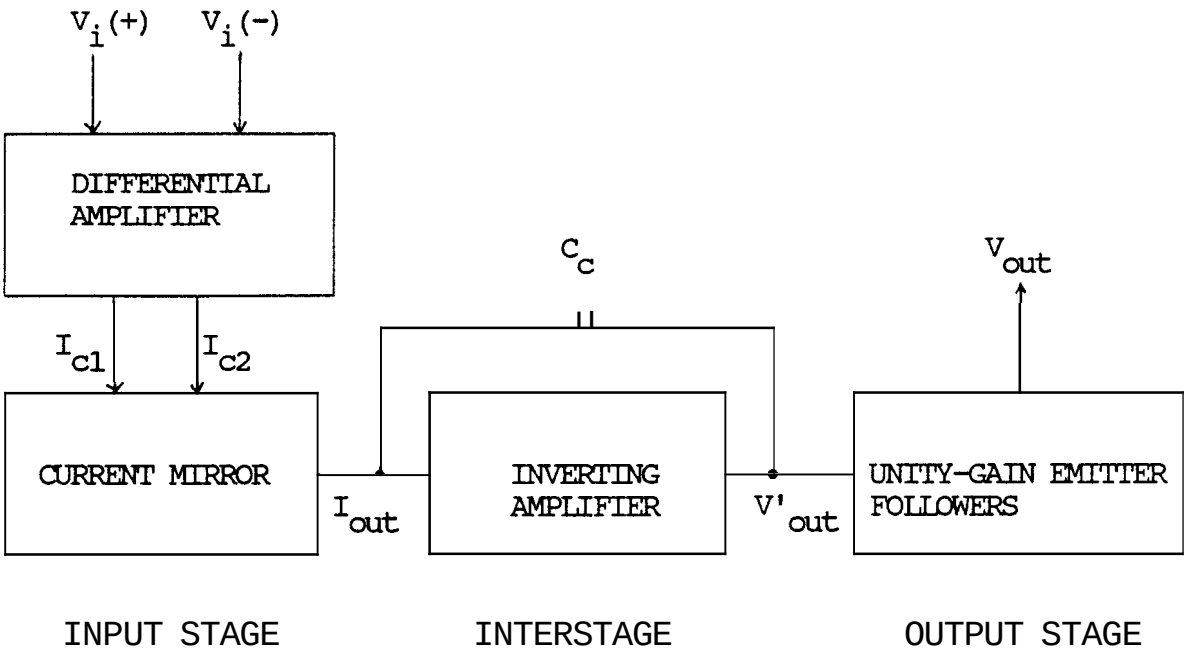


Fig. 2-1 Block Diagram of a Basic Op Amp.

2.2 INPUT STAGE

2.2.1 INPUT OFFSET VOLTAGE

For an ideal op amp with finite gain, the output voltage is an amplified replica of the difference between two input voltages. The output voltage will be zero when the input voltages are the same. Real op amps do not provide this idealized performance because of the imbalance of the internal circuit and the common-mode gain coupled with very high gain. The input offset voltage, v_{os}, is the amount of the input voltage added between two input terminals to make the output voltage zero. For the 741 op

amp, V_{os} is 6 mV maximum. With the help of an offset voltage compensating network, the output voltage can be reduced to zero.

2.2.2 INPUT BIAS CURRENT

Input bias currents, I_{b1} and I_{b2}, are the base bias currents of the bipolar input transistors or the gate leakage currents of JFETs. I_{b1} and I_{b2} are not equal because of internal circuit imbalance and non-identical input transistors. The difference between I_{b1} and I_{b2} is the input offset current, I_{os}. For the 741 op amp, a typical value of input bias current, I_b, is 500 nA at supply voltages of f15 V and I_{os} is 200 nA.

2.2.3 INPUT IMPEDANCE

The ideal op amp has an infinite input impedance, Z_i. A real op amp has a finite input impedance which can be represented as a combination of a difference-mode impedance, Z_{id}, and a common-mode input impedance, Z_{ic}. Z_{id} and Z_{ic} are both ac signal impedances, that is

$$Z_{id} = R_{id} \,/\!/\, C_{id}$$

$$Z_{ic} = R_{ic} \,/\!/\, C_{ic}$$

R_{id} is generally in the range of 100k ohms up to 100M ohms for bipolar op amps or 10^{12} ohms for FET op amps [10]. The difference-mode input capacitance, C_{id}, is typically 2 pF for both types of op amps. The value of R_{ic} is in the

range of 1M ohms to 100G ohms. The common-mode input capacitance, C_{ic}, is 3 to 5 pF for FET op amps and 2 to 3 pF for bipolar op amp. Z_{id} is increased by the use of feedback but Z_{ic} remains unaffected [11].

2.3 INTERSTAGE

2.3.1 GAIN CHARACTERISTICS

The voltage gain of the op amp is usually provided by the input stage and interstage. The differential-mode voltage gain, A_{dm}, is the ratio of the voltage change in the output to the change in the difference between the two inputs. The open-loop voltage gain is essentially identical to the differential-mode voltage gain. The open-loop gain is usually in the range 10^5 to 10^6 at low frequency [11]. The common-mode voltage gain, A_{cm}, is the ratio of the voltage change in the output to the change of the common-mode input. A_{cm} is usually very small compared to A_{dm}.

The op amp gain is frequency dependent because of the capacitive components in the op amp circuit. There are three major sources responsible for capacitive effects [12]: 1) the compensation capacitor which is used for stablization, 2) the junction capacitors in the bipolar transistors or FETs which compose the op amp, and 3) the stray capacitance of the semiconductor device's substrate. The cumulative effect of these capacitive effects causes the gain to decrease as the frequency increases. A typical Bode plot is shown in Fig. 2-2.

The frequency f_1 is the first break point frequency of the op amp and is usually small (around 10Hz). For high-gain IC op amps, the second break point frequency, f_2, is usually very large (1 to 3 MHz) compared to f_1 [11]. The unity-gain frequency, f_u, is defined as the frequency at which the gain is unity. The gain as a function of frequency can be expressed in the form [10]

$$A_{ol}(f) = \frac{A_{ol}(0)}{(1+jf/f_1)(1+jf/f_2)(1+jf/f_3)\ldots} \qquad (2.2)$$

where $f_1 < f_2 < f_3 < \ldots$

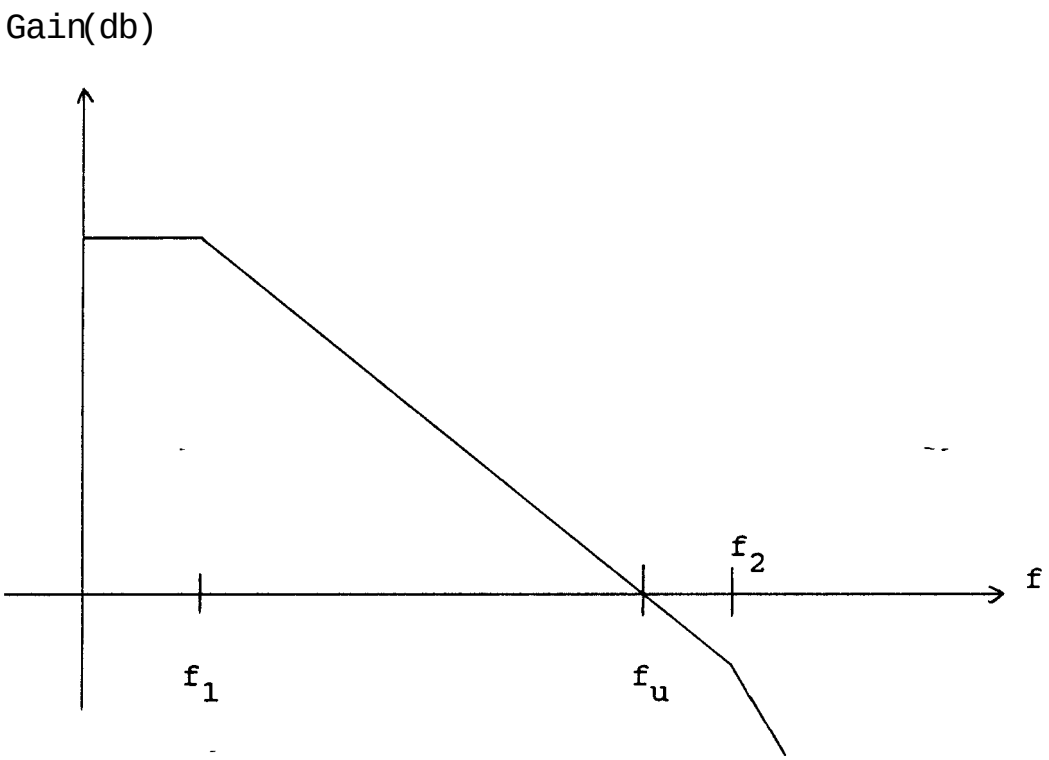


Fig. 2-2 Bode Plot for Op Amp.

2.3.2 SLEW RATE

The slew rate specification of an op amp is the maximum rate of change of output voltage with respect to time, $(dv_o/dt)_{max}$. Slew rate limitation arises because of current limiting of an op amp when a high frequency and large (quickly changing) signal is applied.

For most op amps, the positive going slew rate is slightly different from the negative going slew rate [13]. The slew rate effect is illustrated in a voltage follower with rectangular-pulse input as shown in Fig. 2-3, since these represent the worst case condition for slew rate in the op amp. For the NPN input stage, the output waveform shows a step "enhancement" on the positive going output and a "degradation" in the negative going output. For the PNP input stage, these effects are reversed as shown by $V_{op}(t)$ in Fig. 2-3.

2.3.3 COMMON-MODE REJECTION RATIO

The common-mode rejection ratio (CMRR) can be defined as the ratio of the differential voltage gain, A_d, to the common-mode voltage gain, A_{cm}, that is,

$$CMRR = A_d/A_{cm} \qquad (2.3$$

For the ideal op amp, A_{cm} would be zero and therefore CMRR ideally would be infinite. The actual op amp has a non-zero common-mode voltage gain which is generally less than 1.0 [12]. The CMRR is a function of frequency and decreases as the frequency is increased.

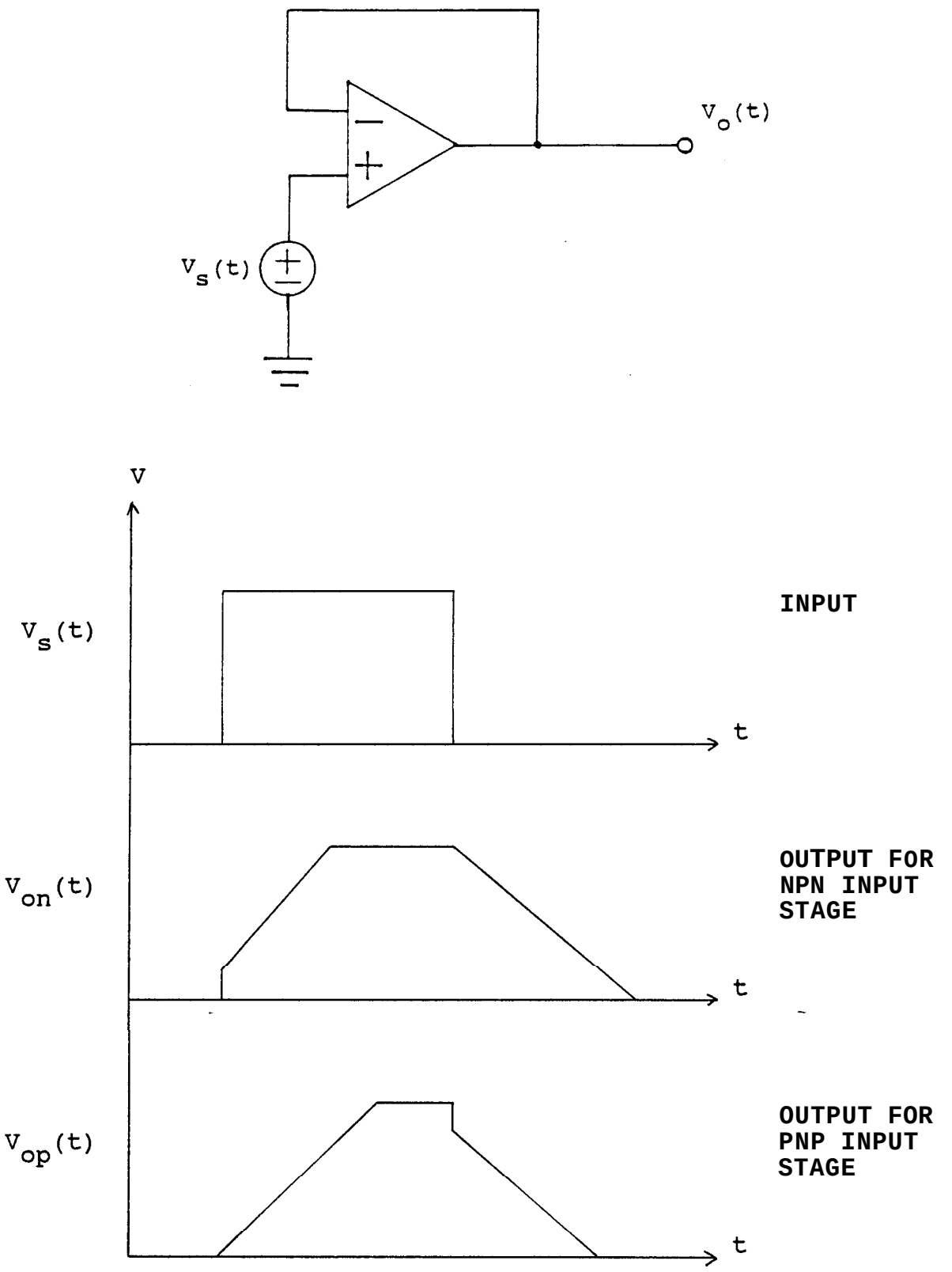


Fig. 2-3 Effect of Slew Rate on Voltage Follower Output.

2.4 OUTPUT STAGE

2.4.1 OUTPUT IMPEDANCE

For the ideal op amp, the output impedance is zero. The output resistance of the op amp is the equivalent resistance that can be measured between the output terminal and the ground. For a real op amp, R_o is generally in the range of 10 to 100 ohms. With feed back in a circuit using an op amp, R_o can be reduced to the milliohm range [11].

2.4.2 OUTPUT VOLTAGE SWING

The output voltage swing, V_{omax}, is limited by the supply voltages. For the 741 op amp, V_{omax} is guaranteed to be between +13 V and -13 V for R_l > 2K ohms and supply voltages of f15 V.

2.4.3 OUTPUT SHORT-CIRCUIT CURRENT

Output short-circuit protection is usually provided to prevent op amp damage due to momentary shorts to ground or to either of the power supply voltages. For the 741 op amp, the short-circuit current, I_{sc}, is 25 mA.

2.5 FET OPERATIONAL AMPLIFIER

The input impedance of op amps using bipolar transistors is usually in the range of several hundred kilohms to megaohms because the base-emitter junction is forward biased. For op amps using junction field-effect transistors (JFETs) in the input stage, the input terminal is the gate which is one side of the reverse-biased gate-channel

junction. The input resistance is much higher than the bipolar op amp's input impedance, with values well up into the gigaohm range. The input current of the JFET device is the gate current and is the reverse leakage current of the gate-channel junction. The current is usually around 10 pA, while the base current of bipolar transistor is in the microampere range. For op amps using metal-oxide-silicon FET (MOSFETs), the gate terminal is separated by a thin insulating layer of silicon dioxide. As a result, extremely high values of input resistance in the teraohm (10^{12} ohm) range can be obtained. The gate current is also extremely small, often below 1 pA.

The slew rate of an op amp is limited by the quiescent current, I_Q [11]. The input resistance and input bias current of the bipolar op amp are both directly dependent on the quiescent current I_Q. Thus a high slew rate is difficult to obtain. For FET-input op amps the gate current is not dependent on the quiescent current. So, a relatively large current I_Q can be used in the design, that is a large slew rate (50 to 75 V/μs) and a high unity-gain frequency (~20MHz) can be obtained.

The advantages of FET op amps over bipolar op amps are higher input resistance, lower input bias and offset current, higher slew rate, and higher unity-gain frequency. The disadvantage is the lower voltage gain because FETs often have 30 to 100 times smaller transfer conductance than bipolar transistors [11,13].

CHAPTER III

DEVELOPING THE OP AMP MACROMODEL

3.1 INTRODUCTION

Circuit simulation has proven to be very useful in the analysis or design of electronic systems. Most electronic circuits contain many integrated circuits (ICs) today. If these ICs are modeled at the device level, the circuit simulation program will require large memory and execution time. The solution to this problem is using macromodels which model the terminal behavior to the desired degree of accuracy with a comparatively small number of circuit elements. The 741 op amp, if modeled at the device level, would consist of 96 nonlinear elements and 131 linear elements in WATAND. Using the macromodel presented by Glesner and Weisang [7], the op amp model would only contain eight nonlinear and fourteen linear elements. This 90% reduction in model size using the macromodel instead of the device level model would result in significantly less simulation time and less memory space.

Two macromodeling procedures have been introduced [6]. One is simplifying the circuitry by using simpler circuits with ideal elements. The other, the "build-up" procedure, simulates the terminal behavior by an equivalent circuit without necessarily resembling the original

circuitry. The macromodel presented in this chapter uses the **"build-up"** technique and is based on the basic diagram shown in Fig. 3-1. The following sections discuss the development of the op amp macromodel.

3.2 INPUT STAGE

The input stage of the op amp macromodel simulates the functioning of the real op amp input stage. It models the input offset voltage, input bias current, input offset current, differential-mode impedence, common-mode impedence, differential voltage gain, and common-mode voltage gain. The differential gain will be modeled in the interstage for simplification.

Boyle's model [6] shown in Fig. 3-2 uses a simplification technique to model the input stage by using a differential amplifier and ideal elements. Because in WATAND each transistor model (Ebers-Moll model) contains four current sources and six passive elements, the circuit-

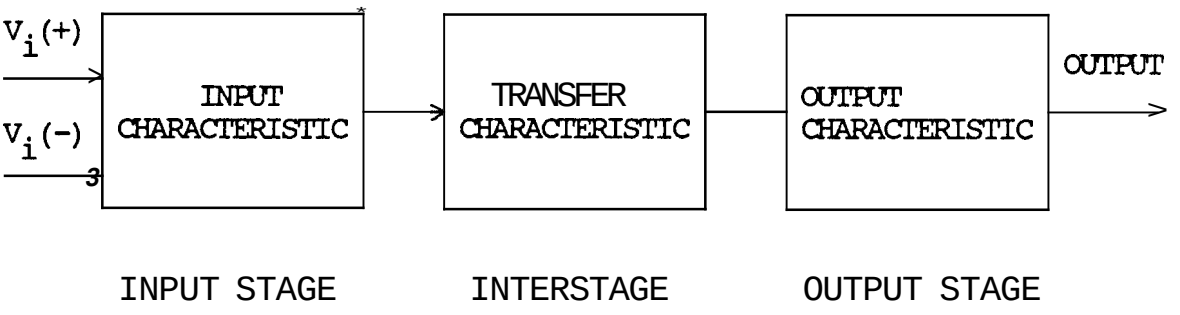


Fig. 3-1 Function Blocks of a Basic Op Amp.

of this input stage model would contain nine current sources, nineteen passive elements, and ten nodes. Since this model is big, it would take relatively large memory and CPU time.

Other macromodels [7,8,14] use the "build-up" technique. Glesner's model [7] shown in Fig. 3-3 uses one voltage source to represent the input offset voltage and three current sources to represent input offset current and bias currents. It contains input differential mode impedance and common-mode resistance. It also simulates the

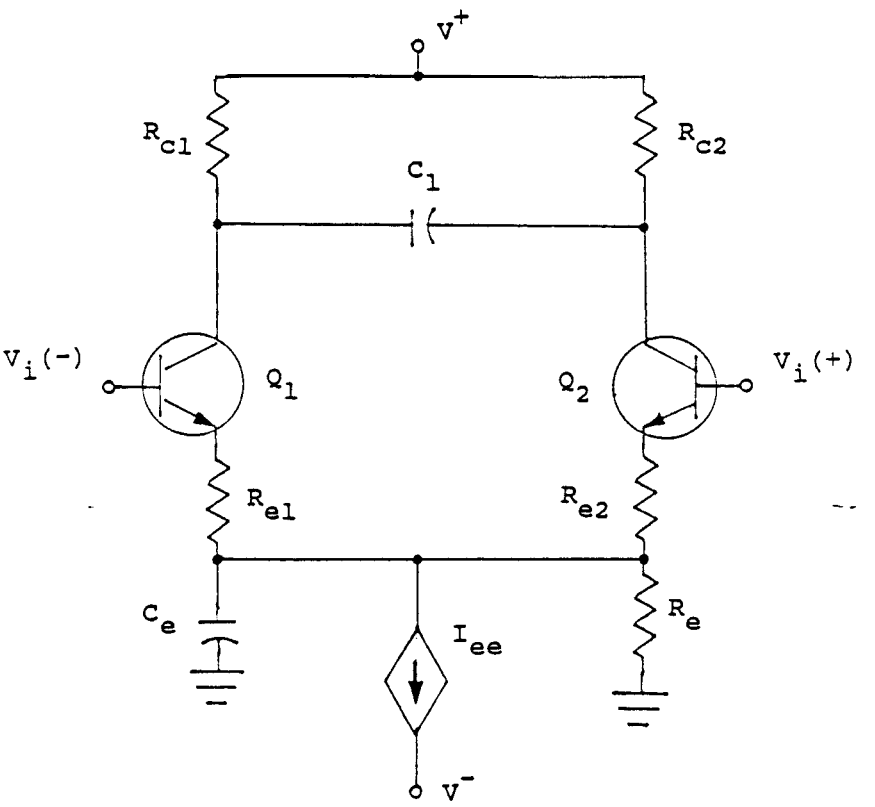


Fig. 3-2 Boyle's Op Amp Input Stage Model.

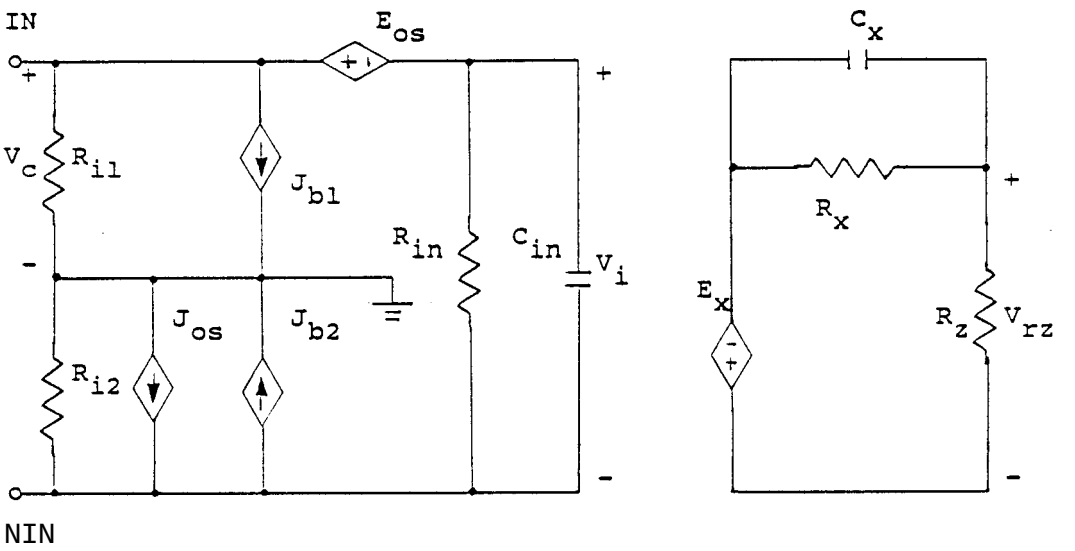


Fig. 3-3 Glesner's **Op Amp Input Stage Model.**

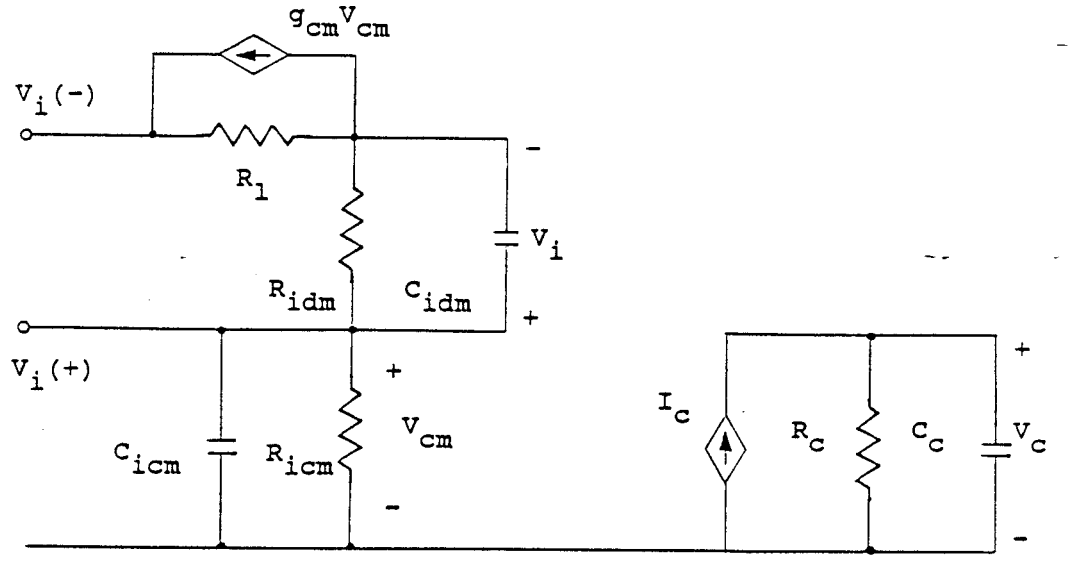


Fig. 3-4 Sanchez-Sinencio's **Op Amp Input Stage Model.**

frequency dependent common-mode rejection behavior by using one dependent voltage source, two resistors and a capacitor. The model needs five dependent sources, seven passive elements and six nodes.

The model of Sanchiez-Sinencio and Majewski [8] shown in Fig. 3-4 simulates the differential and common-mode input impedance. An extra stage (I_c, R_c, and C_c) must be used to provide the frequency dependent common-mode rejection ratio, CMRR(ω), when used in WATAND. The model would need two dependent sources, seven passive elements and five nodes.

The model proposed by Weil and McNamee [9] shown in Fig. 3-5 uses two diodes and a current source to model the impedance, input offset current, and nonlinear input bias current. It needs four dependent sources, six passive elements, and seven nodes when modeled in WATAND.

The proposed model shown in Fig. 3-6 is based on Glesner's model but with some modification. R_i and C_i make up the input differential impedance. R_{ic} is the input common-mode resistance. V_{os} is the input offset voltage. The sign for V_{os} may be positive or negative. I_{b1} and I_{b2} are input bias currents in terms of average bias current, I_b, and offset current, I_{os}, and

$$I_{b1} = I_b + I_{os}$$
$$I_{b2} = I_b - I_{os} \qquad (3.1)$$

I_{os} may be positive or negative. The signs of I_{b1} and I_{b2}

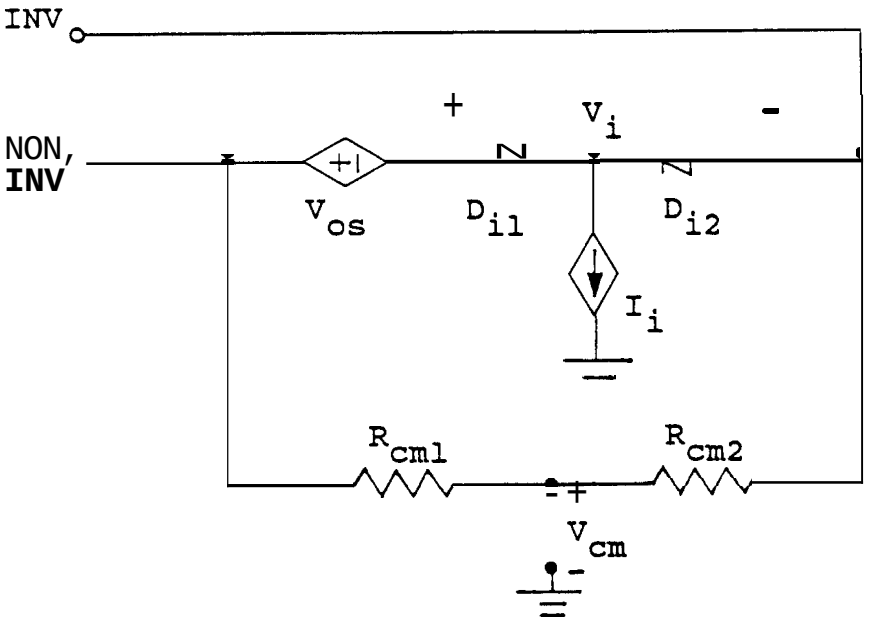


Fig. 3-5 Weil and McNamee's Op Amp Input Stage Model.

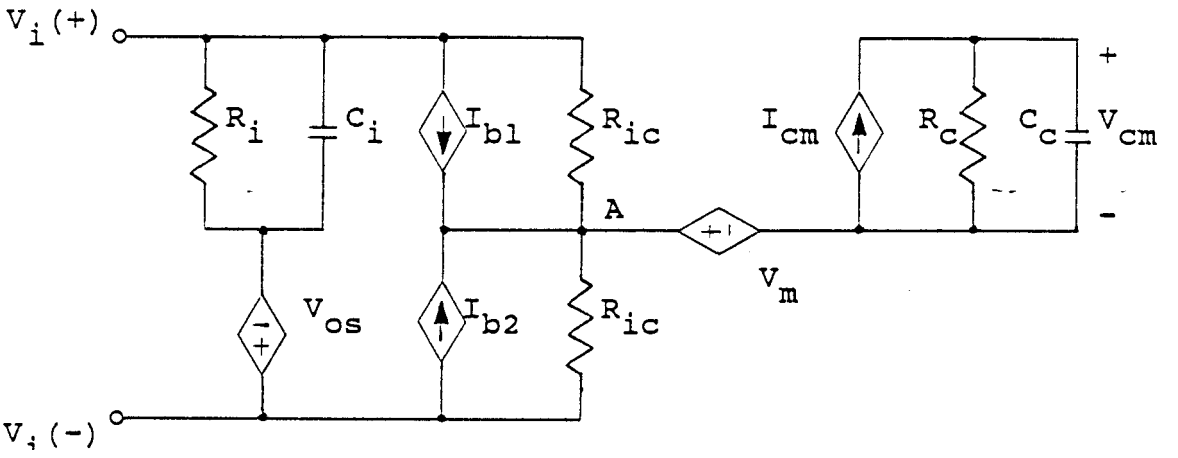


Fig. 3-6 Proposed Op Amp Input Stage Model.

shown in Fig. 3-6 are positive for NPN-input or FET/bipolar op amps where the bias currents enter the op amp. For PNP-input op amps, these signs are reversed. Because the values of V_{os}, I_{os}, and I_b are random, one may want to use the Monte-Carlo analysis (see Ref. [15]) to model the random effect of these parameters' values.

The voltage source V_m is used for the voltage level between the input stage and the output stage. For a balanced supply voltage situation, the middle point (common point), V_A, should be zero voltage (ground), but for an unbalance supply voltage case, the middle point is not at zero voltage. The voltage level is

$$V_m = \frac{(V^+ + V^-)}{2} \tag{3.2}$$

I_{cm}, R_C and C_C (see Fig. 3-6) are used for the frequency dependent CMRR.

$$I_{cm} = \frac{CMRR(0)}{R_C}$$

$$\omega_{cmrr} = \frac{1}{R_C C_C}$$

$$V_{cm} = \frac{I_{cm} R_C}{1+j\omega R_C C_C} = \frac{CMRR(0)}{1+jf/f_{cmrr}} = CMRR(\omega) \tag{3.3}$$

where f_{cmrr} is the breakpoint frequency of CMRR obtained from the manufacturer's specifications.

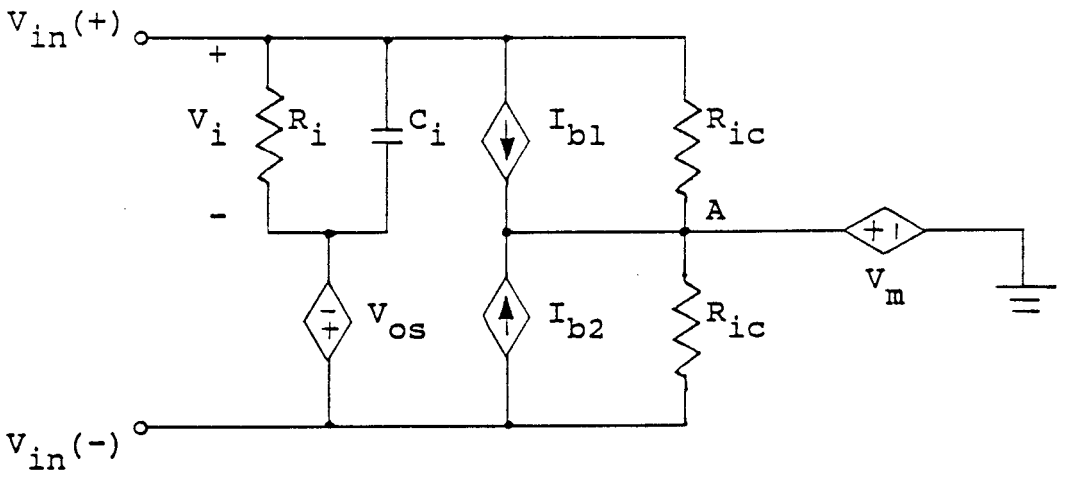


Fig. 3-7 The Simpler Op Amp Input Stage Model.

The model has five dependent sources and six passive elements. Since the **CMRR** is usually very large, the common-mode gain is very small compared to differential gain. The **CMRR** stage is, therefore, omitted for simplicity. The final simplified input stage model is shown in Fig. 3-7. Two voltage sources, two current sources, four passive elements, and five nodes are used in this model.

3.3 INTERSTAGE

The interstage models the gain which is affected by frequency and slew rate. Most interstage models use the **"build-up"** technique [6-9]. The models use the frequency domain method (using RC circuits) to simulate the pole function. These models provide two-pole (-breakpoint)

characteristics. Fig. 3-8 shows Vlach's model [14] for the interstage. I_2, R_2 and C_2 provide the first pole and slew rate characteristics. The slew rate is modeled by limiting I_2.

$$I_m = V_{omax}/R_o$$

$$I_2 < |I_m|$$

$$C_2 = I_m/SR$$

$$R_2 = 1/\omega_1 C_2$$

where I_m = the maximum output current swing

V_{omax} = the maximum output voltage swing

R_o = output resistance

SR = slew rate

ω_1 = the first breakpoint frequency

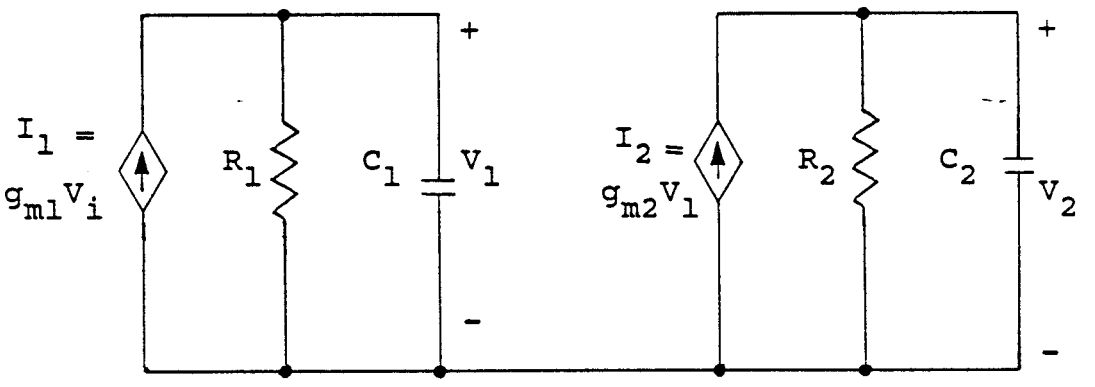


Fig. 3-8 Vlach's Interstage Model [14].

R_1, C_1, and I_1 form the second pole characteristic. R_1 is chosen arbitrarily.

$$R_1 = 100$$

$$C_1 = 1/\omega_2 R_1$$

where ω_2 = the second break point frequency.

Another method for modeling the interstage is to use the time domain equation to simulate the two-pole function.

$$\text{Gain} = \frac{V_2(s)}{V_i(s)} = \frac{A_0}{(1+s/\omega_1)(1+s/\omega_2)}$$

$$= \frac{A_0}{1 + \frac{(\omega_1+\omega_2)}{\omega_1\omega_2}s + \frac{s^2}{\omega_1\omega_2}} \qquad (3.4)$$

$$V_2(s) + \frac{\omega_1+\omega_2}{\omega_1\omega_2} sV_2(s) + \frac{1}{\omega_1\omega_2} s^2V_2(s) = A_0V_i(s)$$

Taking the inverse Laplace transform [16], the equation becomes

$$V_2(t) + \frac{\omega_1+\omega_2}{\omega_1\omega_2}\frac{dV_2(t)}{dt} + \frac{1}{\omega_1\omega_2}\frac{d^2V_2(t)}{dt^2} = A_0V_{i(t)}$$

$$V_2(t) = A_0V_i(t) - \frac{\omega_1+\omega_2}{1\omega_2}\frac{dV_2(t)}{dt} - \frac{1}{\omega_1\omega_2}\frac{d^2V_2(t)}{dt^2} \qquad (3.5)$$

In WATAND a derivative such as dV_2/dt can be represented with a charge source, Q, or a flux source, F. The Q source has a current value equal to dQ/dt, and the F source has voltage value equal to dF/dt. Since the F source is accompanied with an auxiliary variable in WATAND, employing it would make the circuit matrix larger than the model using the Q source. Therefore, Eq. 3.5 is modeled by using the charge source as shown in Fig. 3-9.

$$Q_a = V_2$$

$$Q_b = \frac{1}{\omega_1 \omega_2} V_1$$

$$I_q = A_0 V_i - \frac{\omega_1 + \omega_2}{\omega_1 \omega_2} V_1$$

Therefore as seen from Fig. 3-9,

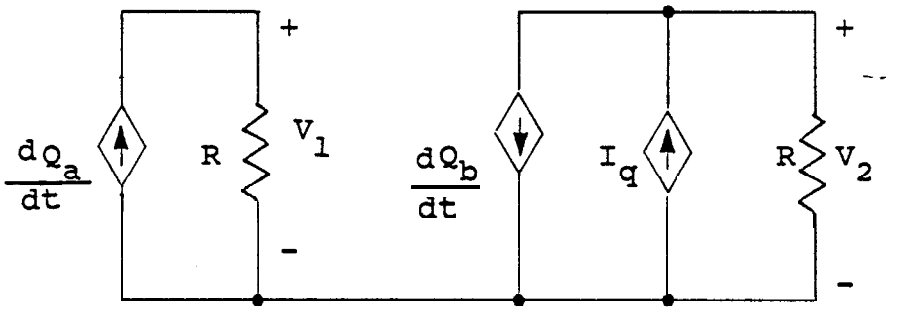


Fig. 3-9 The Q Source Method Interstage Model.

$$R_1 = R_2 = 1$$

$$V_1 = \frac{dQ_a}{dt} = \frac{dV_2}{dt}$$

$$V_2 = I_q - \frac{dQ_b}{dt}$$

$$= A_0 V_i - \frac{\omega_1+\omega_2}{\omega_1\omega_2} V_1 - \frac{1}{\omega_1\omega_2} \frac{dV_1}{dt}$$

$$= A_0 V_i - \frac{\omega_1+\omega_2}{\omega_1\omega_2} \frac{dV_2}{dt} - \frac{1}{\omega_1\omega_2} \frac{d^2V_2}{dt^2}$$

This equation is exactly the same as Eq. 3.5.

The slew rate characteristic is modeled by limiting the current I_q. Eq. 3.6 is given in Ref. [13]

$$SR = \left.\frac{dV_o}{dt}\right|_{max} = \omega_u V_m \tag{3.6}$$

where ω_u = the unity-gain frequency

SR = the slew rate

The maximum input to the interstage. V_m, is

$$V_m = \frac{SR}{\omega_u} = \frac{SR}{\omega_1 A_0}$$

Then, the input voltage. V_i, is limited as follow:

if $V_i > V_m$, $V_i = V_m$

and if $V_i < -V_m$, $V_i = -V_m$ (3.7)

3.4 OUTPUT STAGE

The output stage simulates the characteristics of output impedance, output voltage limit and short-circuit current limit. Boyle [6] and Weil [9] use two diodes to limit the output voltage. Vlach [14] and Sanchez-Sinencio [8] use a nonlinear resistor to limit the voltage. These nonlinear elements make the model more complicated to simulate on the computer. A simpler method for WATAND is to use a voltage source having a voltage limit function.

$$\text{If } V_o > V_{omh}, \qquad V_o = V_{omh}$$
$$\text{If } V_o < V_{oml}, \qquad V_o = V_{oml}$$

where V_o = the output voltage of the op amp
V_{omh} = the maximum output voltage
V_{oml} = the minimum output voltage

The short-circuit current can be limited by using two diodes [6,9], or by using a current source [7]. The latter method will be used for the proposed model because it is simpler for computer simulation. Fig. 3-10 is the output stage for the proposed model. The equations are

$$I_o' = \frac{V_r}{R_o}$$

$$I_o = I_o' - I_1$$

$$I_1 = 0 \qquad \text{if } -I_{sc} < I_o' < I_{sc}$$

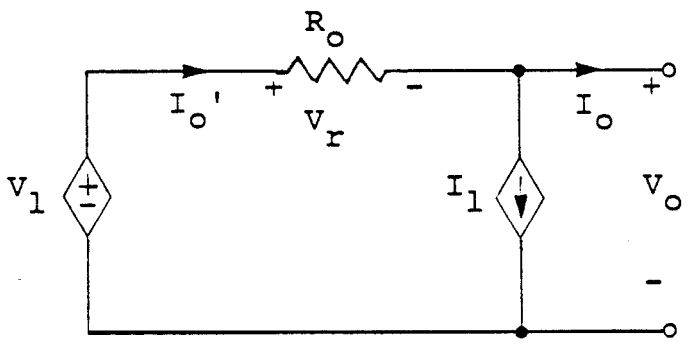


Fig. 3-10 The Output Stage Model.

$$I_1 = I_o' + I_{sc} \quad \text{if } I_o' < -I_{sc}$$

$$I_1 = I_o' - I_{sc} \quad \text{if } I_o' > I_{sc}$$

where R_o = the output resistance

V_r = the voltage across R_o

I_o = the output current of the op amp model

I_1 = the current limiter

I_{sc} = the short-circuit current

3.5 THE COMPLETE OP AMP MACROMODEL

The complete model of the op amp shown in Fig. 3-11 is the combination of the separated models in Fig. 3-7 to 3-10. This macromodel uses RC circuits to simulate the pole frequencies. Another macromodel shown in Fig. 3-12 simulates the poles function with Q sources which are part of the #DEFINE element in the WATAND macromodel. The difference between these two models is the interstage. The

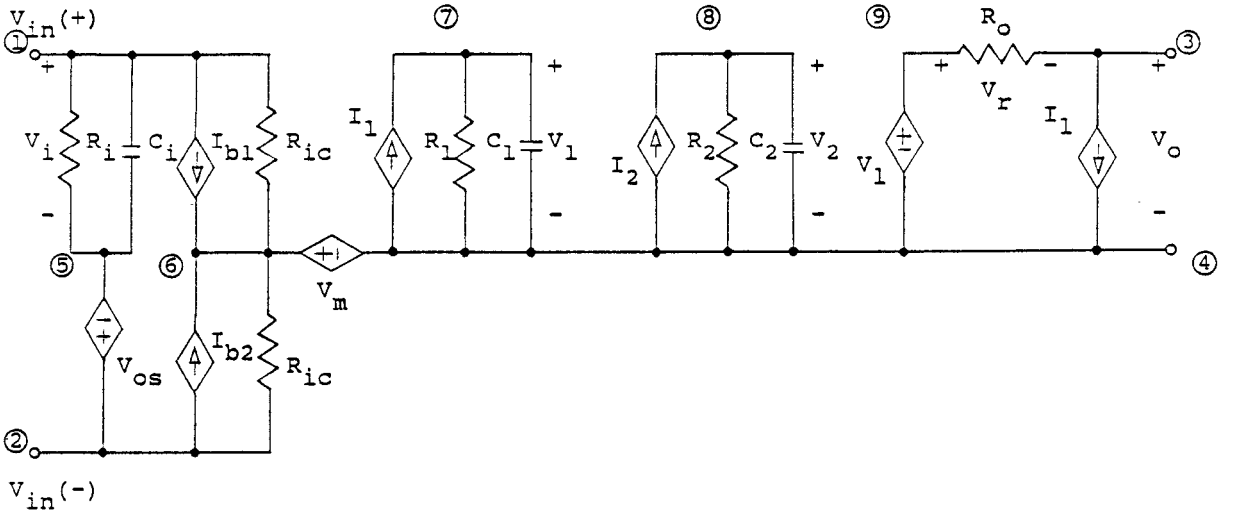


Fig. 3-11 The RC Circuit Method Op Amp Macromodel.

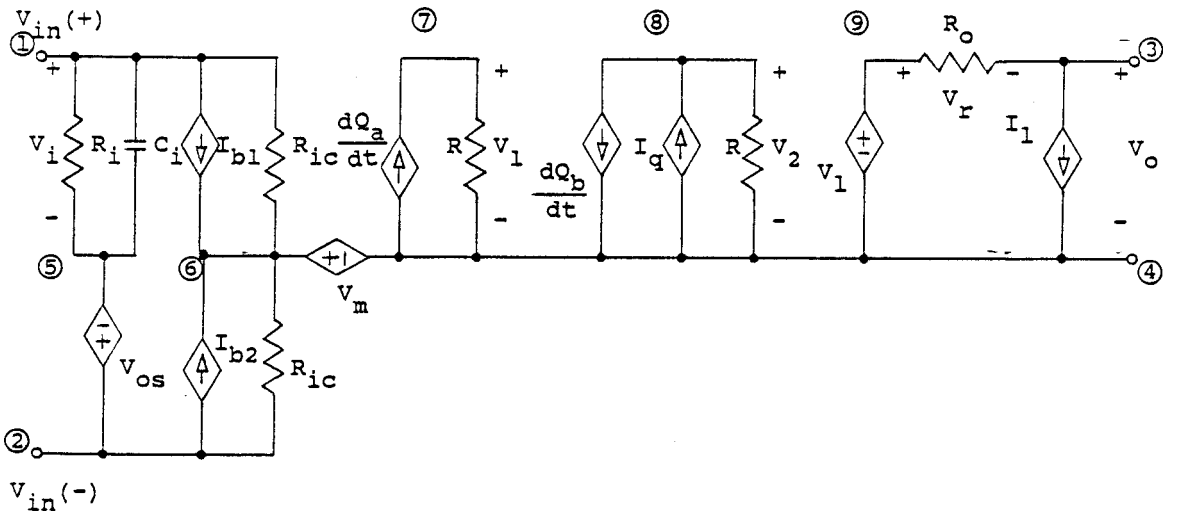


Fig 3-12 The Q Source Method Op Amp Macromodel.

function for these two macromodels is the same but the performance is somewhat different.

The macromodels shown in Fig. 3-11 and 3-12 work well in the small-signal case. However, in a large-signal case, because of the large gain in the interstage, that stage's output will be very large compared to the power supply voltages. Due to the large charge supplied to C_1 (see Fig. 3-11), the output response can not follow the input voltage at high frequency. A noninverting amplifier using a test macromodel shown in Fig. 3-13 is used to illustrate with WATAND.

Because the slew rate limits the change of I_2, V_2 becomes triangular instead of sinusoidal as seen in Fig. 3-14. When the input voltage of this amplifier goes from positive to negative, V_2 is very high and C_2 takes additional time to discharge. The output voltage of this amplifier becomes rectangular instead of being a square wave. Therefore, the model must be modified to eliminate the discharge delay. A voltage reduction in V_2 during large-signal response must be added. Boyle's model [6] provides this voltage limit by using two diodes and a dependent variable.

In this work, V_2 is limited by modifying the function I_2 (dependent source). If V_2 exceeds the maximum output voltage, I_2 is reduced by an amount I_d. The equations for I_d are

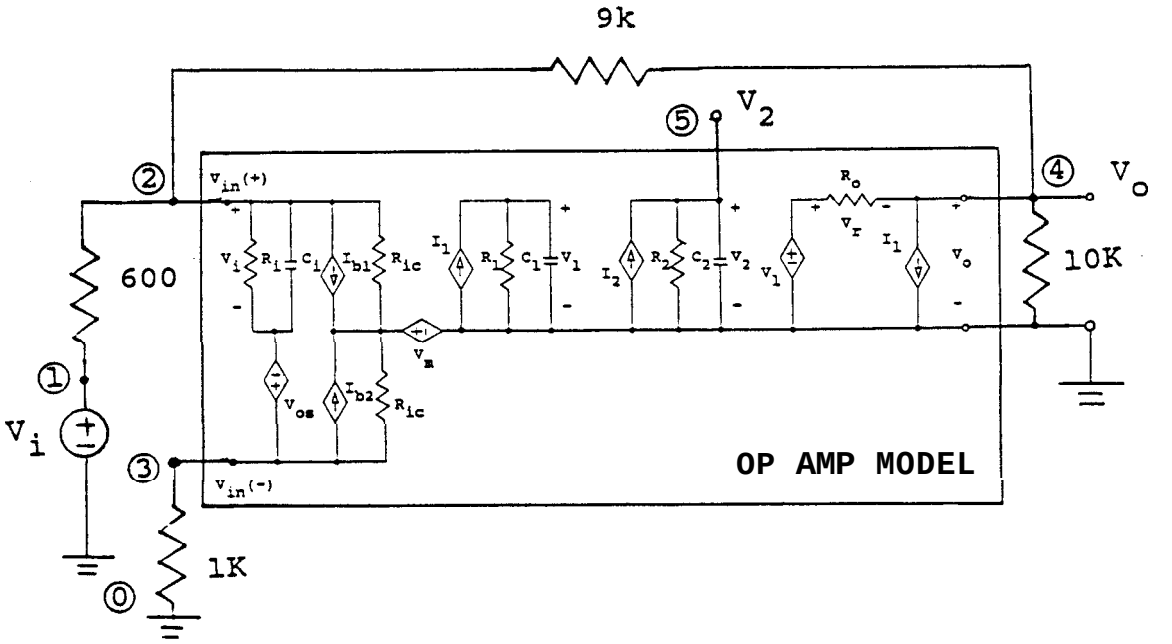


Fig. 3-13 A Noninverting Amplifier.

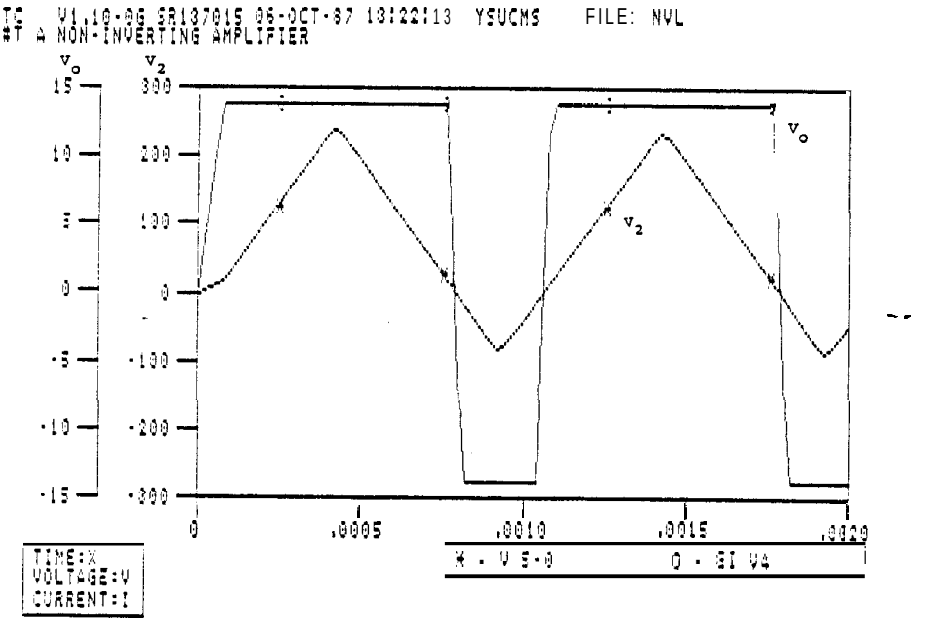


Fig. 3-14 The Output Voltage V_2 of the Interstage for Large V_i.

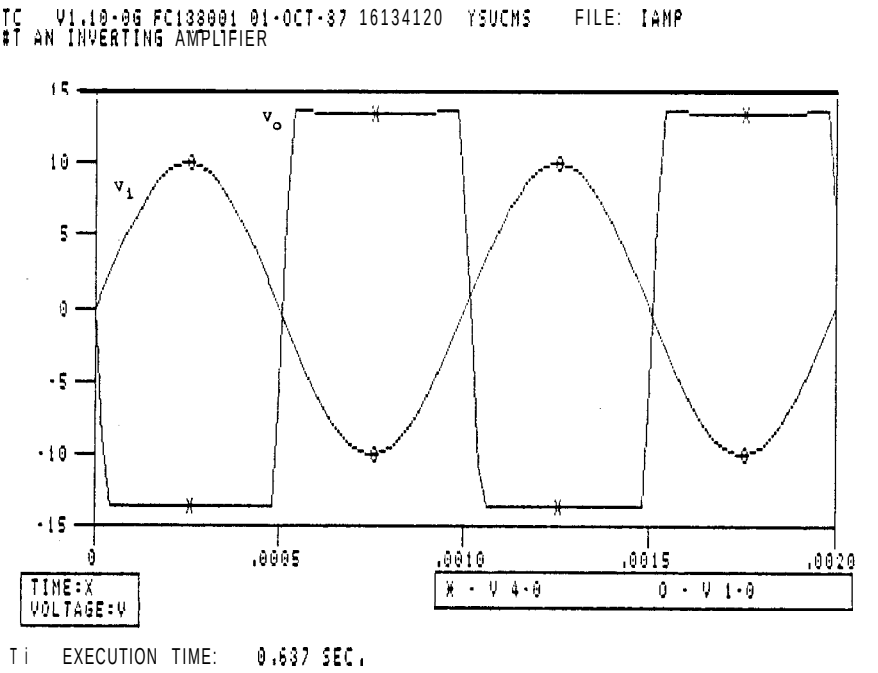


Fig. 3-15 The Output Voltage of the Modified Model.

$$I_d = 0 \qquad \text{if } V_{omh} > V_2 > V_{oml}$$

$$I_d = \exp(V_2 - V_{omh}) - 1 \qquad \text{if } V_2 > V_{omh}$$

$$I_d = -\exp(V_{oml} - V_2) - 1 \qquad \text{if } V_2 < V_{oml}$$

Under this limit, V_2 won't go too high above the maximum output voltage. Fig. 3-15 shows the output of the non-inverting amplifier using the modified model.

The Q source model shown in Fig. 3-12 can be modified by just changing the dependent current source I_q, that is

$$I_q = A_0 V_i - \frac{\omega_1 + \omega_2}{\omega_1 \omega_2} \frac{dV_2}{dt} - [\exp(V_2 - V_{omh}) - 1]$$

$$\text{for } V_2 > V_{omh} \qquad (3.8a)$$

$$I_q = A_0 V_i - \frac{\omega_1+\omega_2}{\omega_1\omega_2}\frac{dV_2}{dt} - [\exp(V_{oml}-V_2)-1]$$

for $V_2 < V_{oml}$ (3.8b)

The exponential expressions in Eqs. 3.8a and 3.8b are added to limit the voltage in the interstage.

These op amp models provide for input and output characteristics, differential gain versus frequency characteristics, offset characteristics, and large signal characteristics, such as slew rate, output voltage swing, and short-circuit current limiting. Both macromodels are capable of working in an unbalanced power supply situation. Chapter 4 deals with the implementation of these two macromodels in WATAND.

CHAPTER IV

THE WATAND OP AMP MACROMODEL

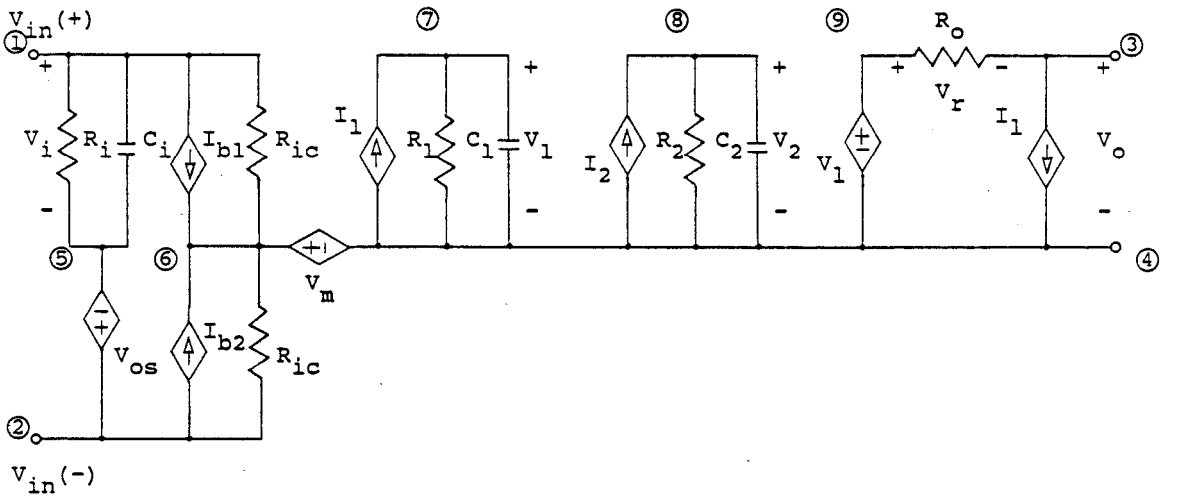
4.1 OVERVIEW

To build a model in WATAND, one can use the #DEFINE control word to describe the internal circuit and parameters of the model. The #DEFINE model may contain a) any WATAND linear elements except independent sources, switches and mutual inductances, and b) any of four nonlinear elements: current source, voltage source, charge source (I=dQ/dt) and flux source (V=dF/dt) [4]. A user written Fortran subroutine is used to evaluate the values of the nonlinear characteristics.

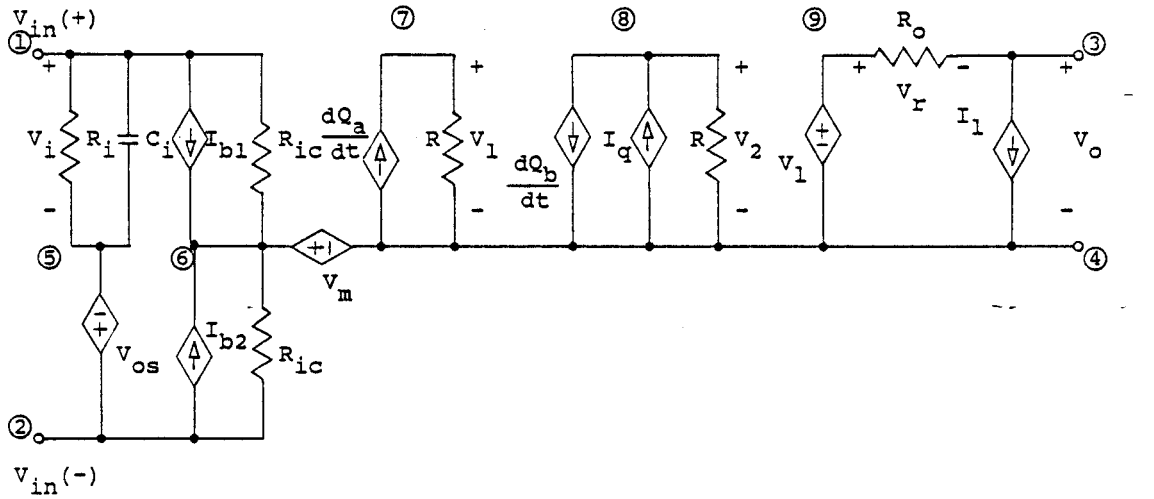
The #DEFINE section of this op amp macromodel is stored in a WBLOCK file which is discussed in section 4.2. The user written Fortran subroutines are described in section 4.3.

4.2 WBLOCK FILE

For convenience, the macromodels developed in Chapter 3 are redrawn in Fig. 4-1. The WBLOCK file of the op amp macromodel using the RC circuit method is shown in Table 4-1 (see Refs. [4,17] for the detail of WBLOCK Macros). The line numbers to the extreme left are not part of the file. The default parameter values are for the Fairchild 741 op amp. The OA in line 18 is the defined element's name.



a) Using the RC Circuit Method.



b) Using the Q Source Method.

Fig. 4-1 Op Amp Macromodels.

Table 4-1 RC **Circuit Method** of Op **Amp** WBLOCK **File.**

OA WBLOCK:

```
01 #*****************************************************************
02 #*
03 #*   OPERATIONAL AMPLIFIER MODEL USING RC CIRCUIT METHOD
04 #*        WITH 741 DEFAULTS AND ZERO-OFFSET VALUES.
05 #*
06 #*   IN THE #MODEL SECTION, ENTER
07 #*
08 #*        OA.MNAME  < OA PARAMETERS >
09 #*
10 #*   IN THE #DATA SECTION, ENTER
11 #*
12 #*        OA.MNAME.NAME  N1  N2  N3  N4
13 #*                      (VI+ VI- VO  GND)
14 #*
15 #*   CREATED 25-OCT-87      B.R. HSU    EE DEPT. YSU
16 #*****************************************************************
17 &MODEL
18 #DE OA
19 MODEL OA 13
20 *      VSUP 15 -15 A0 2D5 RI 2D6 CI 1.4P RO 75 SR 6.7D5 5D5
21 *      FB 5 3D6 VOS 0 IOS 0 IB 80N RIC 2D9 ISC 25M VOLIM -1.5 2.5
22 *      AUTOSP 1
23 *      SPVI -15 -14 -80M -1M 1M 80M 14 15
24 *      SPV1 -15 -14 -80M -1M 1M 80M 14 15
25 *      SPV2 -20 -15 -14 -7 0 7 14 15 20
26 *      SPVR -20 -5 -1.975 -1.875 1.875 1.975 5 20
27 DATA 4  1 5  7 4  8 4  9 3
28 FUNCTIONS
29 V 2 5
30 J 1 6
31 J 2 6
32 V 6 4
33 J 4 7
34 J 4 8
35 V 9 4
36 J 3 4
37 ELEMENTS
38 R 1 5  RI
39 C 1 5  CI
40 R 1 6  RIC
41 R 2 6  RIC
42 R 9 3  RO
43 C 7 4  1 M
44 R 7 4  2 M
45 C 8 4  3 M
46 R 8 4  4 M
47 #M
48 OA.&MNAME &PARAM
```

The OA in line 19 is the Fortran subroutine's name. The number 13 after OA is the number of extra storage locations reserved for use by the subroutine. Lines 20 to 22 contain parameters and their default values. Lines 23 to 26 contain sample-point parameter names and their default values. The number 4 after DATA in line 27 indicates that the first four nodes in the model will be connected to the external circuit. The numbers following DATA 4 are the node pairs for the independent variables (V15, V74, V84, and V93). Lines 28 to 36 make up the FUNCTIONS section. The first two numbers following each V and J are the nodes of the dependent source. The first four functions, V25, J16, J26, and V64, are constant sources which depend only on the constant parameters. The linear elements in the op amp macromodel are in the ELEMENTS section in lines 37 to 46. Values are obtained from parameter values RI, CI, etc., or from the extra storage locations for the last four elements.

Table 4-2 is the WBLOCK file of the op amp macromodel using the Q source method. It is similar to Table 4-1 except that it uses charge sources to simulate the pole frequencies instead of using RC circuits.

The parameter values of either macromodel can be taken from manufacturers' data sheets and from the user's circuit. The description of these parameters is given in Table 4-3. The default parameter values are for 741 op amp.

One can use these general WBLOCK files to build other op amp models. A WBLOCK file for the LF355, a JFET/bipolar

Table 4–2 Q Source Method of Op Amp WBLOCK File.

OA2 WBLOCK:

```
#*********************************************************************
#*
#*   OPERATIONAL AMPLIFIER MODEL USING Q SOURCE METHOD
#*       WITH 741 DEFAULTS AND ZERO-OFFSET VALUES.
#*
#*   IN THE #MODEL SECTION, ENTER
#*
#*        OA2.MNAME  < OA2 PARAMETERS >
#*
#*   IN THE #DATA SECTION, ENTER
#*
#*        OA2.MNAME.NAME  N1  N2  N3  N4
#*                       (VI+ VI- VO  GND)
#*
#*   CREATED 25-OCT-87  B.R. HSU   EE DEPT. YSU
#*********************************************************************
&MODEL
#DE OA2
MODEL OA2 8
*     VSUP 15 -15 A0 2D5 RI 2D6 CI 1.4P RO 75 SR 6.7D5 5D5
*     FB 5 3D6 VOS 0 IOS 0 IB 80N RIC 2D9 ISC 25M VOLIM -1.5 2.5
*     AUTOSP 1
*     SPVI -30 -15 -10 -1 -8D-2 -7.9D-2 .10663 .10763 1 10 15 30
*     SPV1 -1D7 -1D5 -1D3 1D3 1D5 1D7
*     SPV2 -30 -15 -14.1 -14 -10 -1 1 10 14 14.1 15 30
*     SPVR -10 -1.975 -1.875 1.875 1.975 10
DATA4  1 5  7 4  8 4  9 3
FUNCTIONS
v 2 5
J 1 6
J 2 6
V 6 4
Q 4 7
Q 8 4
J 4 8
v 9 4
J 3 4
ELEMENTS
R 1 5  RI
C 1 5  CI
R 1 6  RIC
R 2 6  RIC
R 9 3  RO
R 8 4  8 M
R 7 4  8 M
#M
OA2.&MNAME &PARAM
```

Table 4-3 Macromodel Parameters.

PARAMETER NAME	DEFAULT VALUES	UNITS	DESCRIPTION
VSUP			Op Amp Supply Voltages
VSUP.1	15	V	Positive supply voltage
VSUP.2	-15	V	Negative supply voltage
A0	500k		Low frequency open-loop gain
RI	2M	Ω	Input resistance
CI	1.4p	F	Input capacitance
RO	75	Ω	Output resistance
SR			Slew rate
SR.1	0.67M	V/s	Positive going slew rate
SR.2	0.5M	V/s	Negative going slew rate
FB			Break-point frequency
FB.1	5	Hz	First break-point frequency
FB.2	3M	Hz	Second break-point frequency
VOS	2m	V	Input offset voltage
IOS	20n	A	Input offset current
IB	80n	A	Input bias currrnt
RIC	2G	Ω	Common-mode input resistance
ISC	25m	A	Output short circuit current
VOLIM			The difference between maximum output voltages and supply voltages
VOLIM.1	-1.5	V	Maximum output minus VSUP.l
VOLIM.2	2.5	V	Minimum output minus VSUP.2
AUTOSP	1		Designates automatic sample-point selection (=1), otherwise, user-specified sample-points are used

Table 4-4 LF355 WBLOCK File.

LF355 WBLOCK:

```
#*****************************************************************************
**
#*    LF355 OP AMP MODEL
#*          USING THE OA MARCO WITH LF355 DEFAULTS
#*
#*    IN THE #MODEL SECTION, ENTER
#*
#*          LF355.MNAME    <LF355 PARAMETERS>
#*
#*    IN THE #DATA SECTION, ENTER
#*
#*          LF355.MNAME.NAME  N1  N2  N3  N4
#*                           (VI+ VI- VO  GND)
#*
#*    CREATED 25-OCT-87       B.R. HSU    EEDEPT.  YSU
#*****************************************************************************
&MODEL
&PARAM  VSUP A0 RI CI RO SR FB VOS IOS IB RIC ISC VOLIM AUTOSP
*       SPVI SPV1 SPV2 SPVR
&DEFAULT VSUP 15 -15 A0 2D5 RI 1D12 CI 3P RO 120 SR 5D6 9D6 FB 20 1.5D7
*        VOS 3M IOS 3P IB 30P RIC 1D12 ISC 25M VOLIM -2 2 AUTOSP 1
*        SPVI  -30 -15 -10 -1 -.l -.01 .01 .1 1 10 15 30
*        SPV1  -1D8 -1D6 -1D4 -1D2 1D2 1D4 1D6 1D8
*        SPV2  -50 -15 -14 -10 -1 1 10 14 15 50
*        SPVR  -50 -15 -14 -10 -1 1 10 14 15 50
#M
OA.&MNAME VSUP &VSUP A0 &A0 RI &RI CI &CI RO &RO SR &SR FB &FB VOS &VOS
*         IOS &IOS IB &IB RIC &RIC ISC &ISC VOLIM &VOLIM AUTOSP &AUTOSP
*         SPVI &SPVI SPV1 &SPV1 SPV2 &SPV2 SPVR &SPVR
&DATA
#D
OA.&MNAME.&NAME &PARAM
```

op amp, is shown in Table 4-4 as an example. The WBLOCK file uses the LF355 parameter values and calls the OA model (the RC circuit model).

4.3 THE FORTRAN SUBROUTINES

The user written Fortran subroutines for the RC circuit and Q source models are shown in Tables 4-5 and 4-6, resp. In this section the RC circuit subroutine is described. The Q source subroutine is very similar.

In the ICODE=1 section, parameters VSUP, VOLIM, ISC, and FB are checked. If any invalid value occurs, an error

message is issued by calling the WATAND utility routine USRMSG, and the error flag IERR is set to 1. After all parameters are checked, the IERR flag is checked and the routine is exited with VAL(1)=1 if IERR=1. Stored parameters such as IMH, IML, VM, IB1, etc., are calculated and moved to storage positions after the check section.

If AUTOSP (automatic sample-point flag) is 1, the subroutine generates a set of sample-point values by calling a WATAND utility routine UDSAP [see Ref. 4]. Because the input voltage, VI, is limited by IML/GM2 and IMH/GM2 for slew-rate limiting in the interstage, sample-point SPVI has two break-points, IML/GM2 and IMH/GM2. SA(1), SA(2), SA(6), and SA(7) are set at or near the break-points. SA(3) and SA(5) are choosen near SA(4) which is 0. SPV1 and SPVI values are identical for the RC circuit model.

The maximum and minimum output voltages (VOMH and VOML) are used as break-points for SPV2. The supply voltages are chosen for SA(1) and SA(7). SA(2) and SA(6) are set equal to VOMH and VOML. VM, a middle point between supply voltages, is chosen for SA(4). SA(3) is set between VM and VOML, and SA(4) is set between VM and VOMH. SPVR also has two break-points, -ISC*RO and ISC*RO. SA(1), SA(2), SA(4), and SA(5) are chosen at or near these break-points, and SA(3) is set to 0.

If the IER return from UDSAP does not equal zero, an error message is issued and IERR is set to 1. After all

sample-points are set, IERR is checked again, and if it is equal to 1, the routine is exited with VAL(1)=1.

In the ICODE=2 section, the values of the functions (dependent sources) are calculated. The equations used are from Chapter 3.

Table 4-5 RC Circuit Method Fortran Subroutine.

OA FORTRAN:

```
C*************************************************************************
      SUBROUTINE OA (ICODE,PAR,VAR,VAL,EPAR,MIDA,DERIV)
C*************************************************************************
C
C     OPERATIONAL AMPLIFIER (USING RC CIRCUIT METHOD)
C
C     CREATED  25-OCT-1987     B.R. HSU    EE DEPT. YSU
C*************************************************************************
      REAL*8 PAR(1),VAR(1),VAL(1),EPAR(1),DERIV(1,1),
     *       SA(7),INC(6),DE,LE,HE,
     *       ERMSG(5),CNSA(4),
     *       VPOS,VNEG,A0,RI,CI,RO,SRP,SRN,F1,F2,VOS,IOS,IB,RIC,ISC,
     *       VOLIMH,VOLIML,AUTOSP,
     *       C1,R1,C2,R2,GM1,GM2,IMH,IML,IB1,IB2,VOMH,VOML,VM,LPAR(31),
     *       VI,V1,V2,VR,I1,I2,VL,IL,TWOPI,IO,ID
      INTEGER ICODE,MIDA(1),IVAR,NSA,IER,IERR
      LOGICAL*1 ERMSG1(40),CNIER(4)
      EQUIVALENCE
     *      (LPAR( 1), VPOS  ), (LPAR( 2), VNEG  ), (LPAR( 3), A0    ),
     *      (LPAR( 4), RI    ), (LPAR( 5), CI    ), (LPAR( 6), RO    ),
     *      (LPAR( 7), SRP   ), (LPAR( 8), SRN   ), (LPAR( 9), F1    ),
     *      (LPAR(10), F2    ), (LPAR(11), VOS   ), (LPAR(12), IOS   ),
     *      (LPAR(13), IB    ), (LPAR(14), RIC   ), (LPAR(15), ISC   ),
     *      (LPAR(16), VOLIMH), (LPAR(17), VOLIML), (LPAR(18), AUTOSP)
      EQUIVALENCE
     *      (LPAR(19), C1    ), (LPAR(20), R1    ), (LPAR(21), C2    ),
     *      (LPAR(22), R2    ), (LPAR(23), GM1   ), (LPAR(24), GM2   ),
     *      (LPAR(25), IMH   ), (LPAR(26), IML   ), (LPAR(27), IB1   ),
     *      (LPAR(28), IB2   ), (LPAR(29), VOMH  ), (LPAR(30), VOML  ),
     *      (LPAR(31), VM    )
      EQUIVALENCE (ERMSG(1), ERMSG1(1))
C
      DATA ERMSG/'UDSAP: I','ER = # F','OR SAMPL','E POINT ','########'/
     *     ,CNIER/'1','2','3','4'/
     *     ,CNSA/'SPVI','SPV1','SPV2','SPVR'/
     *     ,TWOPI/6.283185307179586D0/
C
C+++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++
C
C...TRANSFER WATAND PARAMETERS INTO LOCAL STORAGE
      DO 10 J=1,31
10    LPAR(J)=PAR(J)
```

```
C
C...CHECK TO SEE IF IT IS INITIAL CALL
      IF(ICODE.EQ.2)  GOTO 200
C
C++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++
C...ICODE=1
C...INITIALIZE CONSTANT
      IERR=0
C
C...CHECK SUPPLY VOLTAGES
      IF(VPOS.GT.VNEG) GOTO 20
      CALL USRMSG('VPOS <= VNEG',12,8)
      IERR=1
C
C...CHECK PARAMETER VOLIMH
20    IF(VOLIMH.GE.(VNEG-VPOS)/2D0.AND.VOLIMH.LE.0D0) GOTO 30
      CALL USRMSG('VOLIMH > 0 OR < (VNEG-VPOS)/2',29,8)
      IERR=1
C
C...CHECK PARAMETER VOLIML
30    IF(VOLIML.LE.(VPOS-VNEG)/2D0.AND.VOLIML.GE.0D0) GOTO 50
      CALL USRMSG('VOLIML < 0 OR > (VPOS-VNEG)/2',29,8)
      IERR=1
C
C...CHECK PARAMETER ISC
50    IF(ISC.GE.0D0) GOTO 60
      CALL USRMSG('ISC < 0',7,8)
      IERR=1
C
C...CHECK PARAMETER F1
60    IF(F1.GT.0D0) GOTO 70
      CALL USRMSG('F1 <= 0',7,8)
      IERR=1
C
C...CHECK PARAMETER F2
70    IF(F2.GT.0D0) GOTO 80
      CALL USRMSG('F2 <= 0',7,8)
      IERR=1
C
C...CHECK ERROR FLAG
80    IF(IERR.NE.0) GOTO 140
C
C...OUTPUT CURRENT SWING
      IMH=(VPOS+VOLIMH)/RO
      IML=-IMH*SRN/SRP
C
C...DOMINANT POLE STAGE
      C2=IMH/SRP
      R2=1D0/(TWOPI*F1*C2)
      GM2=A0/R2
C
C...SECOND POLE STAGE
      R1=1D2
      C1=1D0/(TWOPI*F2*R1)
      GM1=1D0/R1
C
C...SET INPUT BIAS CURRENT
      IB1=IB+IOS/2D0
      IB2=IB-IOS/2D0
C
C...SET VOLTAGE LEVEL FOR INPUT STAGE
      VM=(VPOS+VNEG)/2D0
C
C...SET OUTPUT VOLTAGE SWING
      VOMH=VM+(VPOS-VNEG)/2D0+VOLIMH
      VOML=VM-(VPOS-VNEG)/2D0+VOLIML
```

```
C
C...CHECK AUTO SAMPLE POINT FLAG
      IF(AUTOSP.NE.1D0) GOTO 150
C
C...SET SPVI SAMPLE POINT
      IVAR=1
      SA(1)=-1D0+IML/GM2
      INC(1)=1D0
      SA(2)=SA(1)+1D0
      SA(3)=SA(2)/1D1
      INC(2)=SA(3)-SA(2)
      INC(3)=-SA(3)
      SA(4)=0D0
      INC(4)=IMH/GM2/1D1
      SA(5)=INC(4)
      INC(5)=INC(4)*9D0
      SA(6)=INC(4)*1D1
      INC(6)=1D0
      SA(7)=1D0+SA(6)
      DE=0D0
      LE=5D0
      HE=5D0
      NSA=7
      GOTO 120
C
C...SET SPV1 SAMPLE POINT
90    IVAR=2
      GOTO 120
C
C...SET SPV2 SAMPLE POINT
100   IVAR=3
      SA(1)=VNEG
      INC(1)=VOML-VNEG
      SA(2)=VOML
      SA(3)=(3D0*VOML+VOMH)/4D0
      INC(2)=SA(3)-SA(2)
      SA(4)=VM
      INC(3)=SA(4)-SA(3)
      SA(5)=(VOML+3D0*VOMH)/4D0
      INC(4)=SA(5)-SA(4)
      SA(6)=VOMH
      INC(5)=SA(6)-SA(5)
      INC(6)=VPOS-VOMH
      SA(7)=VPOS
      DE=0D0
      LE=5D0
      HE=5D0
      NSA=7
      GOTO 120
C
C...SET SPVR SAMPLE POINT
110   IVAR=4
      SA(1)=-ISC*RO-1D-1
      INC(1)=1D-1
      SA(2)=SA(1)+1D-1
      INC(2)=-SA(2)
      SA(3)=0D0
      INC(3)=INC(2)
      SA(4)=INC(2)
      INC(4)=1D-1
      SA(5)=INC(2)+1D-1
      DE=0D0
      LE=5D0
      HE=5D0
      NSA=5
```

```
C...CALL UDSAP, IF ERROR, SEND ERROR MESSAGE AND RETURN
120   CALL UDSAP(MIDA,DERIV,IVAR,DE,LE,HE,SA,INC,NSA,IER)
      IF(IER.EQ.0) GOTO (90,100,110,130),IVAR
      ERMSG1(14)=CNIER(IER)
      ERMSG(5)=CNSA(IVAR)
      CALL USRMSG(ERMSG,36,8)
C
C...SET ERROR FLAG
      IERR=1
      GOTO (90,100,110),IVAR
C
C...CHECK ERROR FLAG, IF =1, FLAG WATAND TO TERMINATE THE OPERATION
130   IF(IERR.NE.1)  GOTO 150
140   VAL(1)=1D0
      GOTO 999
C
C...TRANSFER INTERNAL PARAMETERS BACK TO WATAND
150   DO 160 I=19,31
160   PAR(I)=LPAR(I)
      GOTO 999
C
C++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++
C...ICODE=2
C...EVALUATE FUNCTION VALUES
C
C...GET VARIABLES
200   VI=VAR(1)
      V1=VAR(2)
      V2=VAR(3)
      VR=VAR(4)
C
C...CURRENT IN THE SECOND POLE STAGE
      I1=GM1*VI
C
C...FIRST POLE STAGE GAIN AND SLEW RATE LIMIT
      I2=GM2*V1
      IF(I2.LT.IML) I2=IML
      IF(I2.GT.IMH) I2=IMH
C
C...LIMIT CURRENT IN THE FIRST POLE STAGE
      ID=0D0
      IF(V2.GT.VOMH) ID=DEXP(V2-VOMH)-1D0
      IF(V2.LT.VOML) ID=-(DEXP(VOML-V2)-1D0)
      12-12-ID
C
C...SET OUTPUT VOLTAGE LIMITING
      VL=V2
      IF(VL. GT.VOMH) VL=VOMH
      IF(VL.LT.VOML) VLTVOML
C
C...SET OUTPUT CURRENT LIMITING
      IO=VR/RO
      ILTODO
      IF(IO.GT.ISC) IL=IO-ISC
      IF(IO.LT.-ISC) IL=IO+ISC
C
C...ASSIGN FUNCTION VALUES AND RETURN
      VAL(1)=VOS
      VAL(2)=IB1
      VAL(3)=IB2
      VAL(4)=VM
      VAL(5)=I1
      VAL(6)=I2
      VAL(7)=VL
      VAL(8)=IL
999   RETURN
```

OA2 FORTRAN:

```
C*********************************************************************
      SUBROUTINE OA2 (ICODE,PAR,VAR,VAL,EPAR,MIDA,DERIV)
C*********************************************************************
C
C     OPERATIONAL AMPLIFIER (USING Q SOURCE METHOD)
C
C     CREATED 17-OCT-87    B.R. HSU    EE DEPT. YSU
C*********************************************************************
      REAL*8 PAR(1),VAR(1),VAL(1),EPAR(1),DERIV(1,1),
     *       SA(7),INC(6),DE,LE,HE,
     *       ERMSG(5),CNSA(4),
     *       VPOS,VNEG,A0,RI,CI,RO,SRP,SRN,F1,F2,
     *       VOS,IOS,IB,RIC,ISC,VOLIMH,VOLIML,AUTOSP,
     *       IB1,IB2,VMH,VML,VOMH,VOML,VM,R1,LPAR(26),
     *       VI,V1,V2,VR,QA,QB,IQ,VL,IL,IO,DEXP,TWOPI
      INTEGER ICODE,MIDA(1),IVAR,NSA,IER,IERR
      LOGICAL*1 ERMSG1(40),CNIER(4)
C
     *EQUIVALENCE
     *      (LPAR( 1), VPOS  ), (LPAR( 2), VNEG  ), (LPAR( 3), A0    ),
     *      (LPAR( 4), RI    ), (LPAR( 5), CI    ), (LPAR( 6), RO    ),
     *      (LPAR( 7), SRP   ), (LPAR( 8), SRN   ), (LPAR( 9), F1    ),
     *      (LPAR(10), F2    ), (LPAR(11), VOS   ), (LPAR(12), IOS   ),
     *      (LPAR(13), IB    ), (LPAR(14), RIC   ), (LPAR(15), ISC   ),
     *      (LPAR(16),VOLIMH ), (LPAR(17),VOLIML ), (LPAR(18), AUTOSP)
      EQUIVALENCE
     *      (LPAR(19), VMH   ), (LPAR(20), VML   ), (LPAR(21), IB1   ),
     *      (LPAR(22), IB2   ), (LPAR(23), VOMH  ), (LPAR(24), VOML  ),
     *      (LPAR(25), VM    ), (LPAR(26), R1    )
      EQUIVALENCE
     *      (ERMSG(1), ERMSG1(1))
C
      DATA ERMSG/'UDSAP: I','ER = # F','OR SAMPL','E POINT ','########'/
     *     ,CNIER/'1','2','3','4'/
     *     ,CNSA/'SPVI','SPV1','SPV2','SPVR'/
     *     ,TWOPI/6.283185307179586D0/
C
C+++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++
C
C...TRANSFER WATAND PARAMETERS INTO LOCAL STORAGE
      DO 10 J=1,26
10    LPAR(J)=PAR(J)
C
C...CHECK ICODE
      IF(ICODE.EQ.2) GOTO 200
C
C++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++
C...ICODE=1
C...INITIALIZE CONSTANT
      IERR=0
      R1=1D0
C
C...CHECK SUPPLY VOLTAGES
      IF(VPOS.GT.VNEG) GOTO 20
      CALL USRMSG('VSUP.1 <= VSUP.2',16,8)
      IERR=1
C
C...CHECK PARAMETER VOLIMH
20    IF(VOLIMH.GE.-VPOS.AND.VOLIMH.LE.0D0) GOTO 25
      CALL USRMSG('VOLIM.1 > 0 OR < -VSUP.1',24,8)
      IERR=1
```

```
C
C...CHECK PARAMETER VOLIML
25    IF(VOLIML.LE.-VNEG.OR.VOLIML.GE.0D0) GOTO 30
      CALL USRMSG('VOLIM.2 < 0 OR > -VSUP.2',24,8)
      IERR=1
C
C...CHECK PARAMETER ISC
30    IF(ISC.GE.0D0) GOTO 40
      CALL USRMSG('ISC < 0',7,8)
      IERR=1
C
C...CHECK PARAMETER F1
40    IF(F1.GT.0D0) GOTO 45
      CALL USRMSG('FB.1 <= 0',9,8)
      IERR=1
C
C...CHECK PARAMETER F2
45    IF(F2.GT.0D0) GOTO 50
      CALL USRMSG('FB.2 <= 0',9,8)
      IERR=1
C
C...CHECK ERROR FLAG
50    IF(IERR.EQ.1)  GOTO 120
C
C...SET INPUT BIAS CURRENT
      IB1=IB+IOS/2D0
      IB2=IB-IOS/2D0
C
C...CALCULATE MAXIMUM INPUT VOLTAGE FOR SLEW RATE LIMITING
      VMH=SRP/(TWOPI*F1*A0)
      VML=-SRN/(TWOPI*F1*A0)
C
C...SET VOLTAGE LEVEL FOR INPUT STAGE
      VM=(VPOS+VNEG)/2D0
C
C...COMPUTE MAXIMUM OUTPUT VOLTAGE
      VOMH=VM+(VPOS-VNEG)/2D0+VOLIMH
      VOML=VM-(VPOS-VNEG)/2D0+VOLIML
C
C...CHECK AUTO SAMPLE POINT FLAG
      IF(AUTOSP.NE.1D0) GOTO 130
C
C...SET SPVI SAMPLE POINT
      IVAR=1
      SA(1)=-1D0+VML
      SA(2)=VML-1D-3
      INC(1)=999D-3
      SA(3)=VML
      INC(2)=1D-3
      SA(4)=VMH
      INC(3)=VMH-VML
      SA(5)=VMH+1D-3
      INC(4)=1D-3
      SA(6)=1D0+VMH
      INC(5)=999D-3
      DE=0D0
      LE=5D0
      HE=5D0
      NSA=6
      GOTO 100
```

```
C
C...SET SPV1 SAMPLE POINT
60    IVAR=2
      SA(1)=-1D5
      INC(1)=99D3
      SA(2)=-1D3
      INC(2)=1D3
      SA(3)=0D0
      INC(3)=1D3
      SA(4)=1D3
      INC(4)=99D3
      SA(5)=1D5
      DE=0D0
      LE=1D7
      HE=1D7
      NSA=5
      GOTO 100
C
C...SET SPV2 SAMPLE POINT
70    IVAR=3
      SA(1)=VNEG
      SA(2)=VOML
      INC(1)=SA(2)-SA(1)
      SA(3)=(3D0*VOML+VOMH)/4D0
      INC(2)=SA(3)-SA(2)
      SA(4)=VM
      INC(3)=SA(4)-SA(3)
      SA(5)=(VOML+3D0*VOMH)/4D0
      INC(4)=SA(5)-SA(4)
      SA(6)=VOMH
      INC(5)=SA(6)-SA(5)
      SA(7)=VPOS
      INC(6)=SA(7)-SA(6)
      DE=0D0
      LE=1D1
      HE=1D1
      NSA=7
      GOTO 100
C
C...SET SPVR SAMPLE POINT
80    IVAR-4
      SA(1)=-ISC*RO-1D-3
      INC(1)=1D-3
      SA(2)=-ISC*RO
      INC(2)=-SA(2)
      SA(3)=0D0
      INC(3)=INC(2)
      SA(4)=INC(2)
      INC(4)=1D-3
      SA(5)=INC(2)+1D-3
      DE=0D0
      LE=5D0
      HE=5D0
      NSA=5
C
C...CALL UDSAP, IF ERROR, SEND ERROR MESSAGE AND RETURN
100   CALL UDSAP(MIDA,DERIV,IVAR,DE,LE,HE,SA,INC,NSA,IER)
      IF(IER.EQ.0) GOTO (60,70,80,110),IVAR
      ERMSG1(14)=CNIER(IER)
      ERMSG(5)=CNSA(IVAR)
      CALL USRMSG(ERMSG,36,8)
C
C...SET ERROR FLAG
      IERR=1
      GOTO (60,70,80),IVAR
```

```
C
C...CHECK ERROR FLAG, IF = 1, FLAG WATAND TO TERMINATE THE OPERATION
110   IF(IERR.NE.1)  GOTO 130
120   VAL(1)=1D0
      GOTO 999
C
C...TRANSFER INTERNAL PARAMETERS BACK TO WATAND
130   DO 140 I=19,26
140   PAR(I)=LPAR(I)
      GOTO 999
C
C+++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++
C...ICODE=2 (EVALUATE FUNCTION VALUES)
C...GET VARIABLES
200   VI=VAR(1)
      V1=VAR(2)
      V2=VAR(3)
      VR=VAR(4)
C
C...LIMIT INPUT VOLTAGE CHANGE FOR SLEW RATE FUNCTION
      IF(VI.GT.VMH) VI=VMH
      IF(VI.LT.VML) VI=VML
C
C...TWO-POLE GAIN FUNCTIONAND VOLTAGE LIMITING
      QA=V2
      QB=V1/(F1*F2*TWOPI**2)
      IQ=A0*VI-(F1+F2)*V1/(F1*F2*TWOPI)
      IF(V2.LT.VOML) IQ=IQ+(DEXP(VOML-V2)-1D0)
      IF(V2.GT.VOMH) IQ=IQ-(DEXP(V2-VOMH)-1D0)
C
C...SET OUTPUT VOLTAGE SWING
      VL=V2
      IF(VL.GT.VOMH) VL=VOMH
      IF(VL.LT.VOML) VL=VOML
C
C...SET MAXIMUM OUTPUT CURRENT
      IO=VR/RO
      IL=0D0
      IF(IO.GT.ISC) IL=IO-ISC
      IF(IO.LT.-ISC) IL=IO+ISC
C
C...ASSIGN FUNCTION VALUES AND RETURN
      VAL(1)=VOS
      VAL(2)=IB1
      VAL(3)=IB2
      VAL(4)=VM
      VAL(5)=QA
      VAL(6)=QB
      VAL(7)=IQ
      VAL(8)=VL
      VAL(9)=IL
999   RETURN
      END
```

CHAPTER V

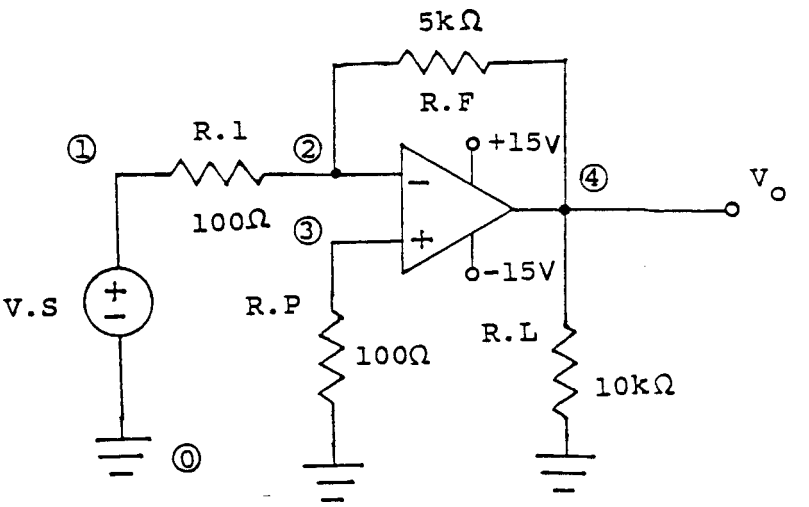
MACROMODEL PERFORMANCE

To investigate the validity of the macromodel, five illustrative examples are presented in this chapter. These examples cover a wide range of applications. The RC circuit model with the default **741** op amp parameters is used for these simulations. **741C** op amps are used for the laboratory tests. The results of computer simulations are compared with experiments, and an execution time comparison between the RC circuit and the Q source models is presented in section **5.6**. All examples are run using WATAND version **1.10-00**.

5.1 INVERTING AMPLIFIER

The inverting amplifier circuit of Fig. **5-1** provides tests with respect to voltage gain versus frequency and voltage limits. The simulation output is compared with the experiments and is shown in Figs. **5-2** to **5-4**. Fig. **5-2** is the frequency domain analysis of the voltage gain. The transient responses of **sinewave** inputs with peak **value 0.3** V is shown in Fig. **5-3** and with peak value of **10** V is shown in Fig. **5-4**. The results show good agreement with the values found experimentally. The offset characteristics are also tested for this circuit and are shown in Table **5-1**. The first DC analysis shown there is with zero offset current and voltage. The second analysis has offset voltage of

2 mV. The last DC analysis is with bias current of 80 nA and offset current 20 nA. These results show that the offset voltage causes more DC shift than the bias and offset currents do, for this circuit.



IAMP WATAND:

```
#T AN INVERTING AMPLIFIER
#M
OA.1
#D
V.S 1 0 SIN .3 1K 0
R.l 1 2 100
R.P 3 0 100
R.F 2 4 5K
R.L 4 0 10K
OA.l.l 3 2 4 0
#E
#GV GAIN ( V 4 / V 1 )
#GI V.S V 1
DC PR OU ALL
TC PS V.S NPER 2 OU V 4 G VIN VB -15 15 IB -.5 .5 PL
FR BE 100 EN 10ME LO 10 DB PP OU G GAIN VB -10 40 KE ALL ON D
#S
```

Fig. 5-1 An Inverting Amplifier Circuit and its WATAND Netlist.

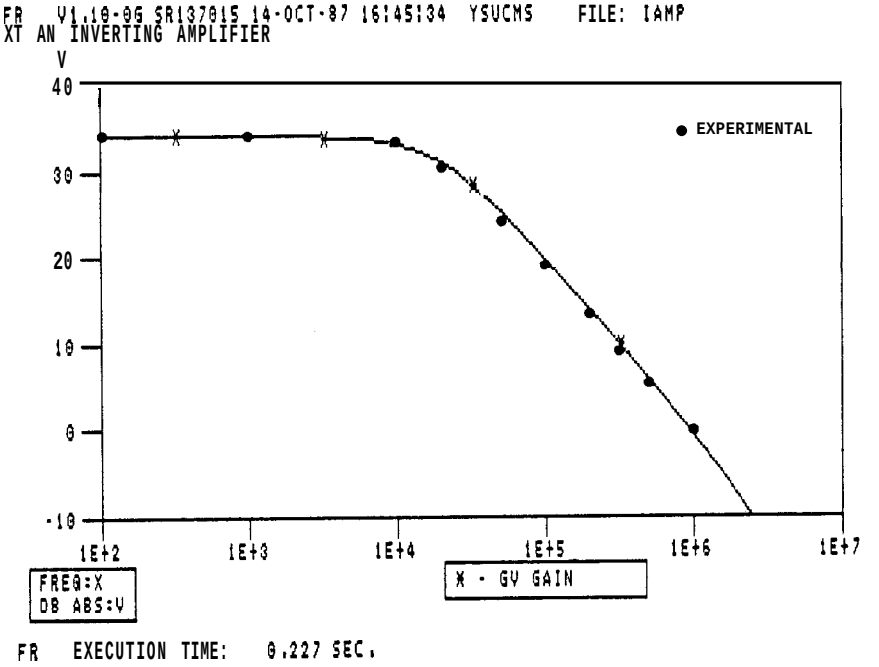


Fig. 5-2 WATAND and Experimental Voltage Gain Versus Frequency.

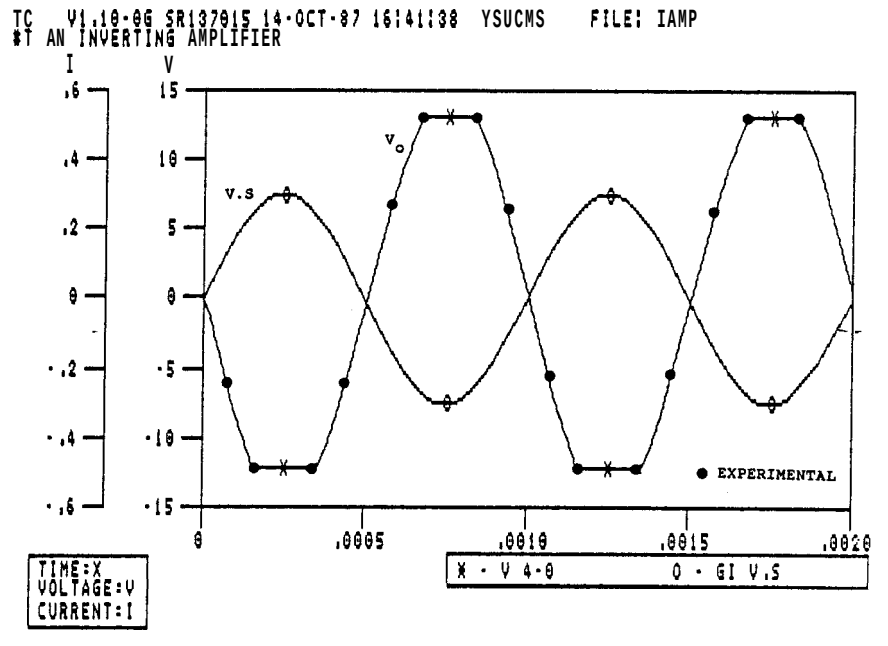


Fig. 5-3 Voltage Limiting Effect with V.S = 0.3 V Amplitude.

Table 5-1 DC Solutions of the Inverting Amplifier.

```
dc

DC   V1.10-0g SR137015 15-OCT-87 21:41:20  YSUCMS    FILE: IAMP


----------------------------
SOL'N #  1 (DET -)   0 ITER.
----------------------------
  (   1)  0.0           (   2) -1.66542D-18   (   3) -8.32667D-23
  (   4) -8.49405D-17   (
  I    V.S           -1.66542D-20   A1   OA.1          -1.66542D-18
  A2   OA.1           0.0           A3   OA.1           9.87708D-19
  A4   OA.l          -8.68266D-17   A5   OA.1          -8.68266D-17
  A6   OA.l          -8.32667D-25   A7   OA.1          -8.32750D-28
  A8   OA.1           2.51491D-20


DC   EXECUTION TIME-   0.003 SEC.

#am oa.1 vos 2m
ALTER PERFORMED
dc

DC   V1.10-0g SR137015 15-OCT-87 21:41:36  YSUCMS    FILE: IAMP


----------------------------
SOL'N #  1 (DET -)   5 ITER.
----------------------------
  (   1)  0.0           (   2)  1.99948D-03   (   3) -2.60595D-11
  (   4)  1.01973D-01   (
  I    V.S           1.99948D-05   A1   OA.1          -5.21215D-07
  A2   OA.1          0.0           A3   OA.l           5.21189D-07
  A4   OA.l          1.04238D-01   A5   OA.l           1.04238D-01
  A6   OA.l         -2.60595D-13   A7   OA.1           9.99739D-13
  A8   OA.1         -3.01921D-05


DC   EXECUTION TIME=   0.023 SEC.

#am oa.1 vos 0 ib 80n ios 20n
ALTER PERFORMED
dc

DC   V1.10-0g SR137015 15-OCT-87 21:41:55  YSUCMS    FILE: IAMP


----------------------------
SOL'N #  1 (DET -)   4 ITER.
----------------------------
  (   1)  0.0           (   2) -8.99944D-06   (   3) -9.00000D-06
  (   4) -1.08972D-04   (
  I    V.S           -8.99944D-08   A1   OA.1          -8.99944D-06
  A2   OA.l           0.0           A3   OA.1          -5.56442D-10
  A4   OA.1          -1.11288D-04   A5   OA.l          -1.11288D-04
  A6   OA.l           2.78221D-16   A7   OA.l           1.60000D-07
  A8   OA.1           3.08916D-08


DC   EXECUTION TIME=   0.027 SEC.
```

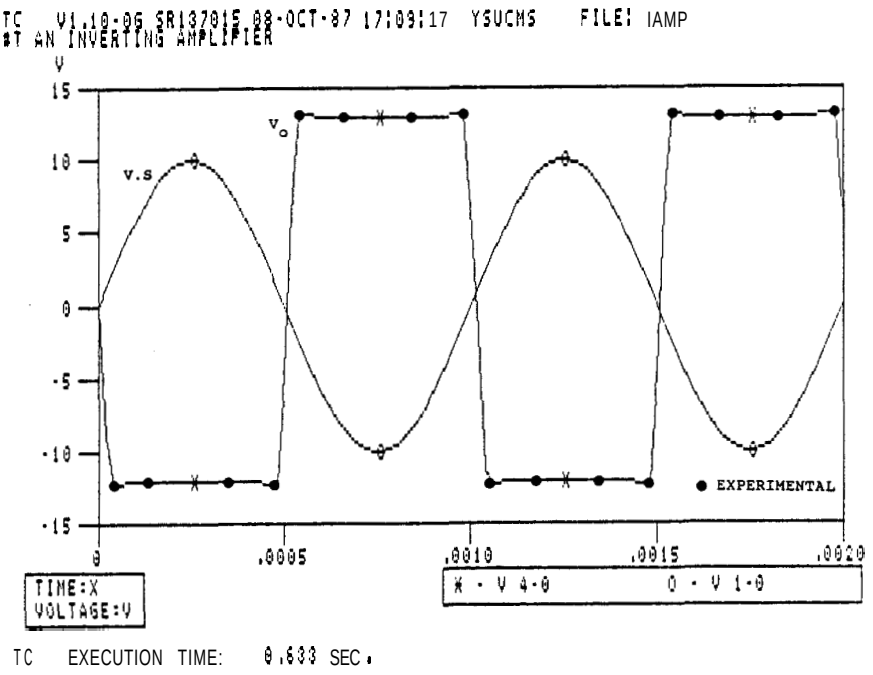
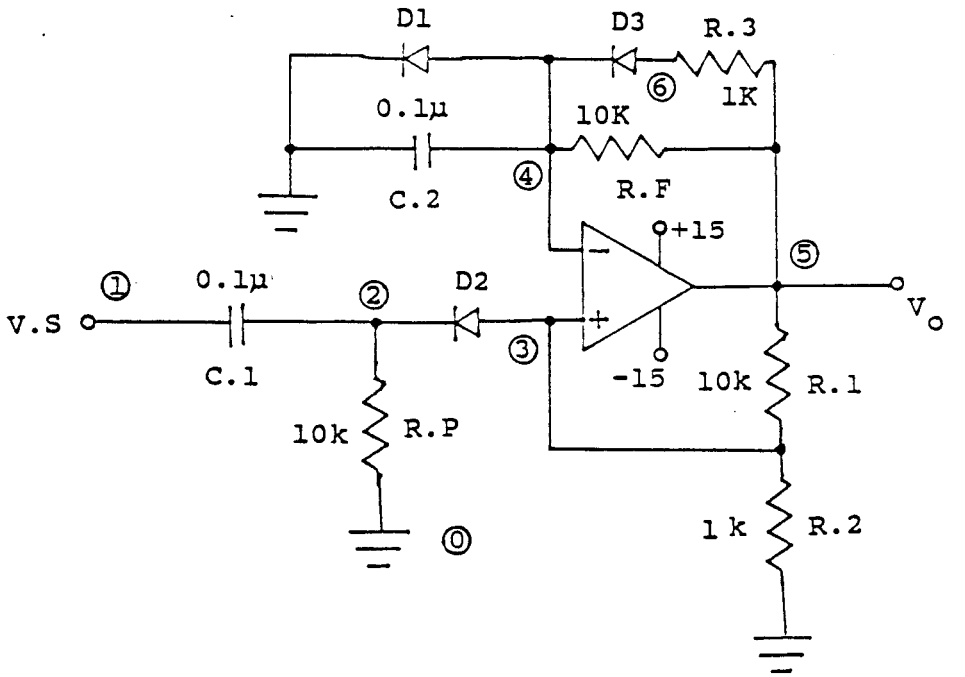


Fig. 5-4 Voltage Limiting Effect with V.S = 10 V Amplitude.

5.2 MONOSTABLE MULTIVIBRATOR

To estimate the slew rate characteristics and output voltage limits of the op amp model, the monostable multivibrator circuit [18] shown in Fig. 5-5 is simulated. The DT analysis (DT SN 4 3 SO -lM 1M ZS) shows three DC solutions in this circuit (see Table 5-2). The last DC solution is the desired initial point for TC analysis. Fig. 5-6 is the simulation output and the experimental result. The slopes from point A to B and C to D show the slew rate limiting. A sharper sloped pulse can be generated by using a faster slew-rate op amp such as the LF355. It is seen that the simulation and experimental output are in good agreement.



MONS WATAND:

```
#T A MONOSTABLE MULTIVIBRATOR
#M
OA.1
D1.l
#D
V.S 1 0 PW 0 0 20MU 0 20.001MU -5 100MU -5 100.001MU 0
R.P 2 0 10K
R.F 4 5 10K
R.l 5 3 10K
R.2 3 0 1K
R.3 6 5 1K
C.l 1 2 .1MU
C.2 4 0 .1MU
D1.l.l 4 0
D1.1.2 3 2
D1.1.3 6 4
OA.l.l 3 4 5 0
#E
DT SN 4 3 SO -lM 1M ZS OU ALL PR
TC IP DT OU V 5 V 1 EN .4M DE 1MU VB -15 15 PL
#S
```

Fig. 5-5 A Monostable Multivibrator Circuit and its WATAND Netlist.

Table 5-2 The DC Solutions of the Monostable Multivibrator.

```
dt
DT   V1.10-0g SR137015 17-OCT-87 12:53:25  YSUCMS    FILE:MONS


----------------------------
SOL'N #  1 (DET -)  19 ITER.
----------------------------
  (   1)  0.0           (   2) -8.41750D-13   (   3) -8.41834D-09
  (   4) -1.24779D-08   (   5)  7.99907D-04   (   6)  7.99899D-04
  I    V.S          0.0          A1   D1.1          -1.24779D-16
  A1   D1.2        -8.41834D-13   A1   D1.3          -1.24699D-08
  A1   OA.1        -1.24779D-08   A2   OA.1           0.0
  A3   OA.1         4.05953D-09   A4   OA.l           8.11907D-04
  A5   OA.1         8.11907D-04   A6   OA.l          -2.02977D-15
  A7   OA.1         1.60000D-07   A8   OA.l          -1.59992D-07

----------------------------
SOL'N #  2 (DET +)  38 ITER.
----------------------------
  (   1)  0.0           (   2)  1.32847D-01   (   3)  7.33079D-01
  (   4)  7.33035D-01   (   5)  8.19752D+00   (   6)  1.46256D+00
  I    V.S          0.0          A1   D1.1           7.48133D-03
  A1   D1.2         1.32860D-01   A1   D1.3           7.39770D-01
  A1   OA.l         7.33035D-01   A2   OA.l           0.0
  A3   OA.1         4.40731D-05   A4   OA.1           8.81461D+00
  A5   OA.1         8.81461D+00   A6   OA.1          -2.20365D-11
  A7   OA.1         1.60733D-07   A8   OA.l          -8.22786D-03

----------------------------
SOL'N #  3 (DET -)  52 ITER.
----------------------------
  (   1)  0.0           (   2)  4.85614D-01   (   3)  1.09213D+00
  (   4)  7.55084D-01   (   5)  1.25016D+01   (   6)  1.50465D+00
  I    V.S          0.0          A1   D1.1           1.21717D-02
  A1   D1.2         4.85663D-01   A1   D1.3           7.66081D-01
  A1   OA.1         7.55084D-01   A2   OA.l           0.0
  A3   OA.l         3.37049D-01   A4   OA.l           1.35775D+01
  A5   OA.1         1.35000D+01   A6   OA.l          -1.68524D-07
  A7   OA.l         1.60924D-07   A8   OA.l          -1.33125D-02

DT   EXECUTION TIME=   0.273 SEC.
```

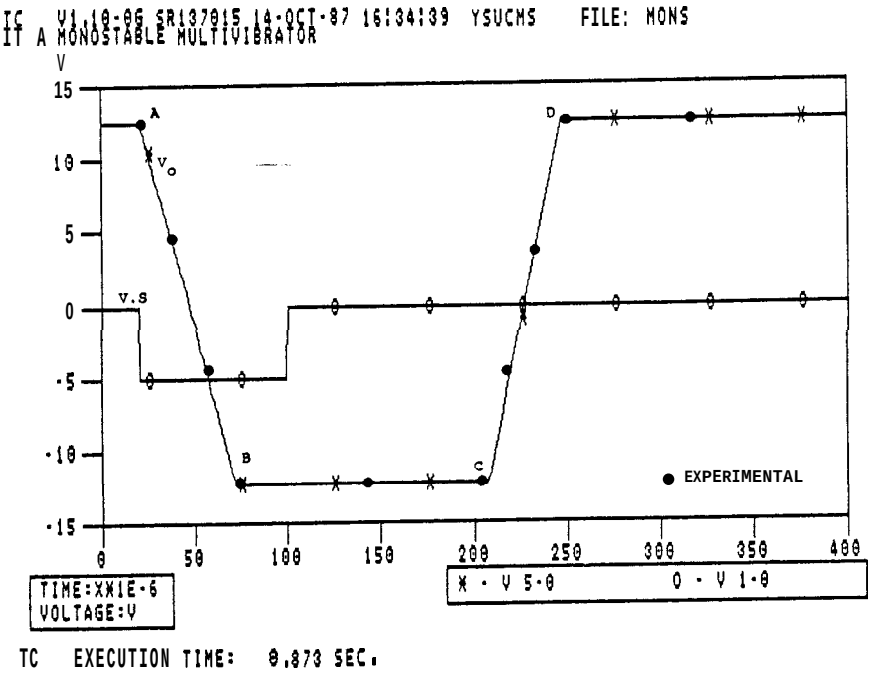
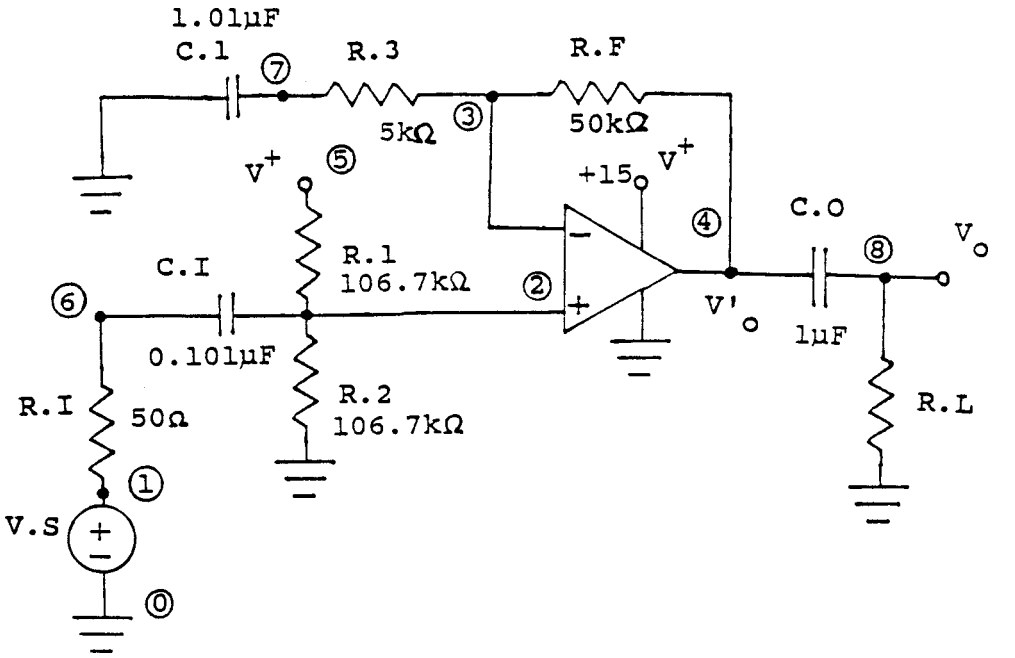


Fig. 5-6 The Input/Output Voltages of the Monostable Multivibrator.

5.3 SINGLE POWER SUPPLY NON-INVERTING AMPLIFIER

A non-inverting amplifier circuit using a single power supply [12] is shown in Fig. 5-7. The gain of this amplifier is 11. Fig. 5-8 is the output of the amplifier. V'_o is the output voltage with a average value of $V^+/2$. The bandwidth of this amplifier is shown in Fig. 5-9. The low frequency cutoff, f_l, and high frequency cutoff, f_h, from WATAND simulation are 50 Hz and 84k Hz. The experimental results for f_l and f_h are 50 Hz and 85k Hz. The results of the WATAND simulation and the experiment are very close.



SPS WATAND:

```
#T A NON-INVERTING AMPLIFIER WITH SINGLE SUPPLY
#M
OA.l VSUP 15 0 FB 4.5
#D
V.S 1 0 SIN .4 1K 0
V.CC 5 0 DC 15
R.F 4 3 50K
R.l 5 2 106.7K
R.2 2 0 106.7K
R.3 3 7 5K
R.I 6 1 50
C.l 7 0 1.01MU
C.I 2 6 .101MU
C.O 4 8 1MU
R.L 8 0 10K
OA.l.l 2 3 4 0
#E
#GV GAIN ( V 8 / V 1 )
#GI PHASE CALL GAPH ( V 8 / V 1 , -1 )
DC PR OU ALL
TC PS V.S NPER 2 OU V 4 V 8 VB -6 14 PP KE ALL ON D
FR BE 1 EN 10ME LO 10 PP OU G GAIN VB 0 12 KE ALL ON D
DI US FR ON D OU G PHASE VB 0 360 PP
#S
```

Fig. 5-7 A Single Power Supply Amplifier Circuit and its WATAND Netlist.

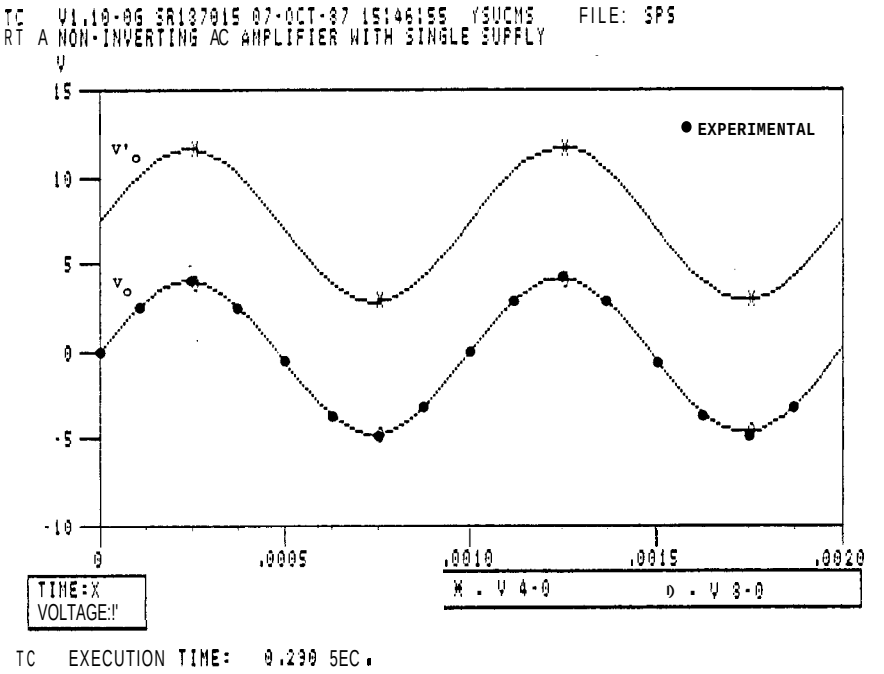


Fig. 5-8 Output Waveform of the Single-Supply Amplifier.

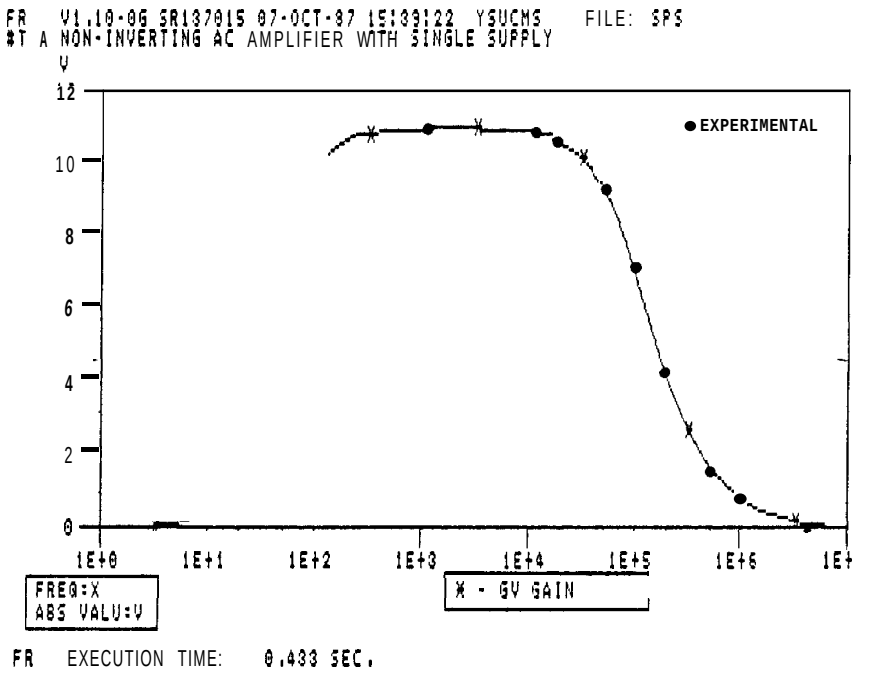


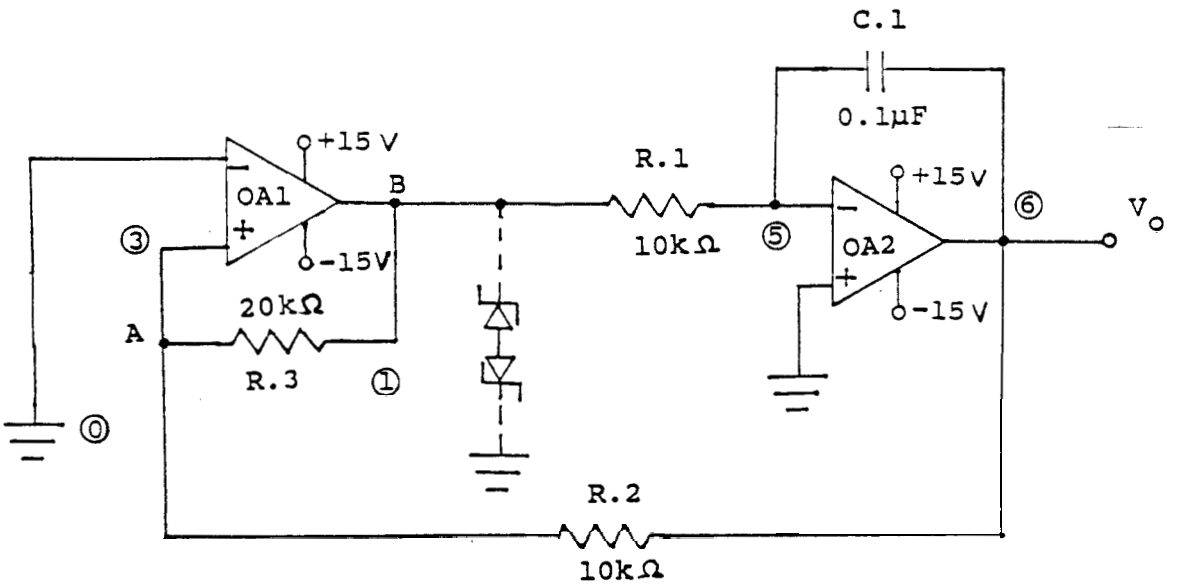
Fig. 5-9 Voltage Gain as a Function of Frequency.

5.4 TRIANGULAR WAVE GENERATOR

The triangular wave generator circuit shown in Fig. 5-10 consists of a comparator OA1 and an integrator OA2. The comparator compares the voltage at point A, V_A, continuously with the inverting input that is at 0 V. When V_A goes slightly above or below zero, the output of OA1, V_B, goes to the positive or negative saturation level, respectively. The integrator converts the square wave input, V_B to the triangular wave. The Zeners, D1 and D2, at the output of OA1 are used to limit the amplitude of the square wave. The circuit netlist in WATAND shown in Fig. 5-10 uses the parameter VOLIM to limit the square wave instead of using Zeners. Because the output of OA1, V_B, is bistable, a command (#IP DC AL VN 1 7) is used to apply a pulse to the circuit at zero time which initiates oscillation. The DC solution is shown in Fig. 5-11 with node 1 of seven Volts. The result of the simulation and the experiment shown in Fig. 5-11 again agree well.

5.5 R-active bandpass filter

An R-active bandpass filter using two op amps is shown in Fig. 5-12. The simulation results in the small signal response are compared with the experiments presented in Ref. [8] and both are very similar (see Fig. 5-13). The center frequency is 100k Hz for both simulation and experimental result.




```
TRI WATAND:

#T TRIANGULAR GENERATOR   (F=500) (#IP DC AL VN 1 7)
#M
OA.A VOLIM -7.6 7.6
OA.B
#D
R.l 1 5 10K
R.2 3 6 10K
R.3 3 1 20K
C.l 5 6 .1MU
OA.A.1 3 0 1 0
OA.B.2  0 5 6 0
#E
DC OU ALL PR
TC OU V 6 V 1 EN 4M DE 20MU VB -8 8 PP
#S
```

Fig. 5-10 A Triangular Wave Generator Circuit and its WATAND Netlist.

```
#ip dc al vn 1 7
#q tip (dc
IP NAME: DC
  (   1)  7.00000D+00    (   3)  3.83209D-09    (   5) -2.12267D-09
  (   6)  4.21060D-04    (
  A1    OA.1            0.0             A2    OA.1            0.0
  A3    OA.1            3.83209D-09     A4    OA.l            7.66418D-04
  A5    OA.1            7.66418D-04     A6    OA.l           -1.91604D-15
  A7    OA.1            1.60000D-07     A8    OA.l           -1.13684D-07
  A1    OA.2           -2.12267D-09     A2    OA.2            0.0
  A3    OA.2            2.12267D-09     A4    OA.2            4.24534D-04
  A5    OA.2            4.24534D-04     A6    OA.2           -1.06133D-15
  A7    OA.2            1.60000D-07     A8    OA.2           -4.63162D-08
EXTRA=  0.0
```

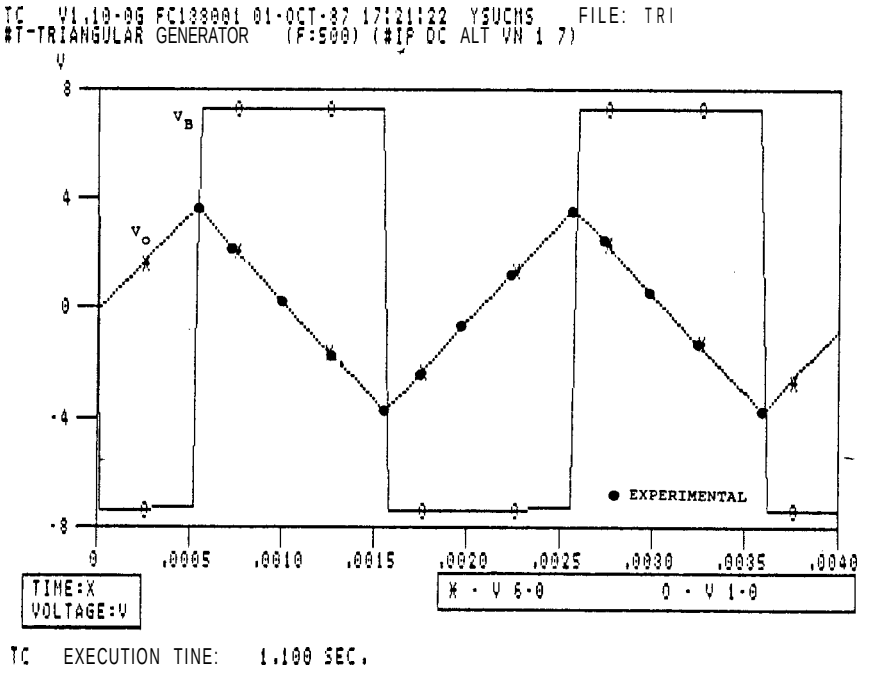
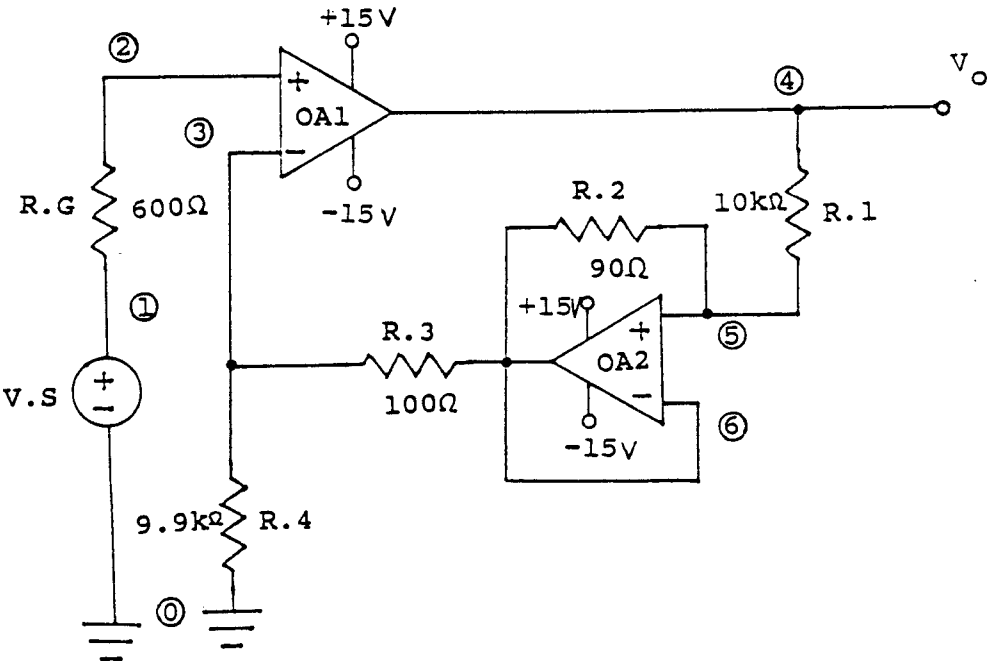


Fig. 5-11 The DC Initial Point and the Output Waveform of the Triangular Wave Generator.



BRF WATAND:

```
#T A BANDPASS R-ACTIVE FILTER
#M
OA.l FB 5.375
#D
V.S 1 0 SIN 3M 1K 0
R.G 1 2 600
R.l 4 5 10K
R.2 5 6 90
R.3 6 3 100
R.4 3 0 9.9K
OA.l.l 2 3 4 0
OA.1.2 5 6 6 0
#E
#GV GAIN ( V 4 / V 1 )
DC PR OU ALL
FR BE 50K EN 200K LI 200 DB PL OU G GAIN VB 15 45
#S
```

Fig. 5-12 An R-Active Bandpass Filter Circuit and its WATAND Netlist.

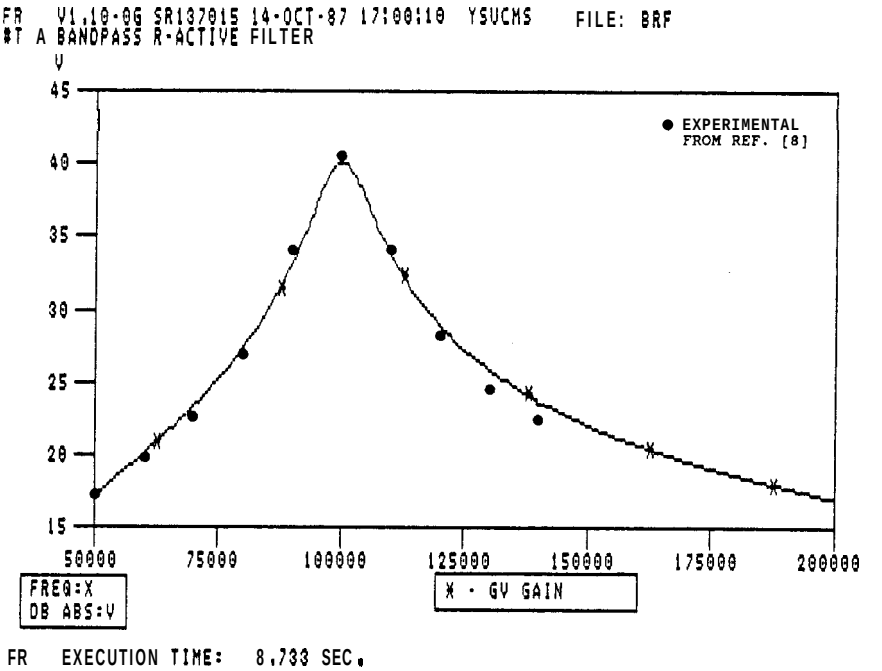


Fig. 5-13 The Response of an R-Active Bandpass Filter.

5.6 MODEL COMPARISON

The above computer outputs were simulated by using the RC circuit model. Simulations using the Q source model were run to compare with the RC circuit model's output. Simulation outputs for both models have only minor differences due to sample-point choice, but execution times are different. Table 5-1 is the CPU time list for these two models when running the above examples. In almost every case the RC model is faster than the Q source model, and. especially in FR (frequency domain) analysis.

Table **5-3** Simulation Time Comparison.

FILE	ANALYSIS	SIMULATION TIME (sec) Q source Model	RC circuit Model
IAMP	DC	0.033	0.03
	FR (Fig. **5-2**)	0.637	0.323
	TC (Fig. **5-3**)	0.683	0.547
	TC (Fig. **5-4**)	1.117	0.727
MONS	DC	0.027	0.04
	TC (Fig. **5-6**)	1.463	1.28
SPS	DC	0.07	0.147
	TC (Fig. **5-8**)	0.433	0.33
	FR (Fig. **5-9**)	1.43	0.48
TRI	DC	0.027	0.04
	TC (Fig. **5-11**)	1.77	1.19
BRF	DC	0.037	0.023
	FR (Fig. **5-13**)	6.243	4.93
SUBTOTAL	DC ANALYSIS	0.194	0.28
	TC ANALYSIS	5.466	4.074
	FR ANALYSIS	8.31	5.733
TOTAL CPU TIME		**13.97**	**10.087**

CHAPTER VI

CONCLUSION

Two macromodels of the operational amplifier have been presented. When designing these op amp macromodels, the major considerations were to keep the model size small (less execution time and memory space) and to model the op amp's large-signal response characteristics.

The macromodel using the RC circuit method has nine passive elements, eight dependent sources, and four independent variables. The other macromodel using the Q source method has seven passive elements, nine dependent sources, and four independent variables. The complexity of each of these macromodels is almost twice that of the BJT transistor models in WATAND. Compared with the real op amp, such as the 741 which has twenty four transistors and twelve passive elements, the size of these macromodels is small. These macromodels can simulate the most important characteristics, such as slew rate limiting, input and output characteristics, offset characteristics, voltage gain versus frequency, output voltage limiting, and short-circuit current limiting. The trade off for the small size of the op amp macromodel is that some less important characteristics in circuit analysis are not modeled. These include common-mode gain, thermal effects, and power supply rejection ratio.

The Q source model is a bit simpler than the RC circuit model but the latter has a faster average simulation speed especially in frequency domain analysis. The simulation results in Chapter 5 show these models are accurate enough and efficient for general large- and small-signal circuit analysis.

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