8085 MICROPROCESSOR BASED
RANDOM ACCESS MEMORY CHECKER

by

Jiinwei **Hung**

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Prof. S. J. Skarote — 3/8/86
Advisor — **Date**

Sally M. Hotchkiss — March 14, 1986
Dean of the Graduate School — Date

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ABSTRACT

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RANDOM ACCESS MEMORY CHECKER

Jiinwei Hung
Master of Science in Engineering
Youngstown State University , 1986

Three stand-alone microcomputer 8085-based memory checkers, which include (1) SRAM checker, (2) 16k*1 DRAM checker and (3) 64k*1 DRAM checker, were designed and built sucessfully with the aid of a microcomputer development system. These boards can be implemented to test additional memory chips using the design technique presented.

The software system is composed of two parts, one for the pattern test and the other for the sensitivity test. The system is able to detect hard memory errors, soft memory errors and bit-to-bit interference within a single byte and within bytes stored in memory. The analysis of typical software is discussed and the 8085 assembly testing programs are included.

ACKNOWLEDGEMENTS

I would like to express my sincere gratitude to my advisor Professor Samuel J. Skarote for his constant guidance and assistance. Thank you!

My deepest respect goes to my parents, who encouraged and supported me to come to Y.S.U.

Finally I would like to express my appreciation to those people working in the school electronic shop for their assistance.

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LIST OF SYMBOLS

SYMBOL	DEFINITION
A8-A15	Address Bus 8-15
AD0-AD7	Address & Data Bus 0-7
ATE	Automatic Testing Equipment
BJT	Bipolar Junction Transistor
CMOS	Complementary Metal Oxide Semiconductor
CPU	Central Processing Unit
DRAM	Dynamic Random Access Memory
ECC	Error Correction Code
ECL	Emitter-Coupled Logic
IC	Integrated Circuit
I^2L	Integrated Injection Logic
I/O	Input or Output
iRAM	integrated Random Access Memory
MDS	Microcomputer Development System
MOS	Metal Oxide Semiconductor
MHz	10^6 Hertz (megahertz)
mW	$10^{(-3)}$ Watt (Milliwatt)
NMOS	N Type MOS
nS	$10^{(-9)}$ Second (nanosecond)
PCB	Printed Circuit Board
RAM	Random Access Memory
ROM	Read Only Memory
SRAM	Static Random Access Memory
SSI	Small Scale Integration

TTL	**Transistor Transistor Logic**
VLS**I**	**Very Large Scale Integration**

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CHAPTER 1

INTRODUCTION

1.1 Introduction

Have you ever had a computer program which ran sucessfully for a long time only to have it suddenly fail? Or are you getting inconsistent results from the expected data? One of the reasons is probably only because one bit out of several hundred thousands erred. A computer system, whether a large computer or a microcomputer, requires a large memory to store data and program instructions. Memory does fail, thus, testing memory becomes important. With the rapid growth of the computer industry in the recent years, the use of semiconductor devices continuously grows at an increasing rate. On the other hand, quality assurance of integrated circuit is being emphasized more each day. However, there also exists the possibility of purchasing a bad memory chip. Once we have doubt about a chip, it wouldn't be too difficult for a qualified person, who is very familiar with the computer system, to find the defective memory chip if the chip is used as the read/write memory in the computer system. But for the general technician, a random access memory checker is indispensable.

1.2 Semiconductor Test

In general, the sophisticated tests applying to a

semiconductor device include three parts: DC test, AC test, and FUNCTION test.[1]

(1) DC test: Electrical DC parametric test verifies specific parameters in terms of voltage or current. This test measures the resulting voltage by applying current to the devices, or measures the resulting current by applying voltages to the devices.

(2) AC test: The AC parametric test verifies the time-related parameters specified in terms of seconds. The basic characteristic of AC parametric test is the measurement of the timing relationship at which devices operate such as rise time, fall time, propagation time, delay time, set-up time, release time and access time.

(3) FUNCTION test: This test verifies that the devices perform functionally correct, which is the best test required for the semiconductor.

1.3 Automatic Testing Equipment[1] (ATE)

ATE is a consequence of computers being interfaced with digitally-controlled stimulus and measurement instruments. ATE dramatically improves the measurement accuracy of test. It reduces the human error in testing and enhances confidence in equipment performance and failure diagnosis. It simplifies the test work and can do mass testing within a short time. ATE is divided into three

[1]F.H. Chen. "Design and Implementation for A General Purpose IC Tester Based on A Microcomputer" Chen Kung University ,1983 , p.1

classes: benchtop, dedicated and general purpose.

1. Benchtop Tester: Benchtop testers usually have limited test capability and are small in size. Normally, they are controlled by a hardware designed decoder or controller. The characteristics of a benchtop tester include its low cost and manual or fixed programs with go/no-go test that may or may not have data readout. Benchtop testers are not easy to maintain, although they are easy to use.

2. Dedicated Tester: The dedicated tester is specified for one device family such as memories. Most dedicated testers are computer controlled.

3. General Purpose Tester: The general purpose tester is a flexible configuration to accommodate almost any device type. Sophisticated computer-controlled hardware and software are also mandatory in this system. This tester tests almost everything from VLSI to SSI. The basic components of this general purpose tester include a computer controller, a stimulus and response unit, and a device-under-test interface.

Generally speaking, a general purpose tester is powerful for testing IC's, but they are normally controlled by a mainframe or a minicomputer. The price of this equipment is high and the equipment is hard to maintain.

1.4 Memory Test With The Microcomputer

The memory chip must be tested to confirm both the uniqueness of the address and the absence of the bit-to-bit interference (a bit may affect the value of another bit on

the same chip). Based on this, the most perfect test is to check 2^{16324} combinations for a 2k by 8 bit memory chip. It could take a lot of time if each possible combination were tested separately even when using a computer. A large amount of research has been done on this in order to find other testing algorithms which could shorten the testing time (Refer to chapter IV).

The rapid rise in the use of the microcomputer can be explained by the many available applications for the relatively low cost of the microcomputer hardware. This makes many applications economically feasible. Many instruments that have been controlled by a main frame or minicomputer before are now being replaced by the microcomputer where high accuracy, speed and complexity are not strictly in demand. Traditionally, memory chips are checked by a universal testing machine which costs several hundred thousand dollars. The cost prohibits a microcomputer owner from acquiring a universal testing machine. Since the microcomputer has become a powerful tool for equipment or instrumentation, it is used along with its well structured support chips (such as ROM, RAM) within the design of a small, low cost and user-friendly computerized memory tester. The cost of incorporating a 8085 microcomputer in a checker was at the time of investigation only forty dollars. Because of their simplicity, these memory testers can quickly perform a functional test on RAMs.

Chapter 2 describes the basic memory cell organization and three different types of memory. This

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Chapter 2 describes the basic memory cell organization and three different types of memory. This

CHAPTER 2

RANDOM ACCESS MEMORY OVERVIEW

2.1 What is RAM?

RAM stands for random access memory which may use MOS or BJT devices in either SRAM or DRAM. BJT devices have a better performance at high speeds than the MOS RAMs because they are manufactured using TTL, ECL, or I^2L technology. Modern MOS RAMs are manufactured using NMOS or CMOS technology. CMOS is especially useful in applications which require low power consumption. A random access memory is one in which the time required for storing (writing) and retrieving (reading) information is independent of the physical location (within the memory) of the stored data. Figure 1 shows a conceptual organization of a memory constituting W words of B bits, each requiring an address of n bits ($2^n=W$).

2.2 RAM Type

The two basic RAM types that have evolved since 1970 are the DRAM and SRAM. DRAM stands for dynamic RAM, and SRAM stands for static RAM. There is another memory called Integrated RAM or iRAM which offers the advantages of the SRAM's design simplicity and the DRAM's high packing capacity.[2]

[2]Intel Memory Component Handbook 1983, pp 1-1, 1-2

chapter gives the reader background information on the memory chip. Chapter 3 describes the failure analysis of the memory chips to help the reader have a basic understanding of memory failure. Chapter 4 contains the software testing algorithms which have been developed and the testing methods used for testing of the RAMs. Chapter 5 contains the circuitry of the RAM checkers and the procedures to extend the capability to test additional RAM chips. Chapter 6 contains the software system used in the RAM checkers, and finally, the summary of this thesis is presented in chapter 7.

2.2.1 SRAM

A static RAM device uses a flip-flop circuit for each bit. Data stored in the flip-flop circuit are retained until they are altered by writing new data in that location or when electric power is lost. More recently, considerable progress has been made in the development of the high speed, low power, high density static MCS RAM. The current state-of-the-art in commercially available static MGS RAM chip is represented by the IMS-1400 manufactured by Inmos. This is a 16k memory chip featuring 45 nS access time and a maximum power dissipation of 660 mW when in operation and 110 mW when in the standby mode.[3]

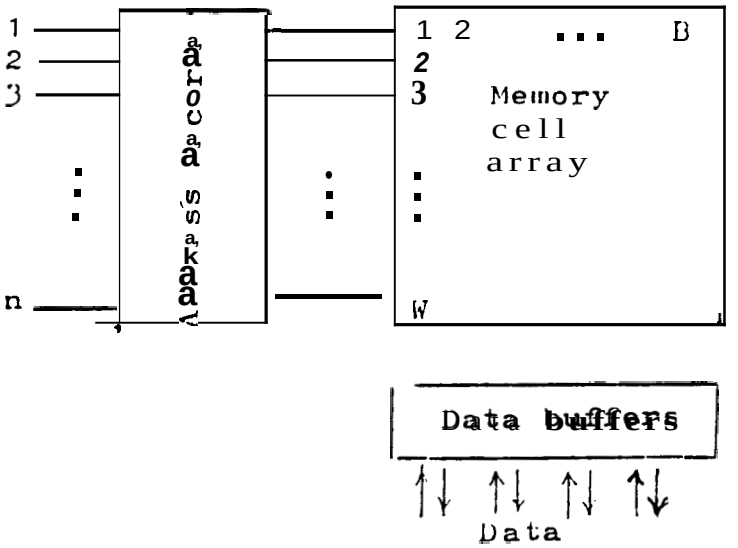


FIGURE 1. Memory Organization

[3]Sedral Smith, Micro-Electronic Circuit, Holt Rinehart and Winston, 1982, p.763

SRAM requires relatively large silicon areas because it is composed of 6-8 MOS transistors, which limits the chip size of the memory. Figure 2 shows a basic cell of the CMOS memory.

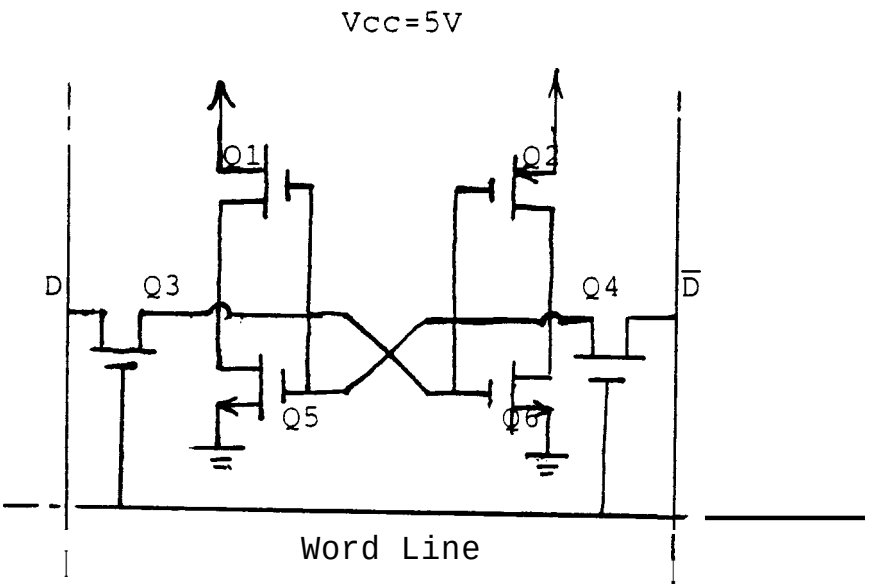


FIGURE 2. CMOS Memory Cell

2.2.2 DRAM

A major breakthrough in the development of the RAM technology was the invention of the one-transistor memory called DRAM, which is noted for its high capacity, moderate speed and low power consumption. This device uses a capacitor-like element and a driving transistor for each bit. Since the charge on the capacitor decays with time, it requires a periodic refresh signal to maintain the data storage. Traditionally, the refresh circuit is built on the

PCB on which the DRAMs are installed. The computer is prohibited from doing a read/write during the refreshing period. Figure 3 shows the structure of a DRAM cell.

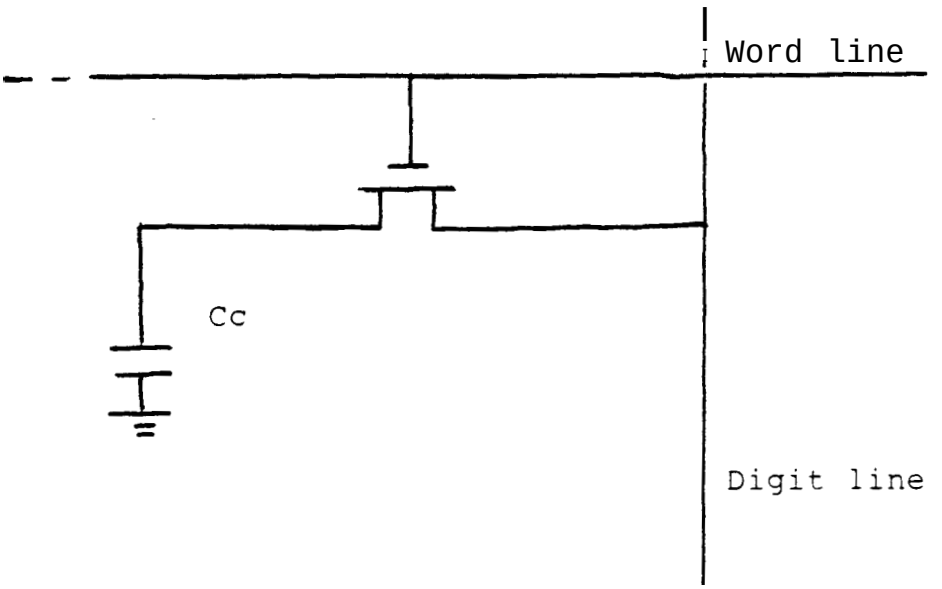


FIGURE 3. DRAM Cell

2.2.3 iRAM

Integrated RAM, which integrates a dynamic RAM and its control and refresh circuitry on one substrate, has the characteristics of a DRAM, but looks like a SRAM.

2.2.4 Comparison of DRAM and SRAM

Dynamic memories are notoriously difficult to work with because of the refresh process which may cause timing problems. Although SRAM is much easier to use than DRAM, attention must be given to the size and cost.

Before considering iRAM, SRAM is a good choice for

the designer who builds boards smaller than 8k bytes because the high price is offset by the dynamic control circuitry. Cn the other hand, for building boards larger than 64k bytes, DRAM is preferred because power consideration and package density begin to take precedence over circuit complexity.

When comparing these two types of memory, there are three major advantages of a DRAM which become apparent.

1. The density of a DRAM is much higher than the SRAM's. That is why DRAM boards contain more memory chips than the SRAM boards even with the supporting control circuitry that the DRAM board requires.

2. A dynamic RAM has less power dissipation. This reduces not only the amount of heat generated but also the current requirements for the power source. Typically, a 64k type dynamic memory board dissipates approximately 8 watts compared to 50 watts for the same size of memory of the static memory board. The decrease in power dissipation can make a big difference in the reliability of the entire system.

3. The third advantage of a DRAM is its low cost because of the high density of memory per chip.

In the comparison of these two memories, dynamic memories have slower data-access time (although they are more than fast enough for the average microprocessor). There is still one aspect that could make the SRAM a better choice. That is, not all types of direct memory access controllers will conveniently interface with all types of dynamic memory

boards.[4]

[4] **Larry Malakoff, "Dynamic Memory: Making An Intelligence Decision" Byte, Feb 1981, p.142**

CHAPTER 3

MEMORY FAILURE ANALYSIS

3.1 Introduction

Faulty memory is a very difficult problem to detect. Most distributers of memory board kits supply a simple test designed to detect some errors. These tests are ineffective in detecting a certain type of failure such as pattern sensitivity.

A number of methods are applied to calculate the reliability of a model memory system. Intel developed a chip 8206/8206-2 using ECC[5] which can correct a single bit failure and detect double bit errors. Studying memory failure analysis is fundamental to any new development in order to evolve other good algorithms and chips to prevent the memory defect or even to correct it without the user's awareness.

3.2 Error Classification.

Normally, the memory errors are classified into two categories, hard memory errors and soft memory errors.

3.2.1 Hard Memory Error

There are two types of hard memory errors, struct-at-0, struct-at-1, which are permanent errors such as shorts, open leads, micro-cracks or other instrinsic flaws. They-

[5] Intel Memory Component Handbook 1983, pp 3-164, 3-179.

are classed as single cell failures, row failures, column failures, combined row failures, half-chip failures and full chip failures. FIGURE 4' shows the failure distribution of a 2117 RAM chip.

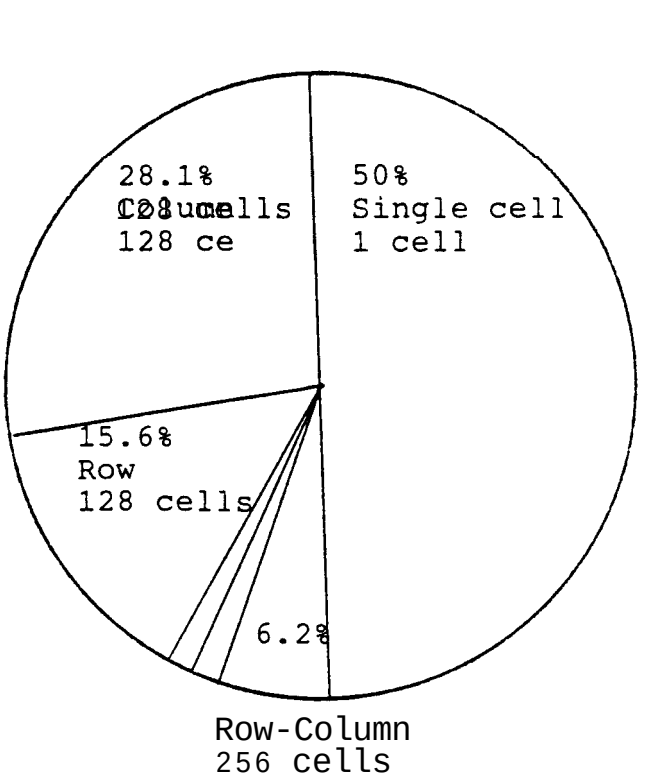


FIGURE 4. 2117 Failure Distribution

3.2.2 Soft Memory Error

A soft memory error occurs when the current state of a dynamic memory bit is changed by ionizing radiation from the plastic or ceramic integrated circuit package. In contrast to a hard memory error, a soft memory error is

[5]Ibid., pp 3-164, 3-179

characterized by being a random, non-recurring, nondestructive single cell error. A soft error can also be the result of a timing problem, or a refresh problem when using dynamic memory. Bit-to-bit interference could be caused by a soft memory error. Sometimes it is incorrect for the first time read out, but correct for the second time read out. This type of error is associated with the system level problem and the rate of failure is hard to quantify; in any event it is assumed to be very small. FIGURE 5[5] shows the combined distribution of failure types.

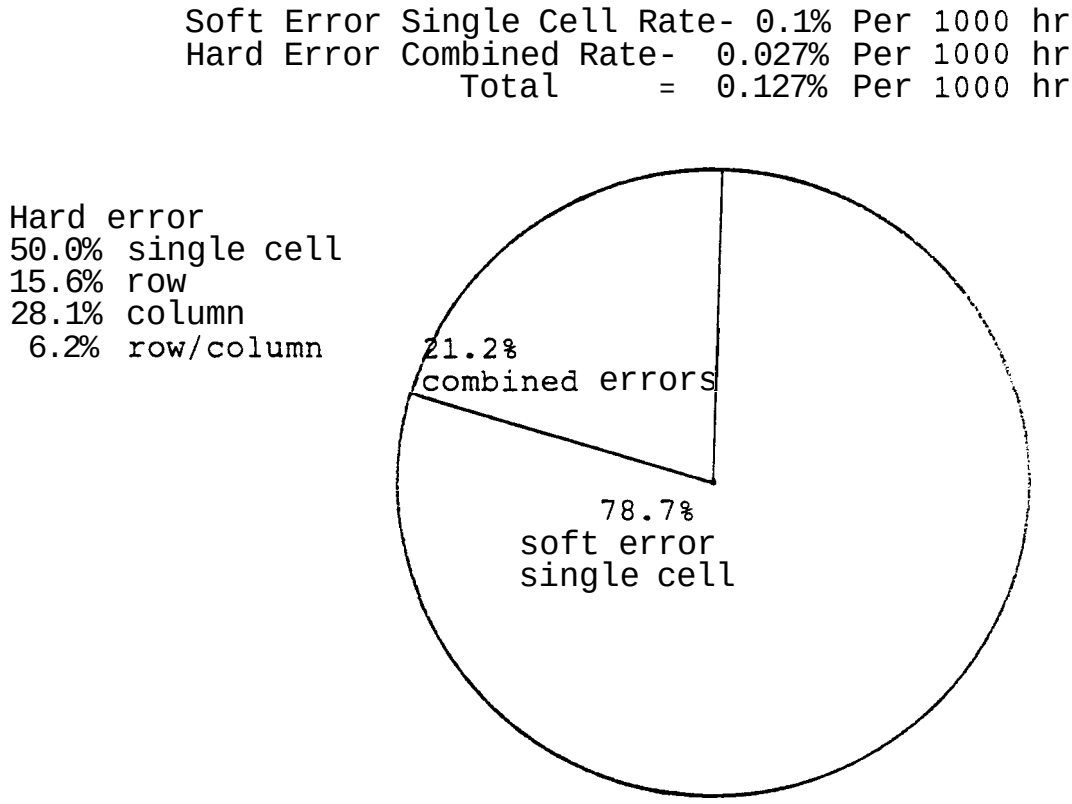


FIGURE 5. Combined Distribution of Failure Type

[5]Ibid., pp3-164, 3-179

CHAPTER 4

TESTING ALGORITHM

The few testing algorithms available today will be examined in order to determine which algorithms will be implemented in the RAM checkers.

4.1 Algorithm Research

During the algorithm research, it was found that there are six major ways to test memory chip. These algorithms will be briefly described.

4.1.1 The First Method[6]

The first method is called the walking-address memory test. Starting at an even memory address given by the user, the algorithm writes the most significant byte of the address into all of the even memory locations and then verifies the byte's content. Next the least significant byte of the address is written into all of the odd or next memory locations and then verified. Finally, the program goes back to the starting address and verifies the contents of all locations. This memory test is rapid, but it could miss hard memory errors like struck-at-0 or 1.

4.1.2 The Second Method[6]

[6] H.R. Pinnick Jr. " Testing Your Memory Using the Barber-pole Algorithm ", Byte Dec, pp 414-444

The second method stores 55H (0101 0101 in binary) into the even.locations and AAH (1010 1010 in binary) into the odd locations then checks the contents of all locations, The test is repeated with the contents of even and odd locations interchanged. This rapid test checks both hard and soft memory errors, but it has no cross-bit-check for the soft memory errors.

4.1.3 The Third Method[6]

The most extensive memory test algorithms are probably the gallop-read and gallop-write test. The gallop-read test clears memory to all zeroes in all locations and stores FFH (1111 1111 in binary) in a specified starting address. This test reads all other locations and verifies the presence of OOH except for the location which contains FFH. Next the pattern FFH is written into the next location, and the reading and verification of all locations are repeated until the end of the locations. The gallop-write test is similar with the gallop-read test except that OOH is replaced by FFH, and FFH is replaced by the OOH. These tests are excellent for testing memory except they are extremely time consuming and they have difficulty in detecting the error if one data bit affects another data bit.

4.1.4 The Fourth Method[6]

[6]Ibid. pp 414-444

The method is called the barber-pole algorithm because patterns used for the test are similar to the barber-pole (rotate by shifting 0 or by shifting 1). Refer to Table 1.

First, consider the test for a 2114 type static 1k*4 memory chip. The nine patterns of Table 1 are written into each location one at a time and then the pattern is retrieved from the location after each write to memory in order to check if it is the same as previously written. The process is repeated until the end of the memory location is reached.

TABLE 1. Testing Pattern

BINARY		HEX
0000	0000	OOH
0001	0001	11H
0010	0010	22H
0100	0100	44H
1000	1000	88H
1110	1110	EEH
1101	1101	DDH
1011	1011	BBH
0111	0111	77H

For another type of memory such as 2k*8, the test patterns will be a little different. They are 01H, 02H, 04H, 08H, 10H, 20H, 40H, 80H, FEH, FDH, FBH, F7H, EFH, DFH, BFH and 7FH.

The barber-pole testing algorithm is very good at detecting both hard memory errors and soft memory errors, except, it only finds the interaction within one byte. It is impossible to detect whether the rest of memory is affected at other locations.

4.1.5 The Fifth Method[7]

The fifth test, called the memory pattern sensitivity test, is a little different from the previous testing methods mentioned above. The program works by initializing the memorytobetested with a sequence consisting of 00H to FFH. Then pointers are set at the beginning and end of the same block of memory. Next, the data at each of the pointer location is exchanged and the pointers are then moved toward one another. The process of exchanging and moving repeats until the pointers meet. The inverted sequence is then checked for accuracy. If any discrepancies are encountered, the memory is defective.

4.1.6 The Sixth Method: Optimal RAM Test Algorithm[8]

Before stating the algorithm, the following notations are introduced. Let A_u be the memory address u.

$$0 \leq u < 2^n$$

$$\pi 0 = \{A_u / u = 0 \text{ (modulo 3)}\}$$

$$\pi 1 = \{A_u / u = 1 \text{ (modulo 3)}\}$$

$$\pi 2 = \{A_u / u = 2 \text{ (modulo 3)}\}$$

Algorithm

Step 1: Write the all 0 words, WO, at all locations.

$$A_j \in \pi 1 \quad \text{and} \quad A_k \in \pi 2$$

Step 2: Write the all 1 word, W1, at all locations.

[7] Don Kins, " A Memory Sensitivity Test ", Byte, Oct 1978, pp 12-16

[8] John Knaizuk, J.R. And C.R.P. Hartmann, " An Algorithm for Testing Random Access Memory ", IEEE Transaction on Computers, April 1977, pp 414-416.

$A_i \in \pi 0$

Step 3: Read all locations $A_j \in \pi 1$:

if output =W0; no fault indicated

$\neq$W0; RAM fault indicated

Step 4: Write all 1 word W1 at all locations.

$A_j \in \pi 1$

Step 5: Read all location $A_k \in \pi 2$:

if output=W0; no fault indicated

$\neq$W0; RAM fault indicated

Step 6: Read all location $A_i \in \pi 0$ and $A_j \in \pi 1$:

if output=W1; no fault indicated

$\neq$w0; RAM fault indicated

Step 7: Write and read the all 0 words WO at all locations

$A_i \in \pi 0$

if output=W0; no fault indicated

$\neq$W0; RAM fault indicated

Step 8: Write and then read the all 1 word W1 at all locations.

$A_k \in \pi 2$

if output=W1: no fault indicated

$\neq$W1: RAM fault indicated

end.

This algorithm presents an algorithm that optimizes in detecting any single struct-at-0 or struct-at-1 fault in a random access memory.

4.2 Algorithm Used in The RAM Checkers

Since the RAM checkers designed in this thesis are for the intensive memory testing , execution time is of minor importance. It is desirable to have a good and detailed testing program to judge the memory once there is any doubt. This type of testing algorithm will not be feasible for production testing purposes. When the time becomes important to the user, a short test option for testing DRAM boards is added to give the user a flexible choice for the testing. Refer to Table 2.

TABLE 2. Execution Time for Each Test

Long Test

RAM Type	8155	2114	4116	4164
RAM Size	.25k*8	2k*4	16K*1	64k*1
Test Time	4 sec	20 sec	120 sec	271 sec

Short Test

RAM Type	8155	2114	4116	4164
RAM Size	.25k*8	2k*4	16k*1	64k*1
Test Time	4 sec	20 sec	6 sec	13 sec

As stated before, the larger the number of -tests; the greater will be the reliability. In the RAM checkers, gallop-read, gallop-write barber-pole and sensitivity testing theories were combined together to arrive at the testing methods selected for the design of the checkers. The difference between the long and short test is that the short test doesn't include the gallop-read test and gallop-write test.

The testing program is composed of two parts, one is for the pattern test, the other is for the sensitivity test. First, the byte OOH is stored into all the memory locations, next using the barber-pole algorithm, storing the baber-pole testing patterns sequentially begining with the first memory location, the data is then verified until the end of the testing pattern is reached. Suppose a discrepancy is found in the middle of test, the program will then be aborted and go to the fail indication routine. After the last testing pattern is read, the rest of the memory locations will be checked one at a time to verify those OOH (or FFH) values which did not change (the short test doesn't include this). The process will be repeated until every memory location is checked. This completes the pattern test.

The sensitivity test is performed after the pattern test. A sequence of 256 bytes will be stored into the memory in increasing order. The number of the byte depends on the size of memory. For instance, for a 1k*4 memory chip, only 16 bytes are used and for a 16k*1 memory size, only 2 bytes are used. Next, the contents of the memory locations are interchanged. If upon checking, the sequence of the numbers is found to be in decreasing order the memory chip is good, otherwise it is a defective chip. When this method is applied to a 8155 chip (256 bytes by eight), the pass test time is about 4 seconds. For the 2114 (2k*4) chip, the pass test time takes approximately 20 seconds when the 3.579545 MHz crystal is used.

CHAPTER 5

HARDWARE DESIGN AND ANALYSIS

The memory checkers which are for testing a SRAM, a 16k*1 DRAM and a 64k*1 DRAM are based on the use of 8085 CPU. Hardware circuitry will be now studied individually.

5.1 Static Memory Checker

This checker was sucessfully designed to test memory chips of the 2114 type and the 8155 family. It can be expanded to test additional memory chips with the aid of a microcomputer design system using the following design technique.

5.1.1 Hardware of The Static Memory Checker

Figure 6 shows the photograph of this Checker, and Figure 7 shows the schematic. This checker is designed to test many different types of static memory chips.

In Figure 7, it can be seen that INTEL 8212 is used as the address latch enabled by the ALE signal. The LEDs which indicate the test results are connected to the PA 1/0 ports of the 8155. For this reason the 8155 chip could not be removed from the board even if it is not the unit under test. There is a dip switch consisting of four switches in which only one is used on the board. When the switch is at the ON position, the 2114 test is selected, otherwise the 8155 is the unit under test.

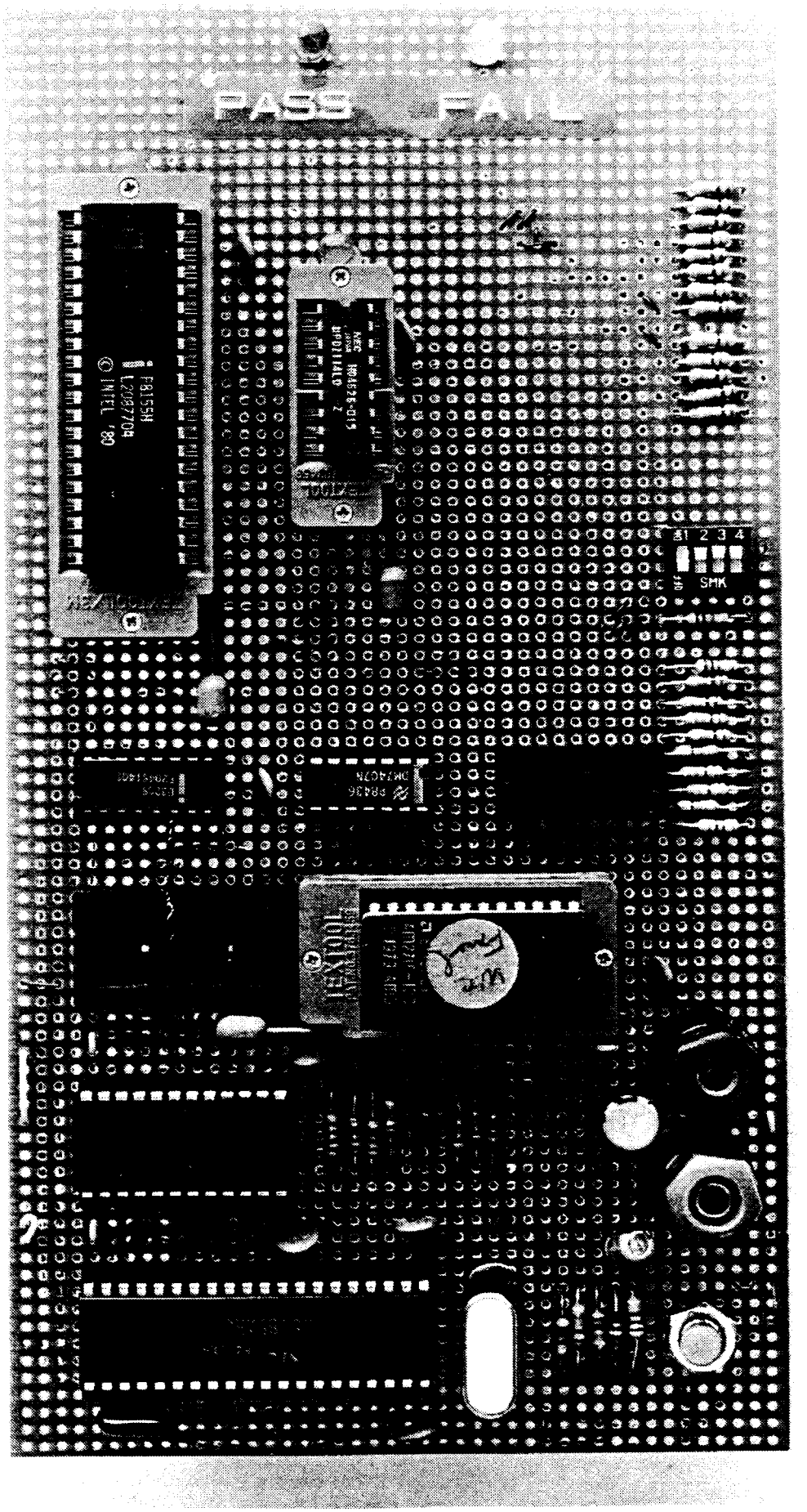


FIGURE 12. **64k** DRAM Checker

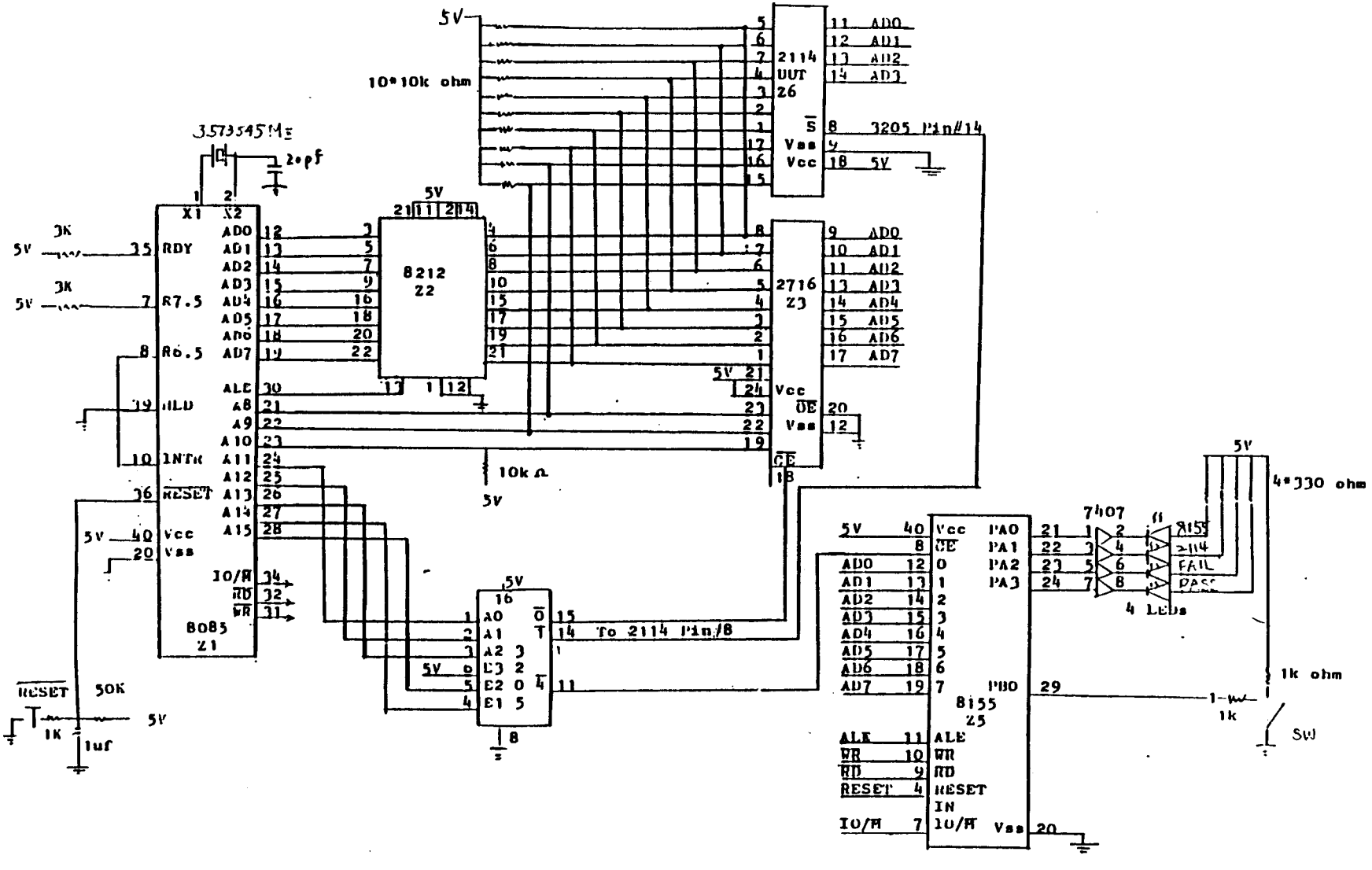


FIGURE 7. SRAM Tester Schematic

5.1.2 Testing Chips in The SRAM Checker

Table 3 lists the memory chips that can be tested using this checker in addition to the INTEL memory chip 8155.

TABLE 3. 2114 Family

VENDER	PART NUMBER
Intel	2114A/2114AL
TI	TMS 2114/TMS 2114L
AMD	9114/91L14
EA	EA2114L
EMM/SEMI	2114
Fairchild	F2114
Hitachi	HM472114A
Intel	2114A/2114AL
Intersil	IM2114/IM2114L
Mitsubishi	M5L2114L
Motorola	MCM2114/MCM21L14
National SC	MM2114/MM2114L
NEC	upD2114/upD2114L
OKI	MSM2114/MSM2114L
Synertek	SY2114/SY2114L

5.1.3 Future Expansion

This testing board is a model for the SRAM checker. Future expansions can be implemented by using the following hardware design procedures:

1. Connected the chip select ($\overline{CS}$) line with the output of 3205. Refer to Figure 8.

The address of each output of decorder 3205 is listed in Table 4.

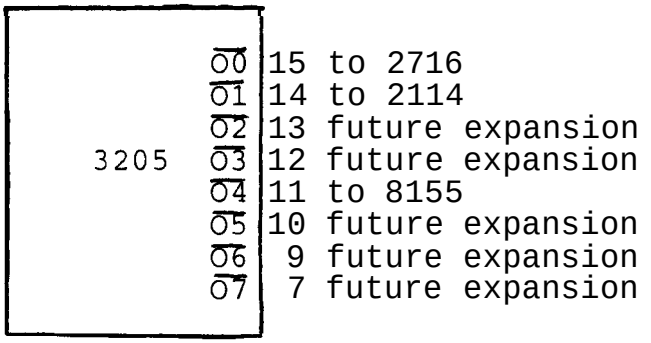


FIGURE 8. 3205 Output Analysis

TABLE 4. 3205 Address Assignment

OUTPUT	PIN NUMBER	ADDRESS
$\overline{O0}$	15	0000H-1FFFH
$\overline{O1}$	14	2000H-3FFFH
$\overline{O2}$	13	4000H-5FFFH
$\overline{O3}$	12	6000H-7FFFH
$\overline{O4}$	11	8000H-9FFFH
$\overline{O5}$	10	A000H-BFFFH
$\overline{O6}$	9	C000H-DFFFH
$\overline{O7}$	7	E000H-FFFFH

2. Connect the data and address lines to AD0 through AD7, and A8 through A15.

The 8085 microprocessor can run at maximum speed of 3 MHz.[9] In order for it to work with most of the-memory chips, approximately half of the maximum speed is considered as the best choice. For this board 3.57945/2 MHz is chosen. If the memory can not be matched with the existing board, it is suggested that the board be interfaced to the MDS, which can implement the additional control circuitry.

[9] Mcs-80/85 TM Family User Manual, Oct 1979, p6-4

5.2 16k DRAM Checker

Two test methods are used on the DRAM checkers. The user can choose a long or a short test by setting the connected dip switch on the testing board to either the ON or OFF position.

5.2.1 Hardware Description

This board is designed as a 16k RAM checker. Figure 9 shows the photograph, and Figure 10 shows the schematic of this checker.

On this board, the 8755 serves as program memory storage and as 1/0 for the system. In order to have the expected data come from the memory under test, a data latch LS373 is necessary, the $\overline{\text{XACK}}$ signal (TRANSFER ACKNOWLEDGE pin #29 of the the 8203) serves as the strobe in this case, and the LS373 is disabled when the 8755 is in the enabled state.

The INTEL 8203 is a dynamic RAM controller designed to provide all necessary signals when using the 2164, 2118, and 2117 DRAM in a microcomputer system. The 8203 provides multiplexed addresses, an address strobe, refresh logic, and refresh/access arbitration.10

[10] Intel Component Handbook pp 3-285, 3-302.

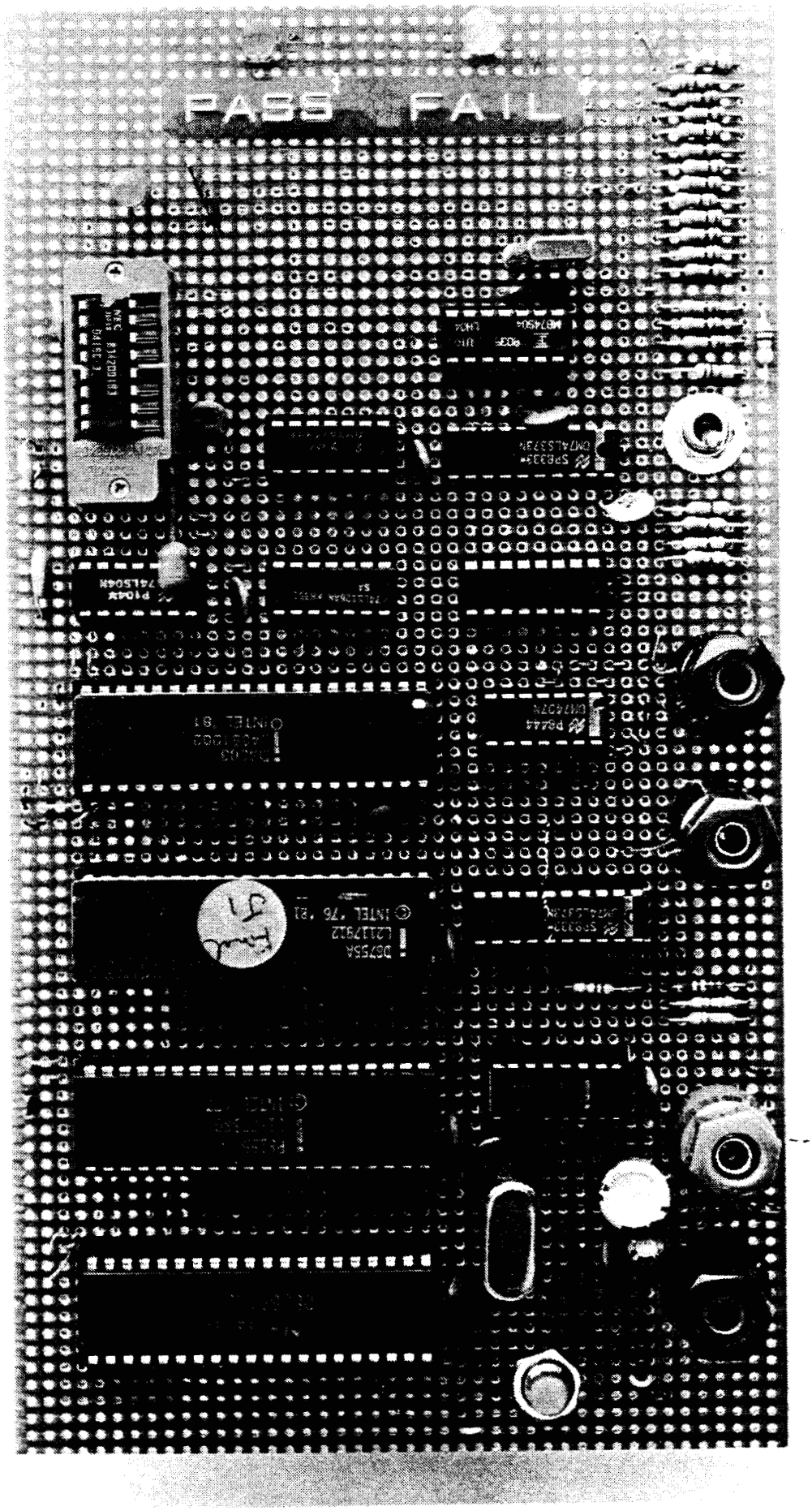


FIGURE 9. 16k **DRAM** Checker

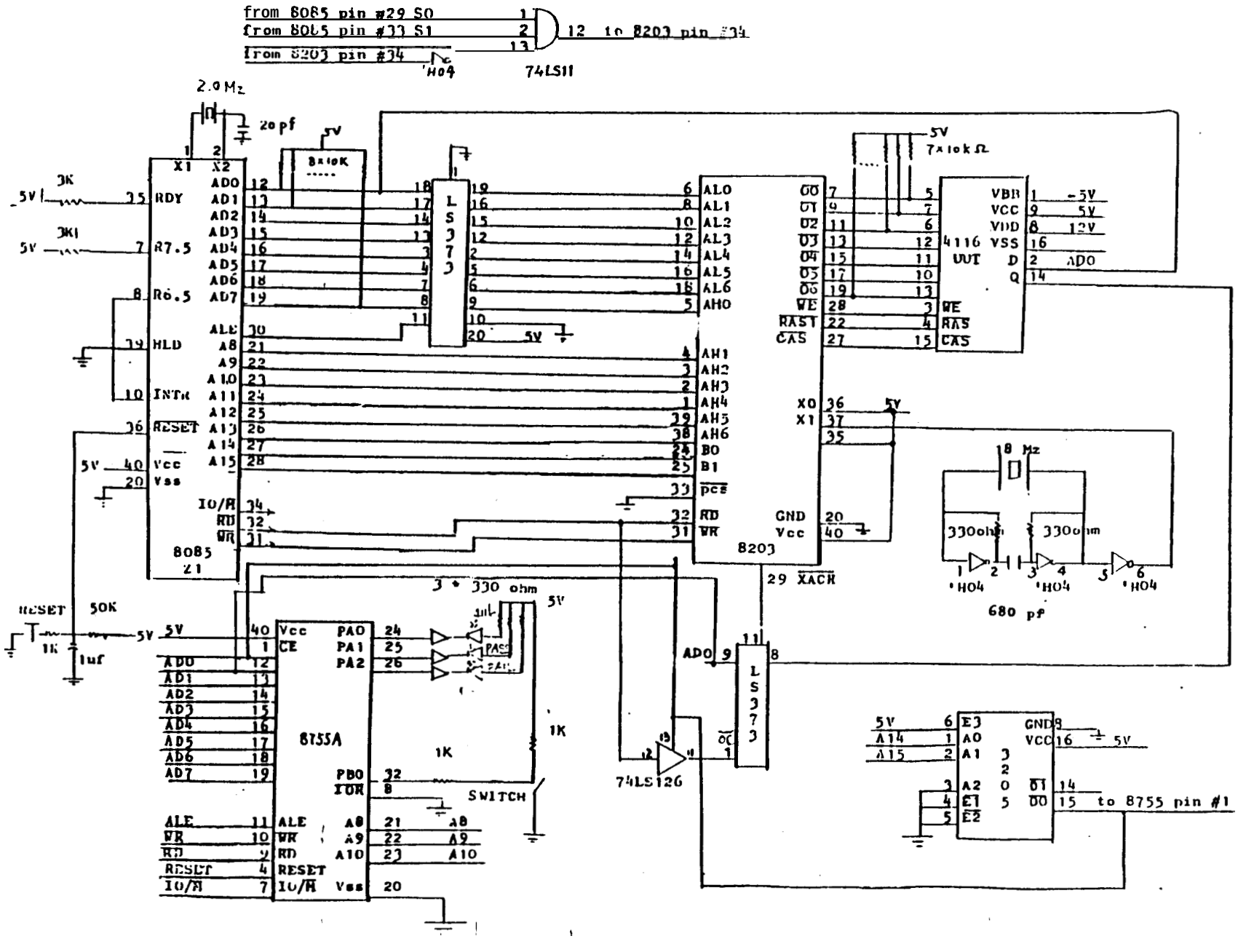


FIGURE 10. 16k DRAM Tester Schematic

5.2.2 Testing Chips in The 16k DRAM Checker

Table 5 lists the 16k DRAM chips that can be tested using this checker.

TABLE 5. 4116 Family

VENDER	PART NUMBER
TI	TMS 4116
AMD	AM9026
Fairchild	F4116
Fujitsu	MB8116
Hitachi	HM4716
Intel	2117
Intersil	IM4116
ITT	ITT4116
Mitsubitsu	M5k4116
Mostek	MK4116
Motorola	MCM4116
National	MM5290
NEC	upD416
GKI	MSM3716
Toshiba	TMM416

5.2.3 Future Expansion

Future hardware expansion is made possible by the following procedures in addition to the data and address lines being connected to the CPU (AD0-AD7 and A8-A15).

1. Connect the $\overline{RAS}$ of the new memory chip to the $\overline{RAS}$ signal coming from the 8203, refer to Table 6.

TABLE 6. 8203 Bank Selection

INPUTS		CUTPUTS			
B1	B0	$\overline{RAS0}$	$\overline{RAS1}$	$\overline{RAS2}$	$\overline{RAS3}$
0	0	0	1	1	1
0	1	1	0	1	1
1	0	1	1	0	1
1	1	1	1	1	0

The addresses assigned to the $\overline{RAS}$ signal are shown in

Table 7.

TABLE 7.
8203 Active RAS Address Assignment

Active $\overline{RAS}$	Assigned Address
$\overline{RAS0}$	0000H-3FFFH
$\overline{RAS1}$	4000H-7FFFH
$\overline{RAS2}$	8000H-BFFFH
$\overline{RAS3}$	C000H-FFFFH

Locations 0 to 3FFFH are being used by the ROM and 4000H to 7FFFH by the 4116.

2. In the case $\overline{RAS2}$ is used, $\overline{O2}$ coming from the 3025 should be connected as shown in Figure 11 in order to disable the data latch when the memory chip addresses are not activated.

5.3 64k DRAM Checker

This DRAM testing board is very similar to the 16k DRAM testing boards except that this board has to test 64k locations. The 8085 is capable of addressing 64k locations.

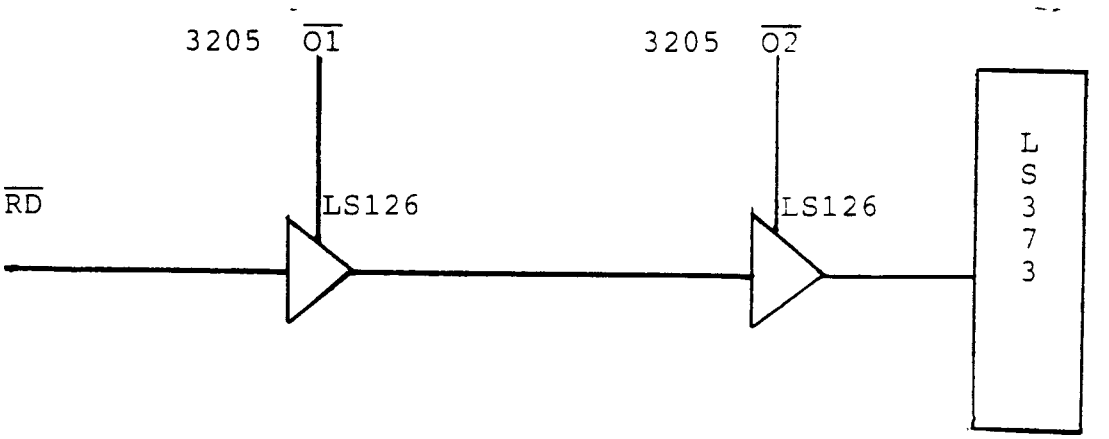


FIGURE 11. Data Latch Method

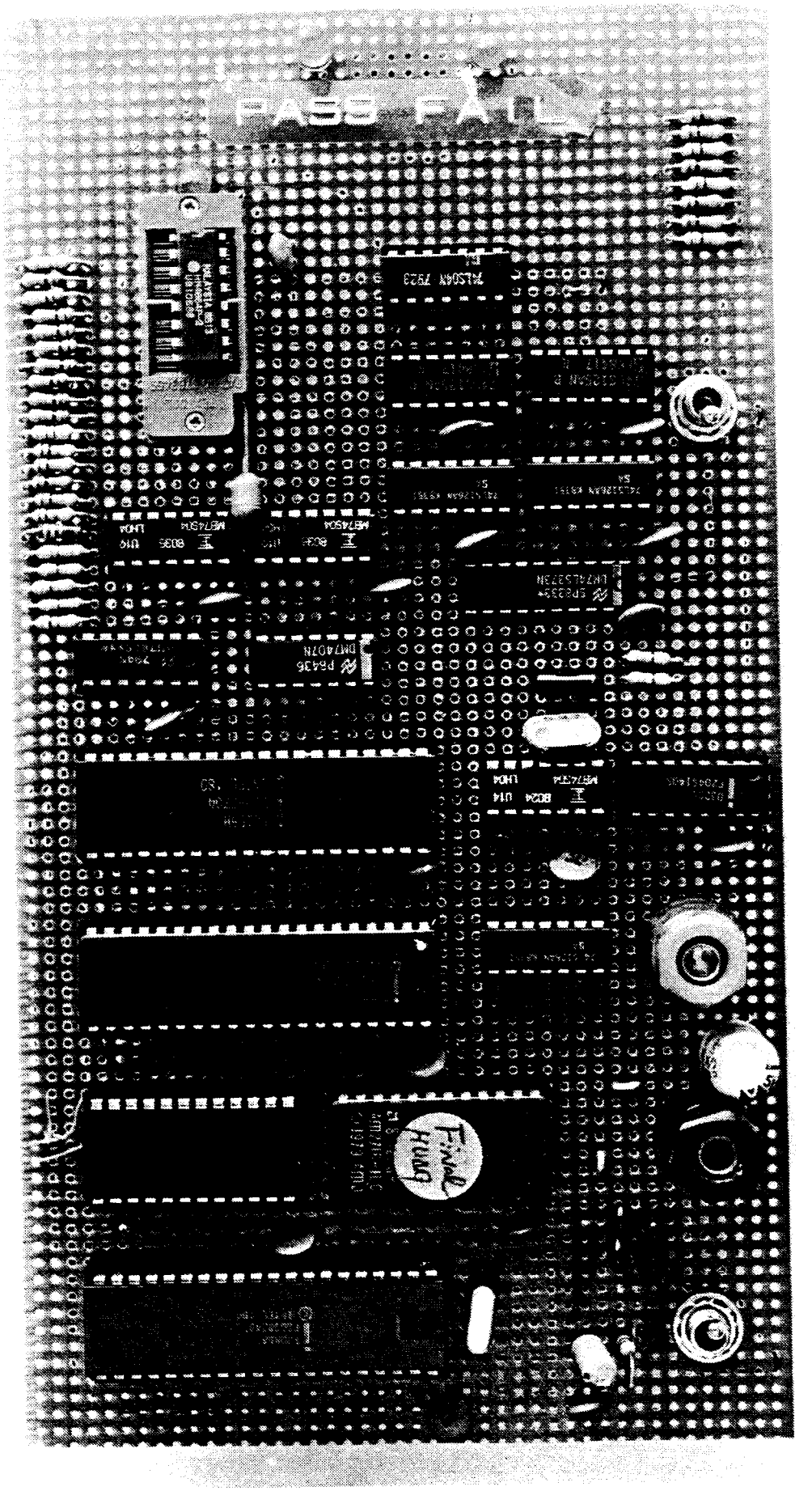


FIGURE 12. **64k** DRAM Checker

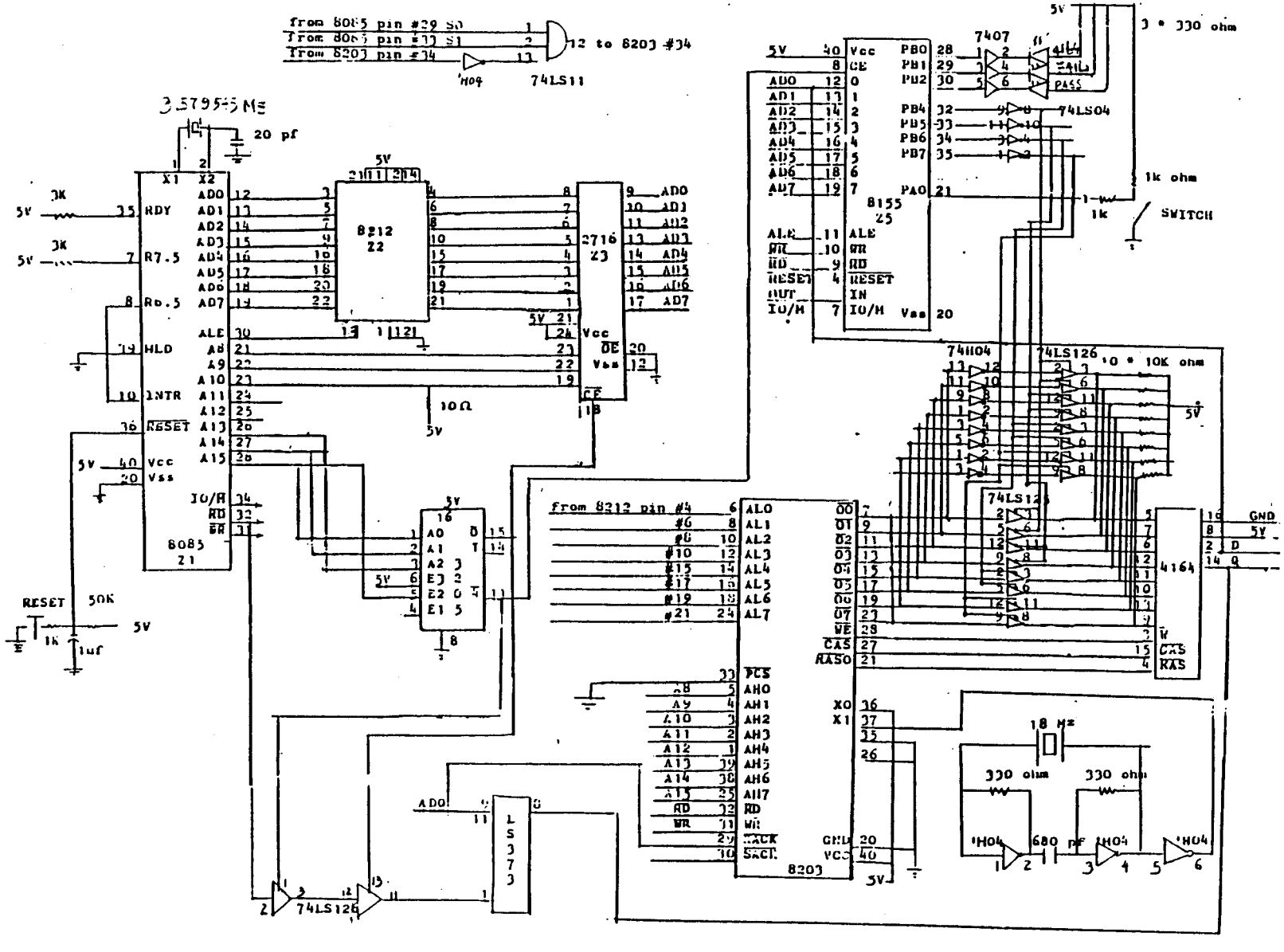


FIGURE 13. 64k DRAM Tester Schematic

5.3.1 Hardware Analysis

This board is designed to test a 64k RAM. Refer to Figure 12 and Figure 13 for the photograph and schematic.

In addition to being similar in structure with the previous two boards discussed, this bcard requires virtual memory in order to test 64k locations when the 8085 is used as the microprocessor. The main feature of this board is that it uses the overlap method to satisfy the requirements of testing the 64k DRAM. Figure 14 shows the hardware structure of this overlap method.

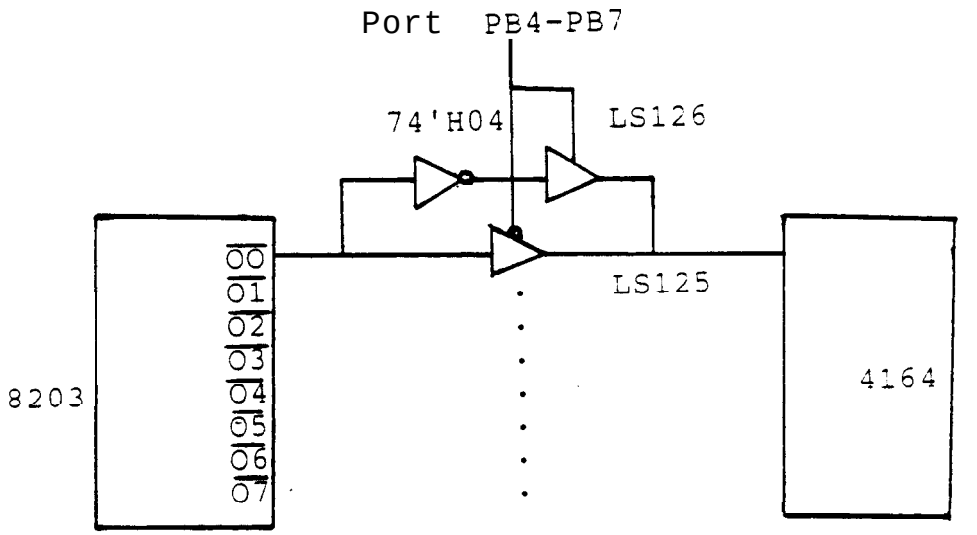


FIGURE 14. Cverlap Structure

When the ports PB4 to PB7 are asserted high, the LS125 goes to the high impedence state. $\overline{00}$-$\overline{C7}$ coming from the 8203 will be connected to the 4164 through the inverters. For this case, the locations 8000H-FFFFH addressed by the processor will be mapped to the locations 7FFFH-0000H within the memory chip. On the other hand, when a Low is asserted on the port PB4 to PB7, the LS126 goes to high impedence state and 8000H-FFFFH addressed by the processor is equal to 8000H-FFFFH within the 4164.

Combining these two cases, 0-FFFFH locations in the memory chip will be checked by setting the output port PB4-PB7 High and then Low.

5.3.2 Testing Chips in The 64k DRAM Checker

Table 8 lists the 4164 family that can be tested using this checker.

Refer to TABLE 8.

TABLE 8. 4164 Family

VENDER	PART NUMBER
TI	TMS4164
Fairchild	F64k
Fujitsu	MB8264
Hitachi	HM4864
Intel	2164
Mitsubishi	M5k4164s
Mostek	Mk4164
Motorola	MCM666
National	NMC4164
NEC	upD4164
GKI	MSM3764
Toshiba	TMM4164

5.3.3 Future Expansion

Future expansion can be obtained by sharing all of the signal lines with the 4164 except for the data line **AD0** used by the 4164. The rest of the data lines AD1–AD7 are available to be used as any data signal. Of course, the software must be modified to support this change.

CHAPTER 6

SGFTWARE DESIGN

This chapter is concerned about the testing software of the three testers. Since the 8085 CPU is used, 8085 machine codes are employed in the checker software design. Each of the three programs contains two parts. The first part is called the pattern test routine. It checks the uniqueness of each byte and makes sure that every single bit is valid. After each location is checked, the gallop-read test is applied to the rest of the memory within this block (256 bytes is defined as a block). In this case, most of the interference between bytes will be detected. The second part of the program is the sensitivity test routine which is very useful in detecting the interference between bytes. For the case of the 8155, OOH - FFH is written into consecutive memory locations. Then the contents of the memory are reversed. If the sequence of FFH, FEH, ... 02H, 01H, OOH is not read from the 8155 memory locations, an error is detected and this memory chip is defective. During the search for defective memory chips in the school's electronic shop, one **4164** chip was found which passed the pattern test but failed the sensitivity test.

6.1 Testing Program for The Static RAM Checker

This program is illustrated in Figure 15, and the complete assembly language program is contained in the Appendix A.

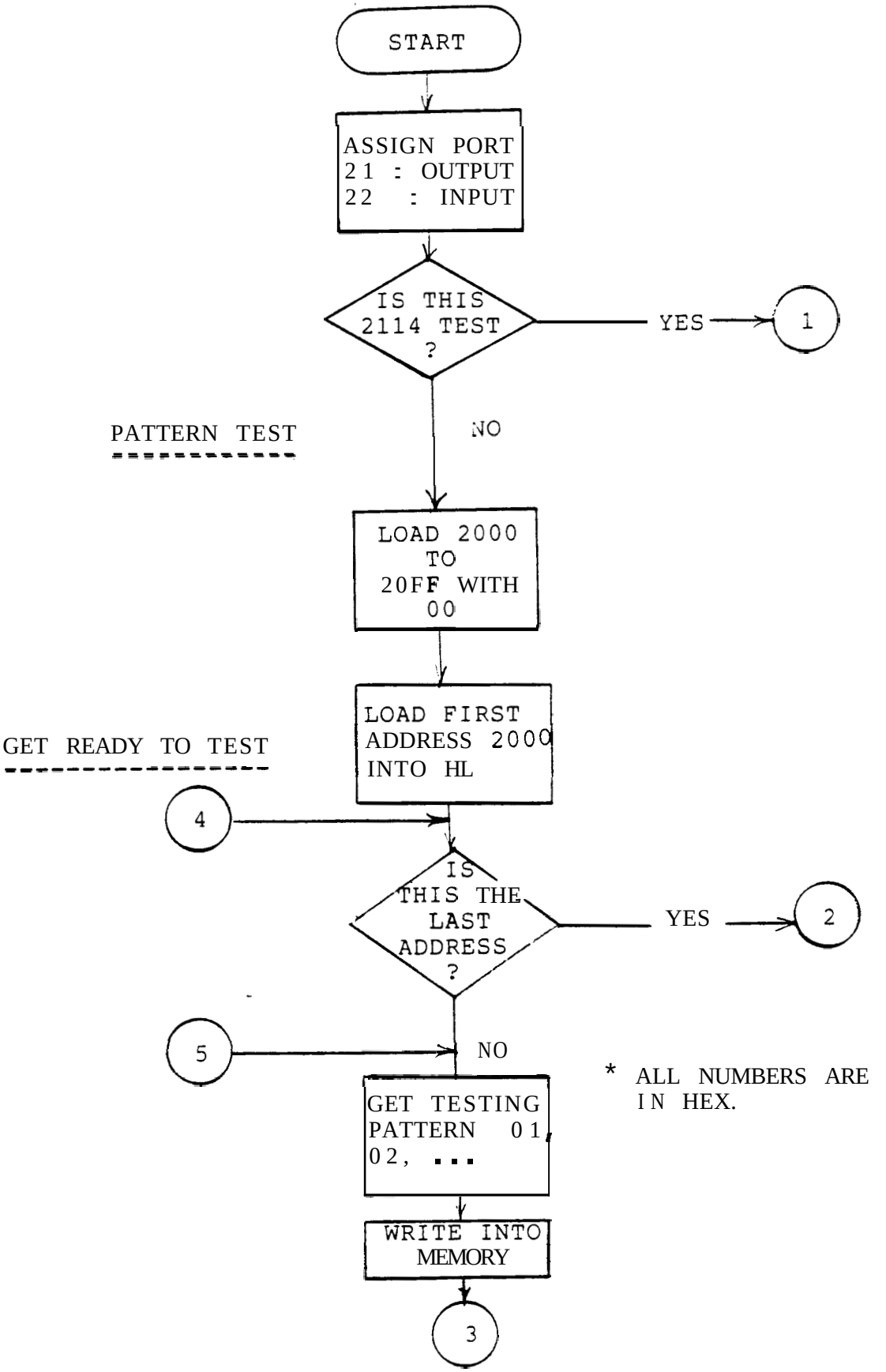


FIGURE 15. SRAM Testing Program Flowchart (continued)

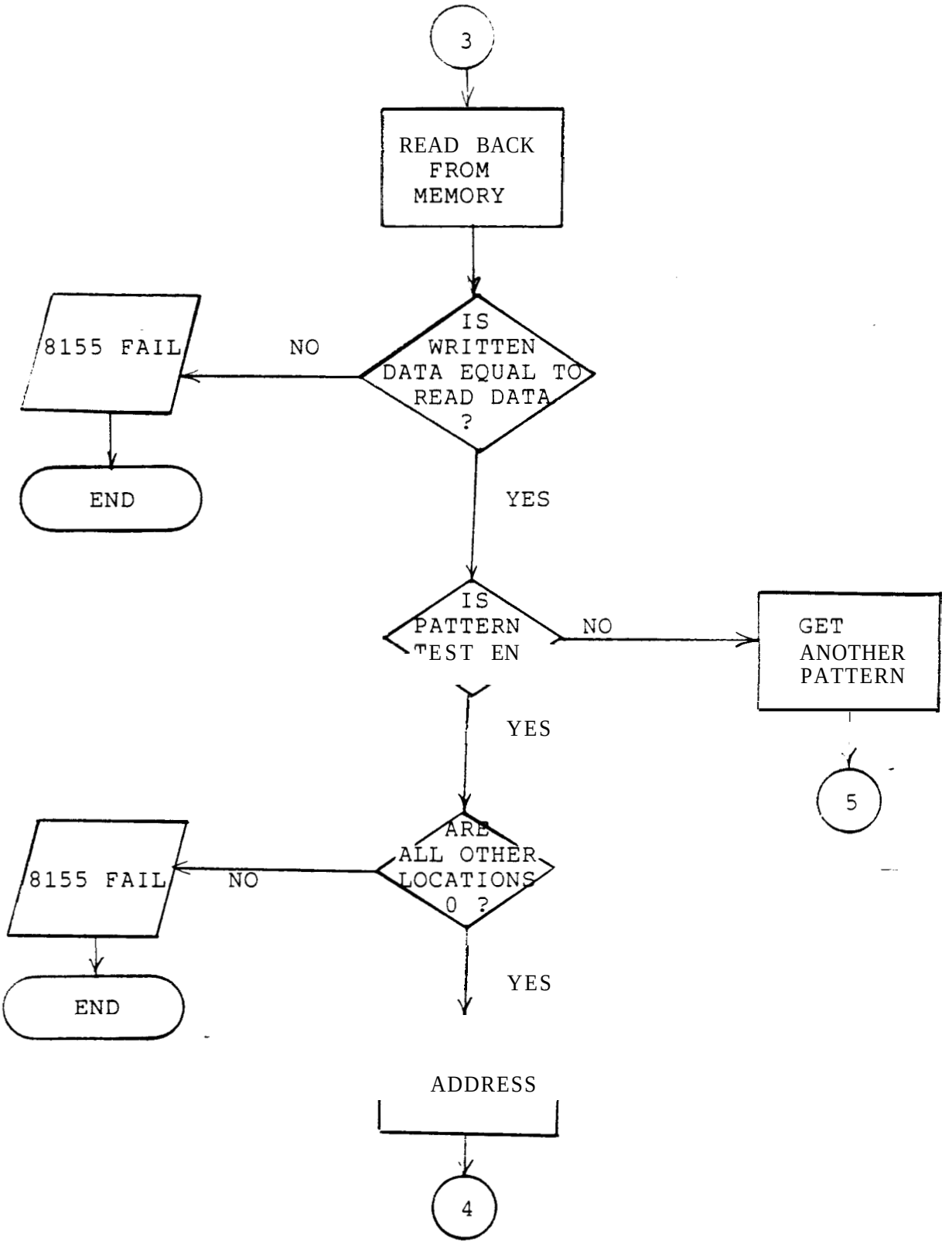


FIGURE 15. SRAM Testing Program Flowchart (continued)

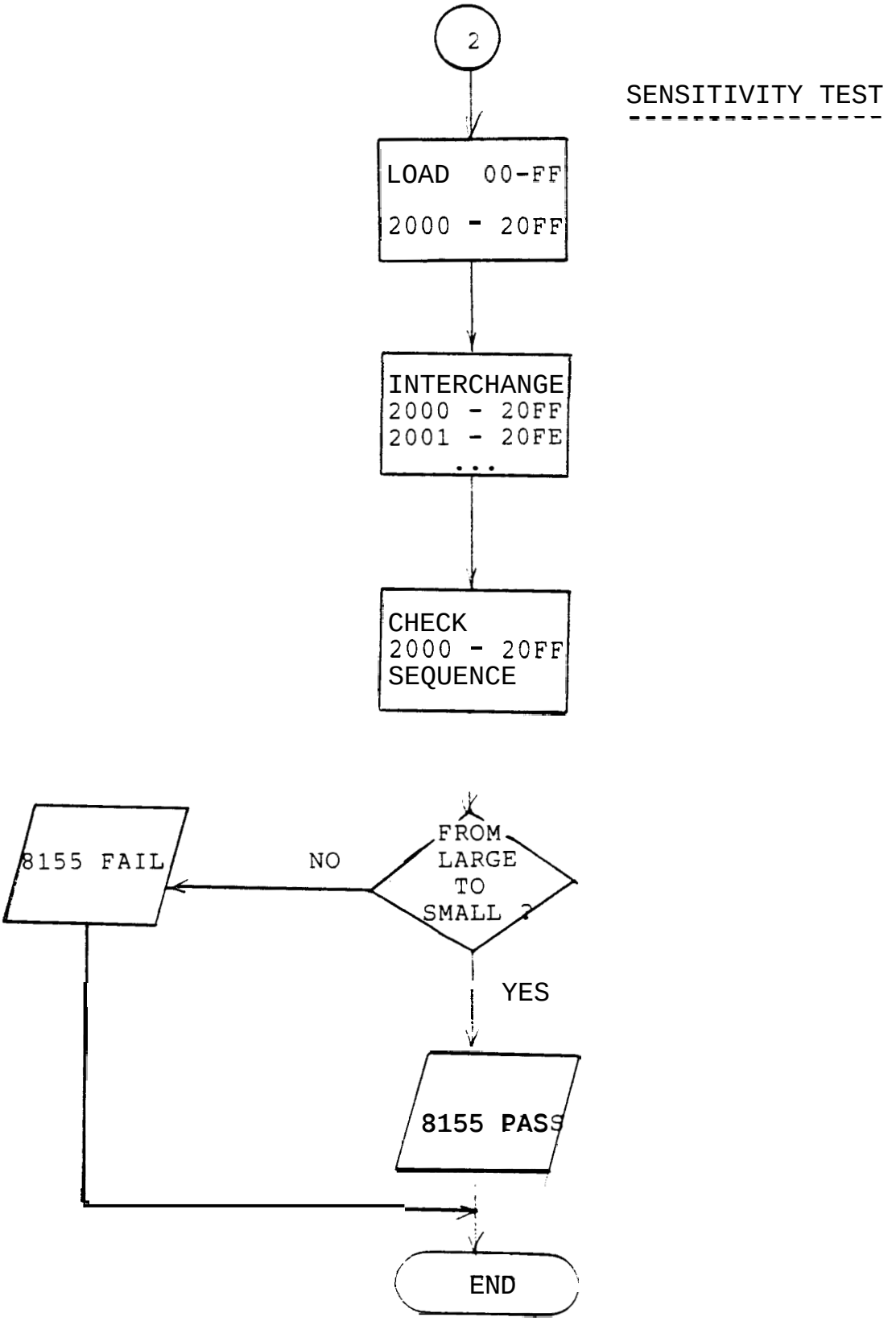


FIGURE 15. SRAM Testing Program Flowchart (continued)

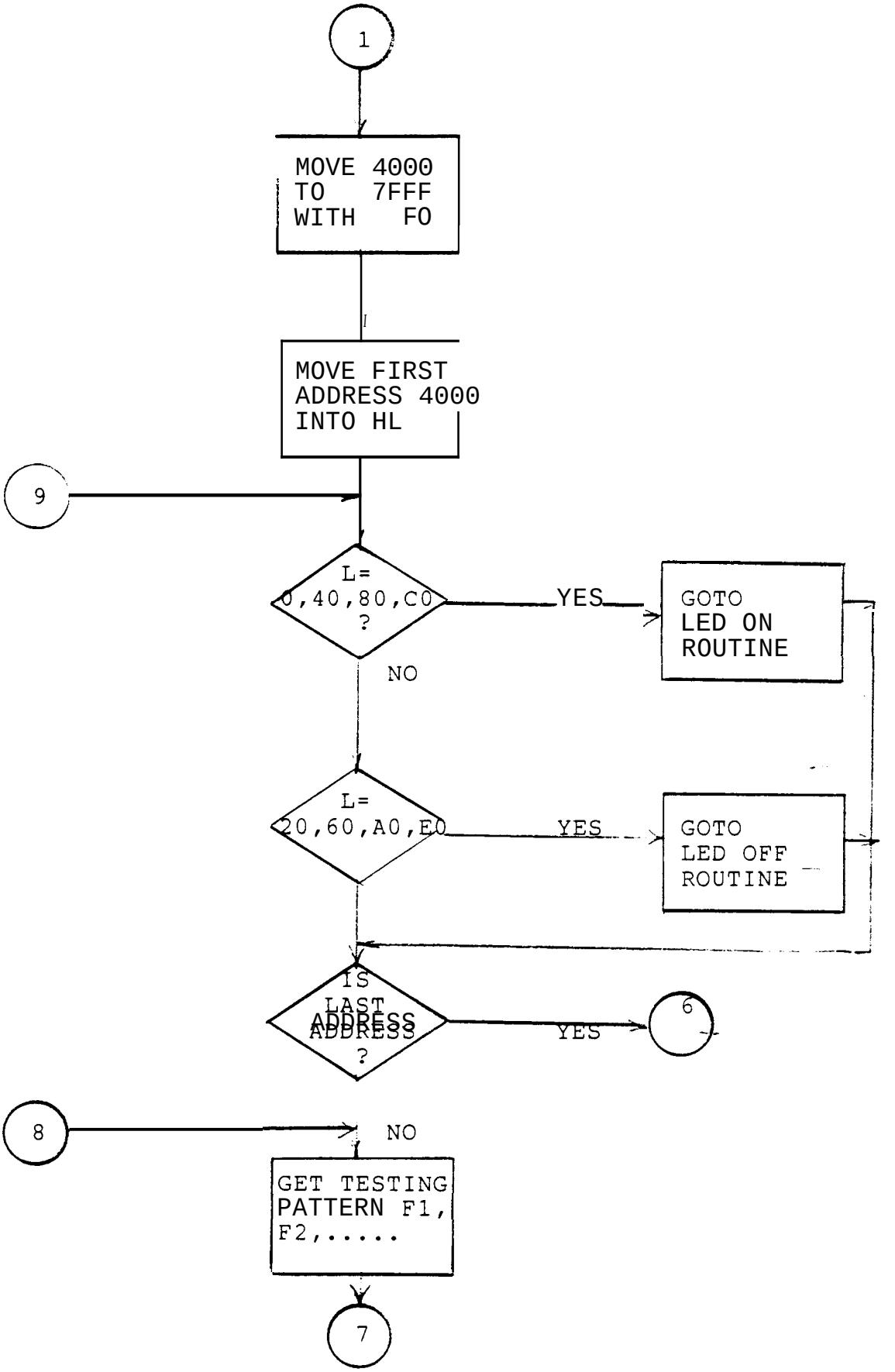


FIGURE 15. SRAM Testing Program Flowchart (continued)

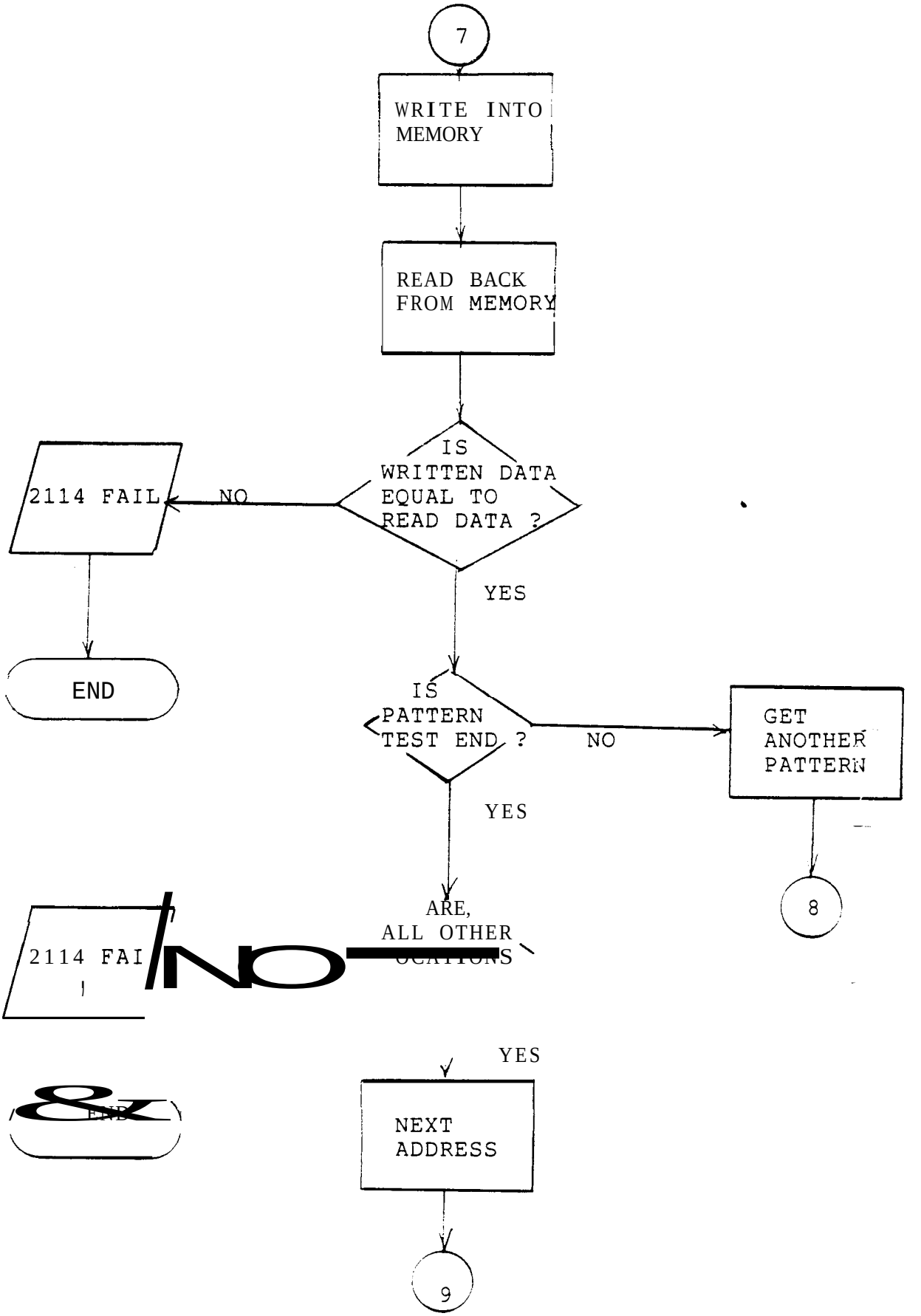


FIGURE 15. SRAM Testing Program Flowchart (continued)

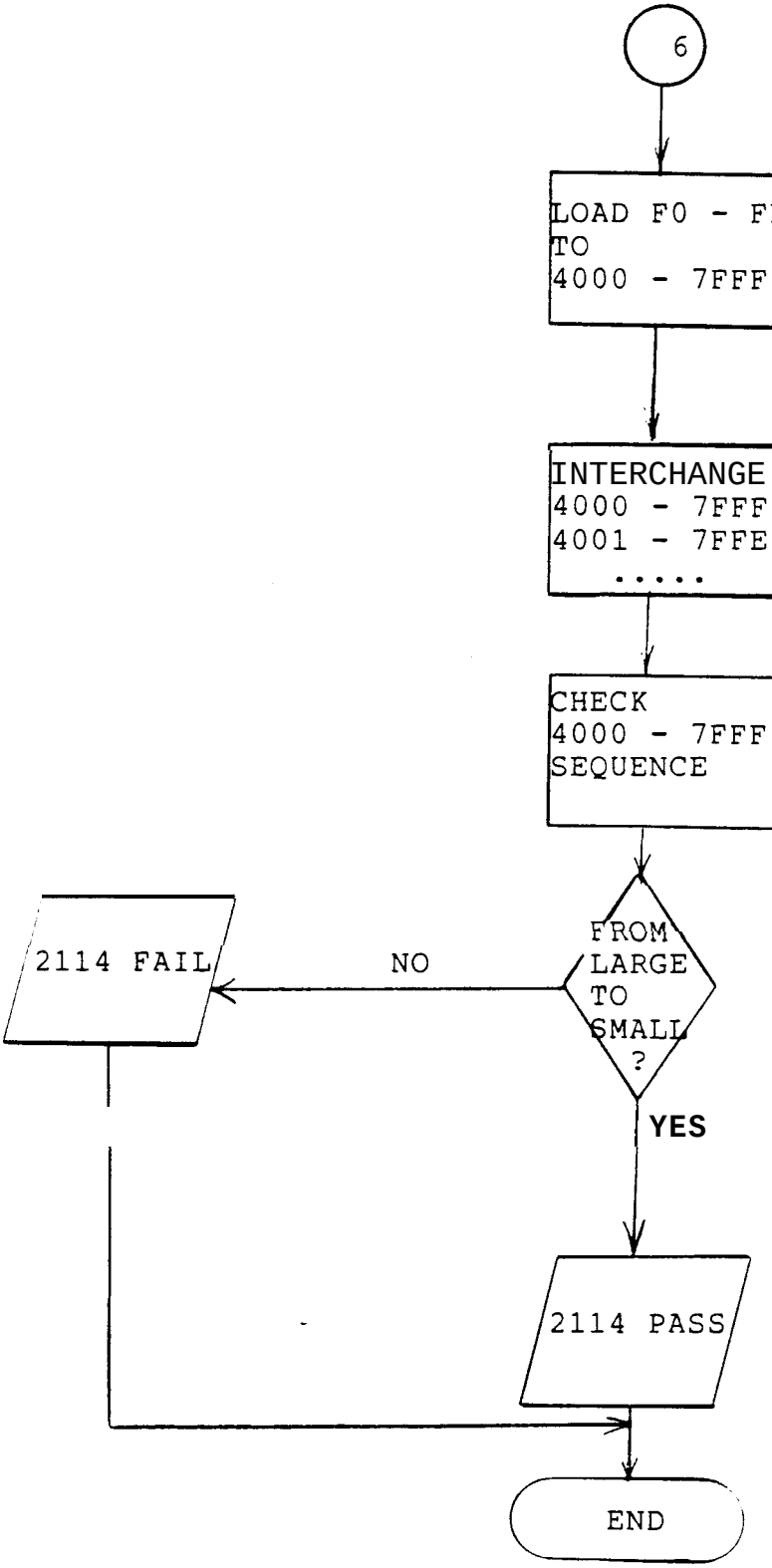


FIGURE 15. SRAM Testing Program Flowchart

6.2 Testing Program for The 16k DRAM Checker

This testing program is similar with the SRAM testing program except that it only has one data line. The testing flowchart is shown in Figure 16 and the assembly language program is contained in Appendix B.

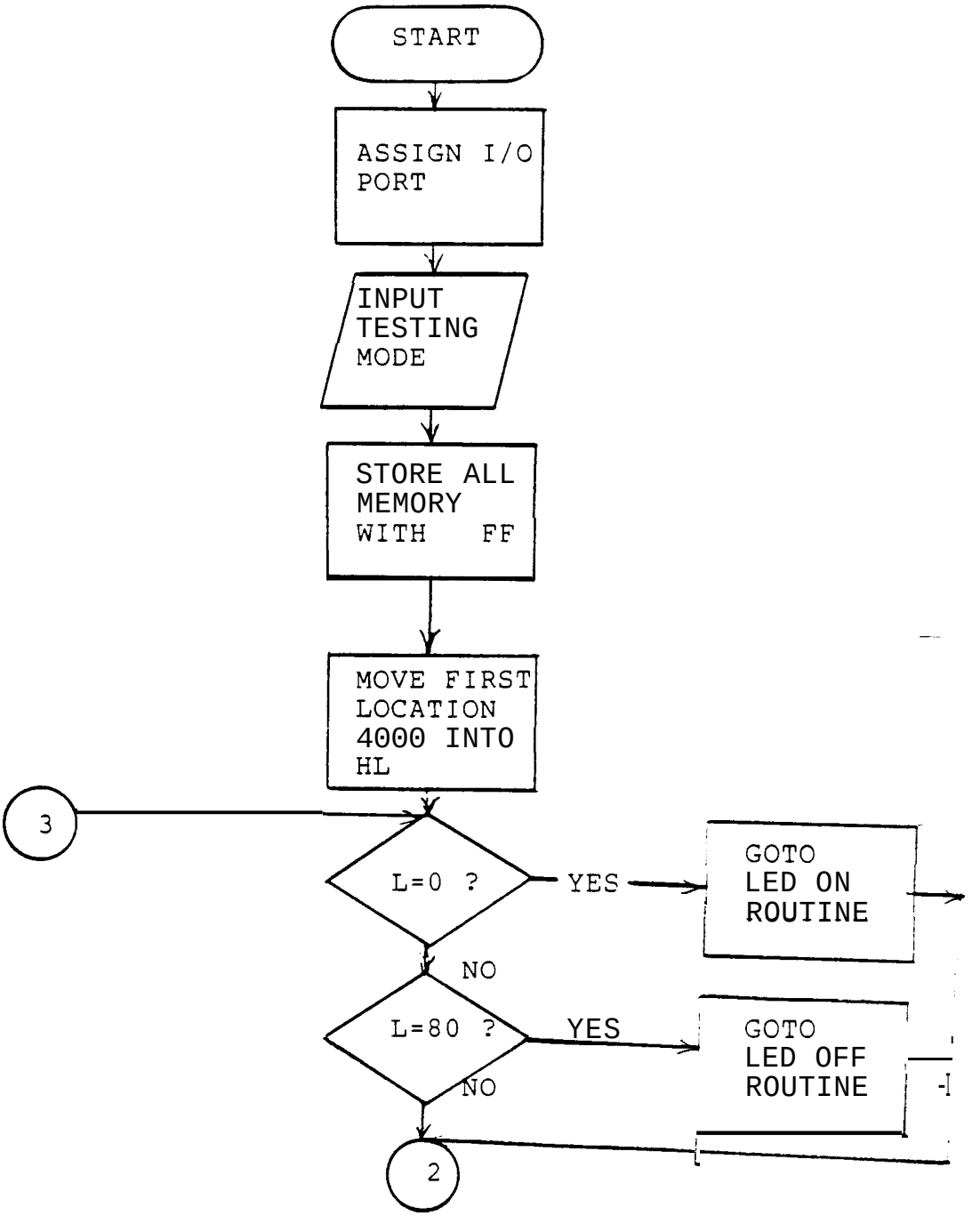


FIGURE 16. 16k DRAM Testing Program Flowchart (continued)

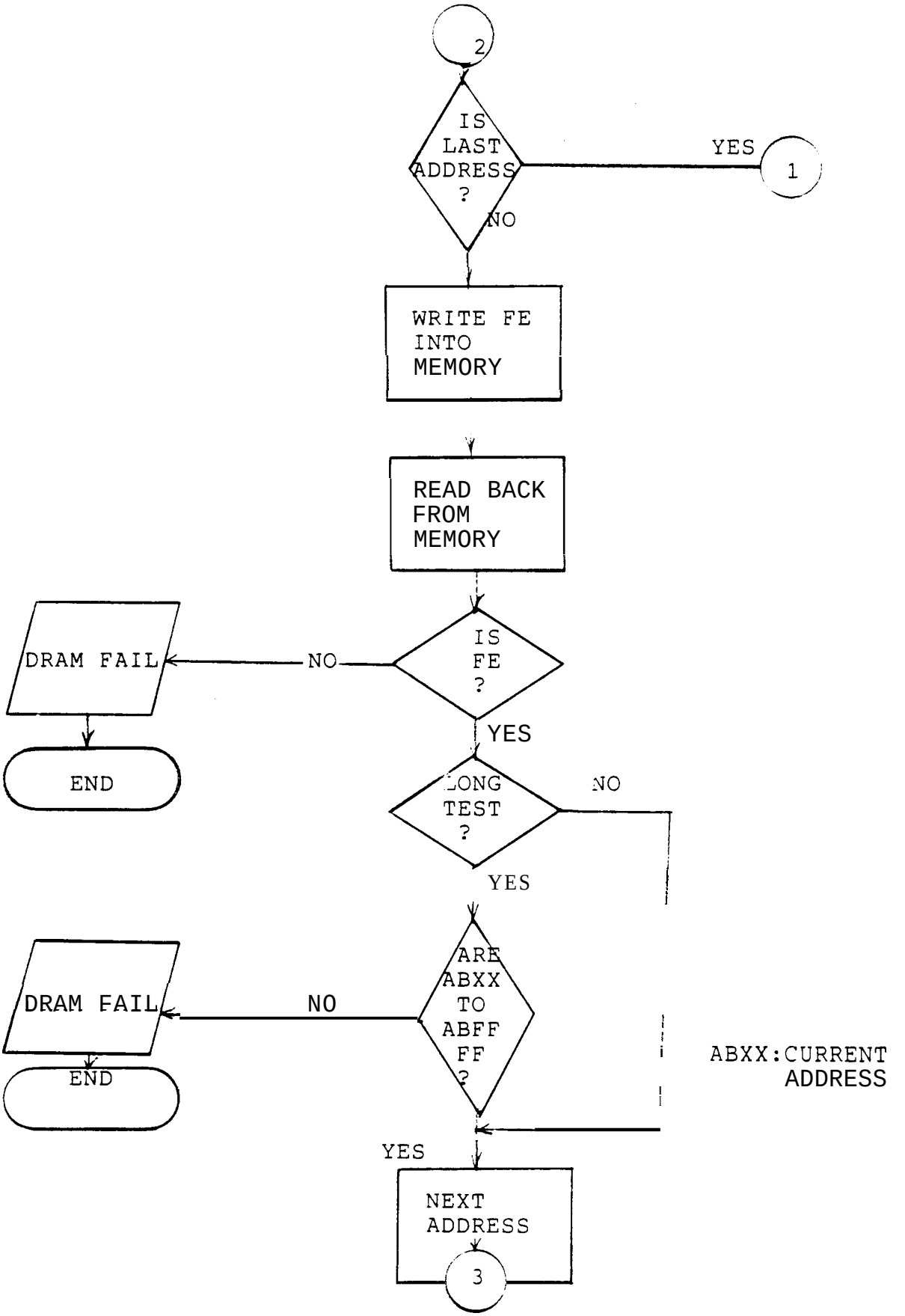


FIGURE 16. 16k DRAM Testing Program Flowchart (continued)

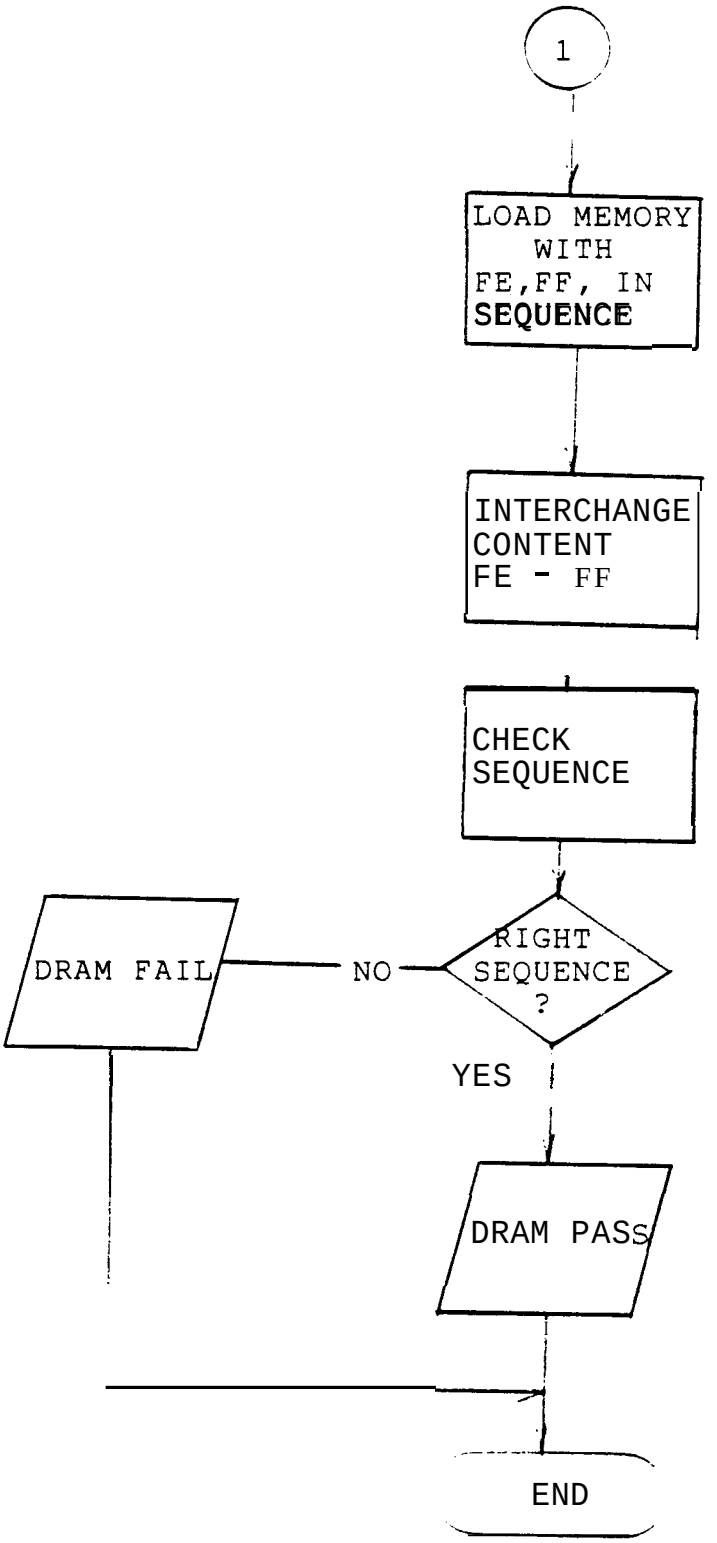


FIGURE 16. 16K DRAM Testing Program Flowchart

6.3 Testing Program for The 64k DRAM Checker

The two testing programs for the 16k DRAM and the 64k DRAM are very similar because both of them have one data line excluding the 64k DRAM which has two sets of locations 8000H-FFFFH addressed by the **8085**. The program flowchart is shown in Figure 17, and the complete assembly language program is contained in the Appendix C.

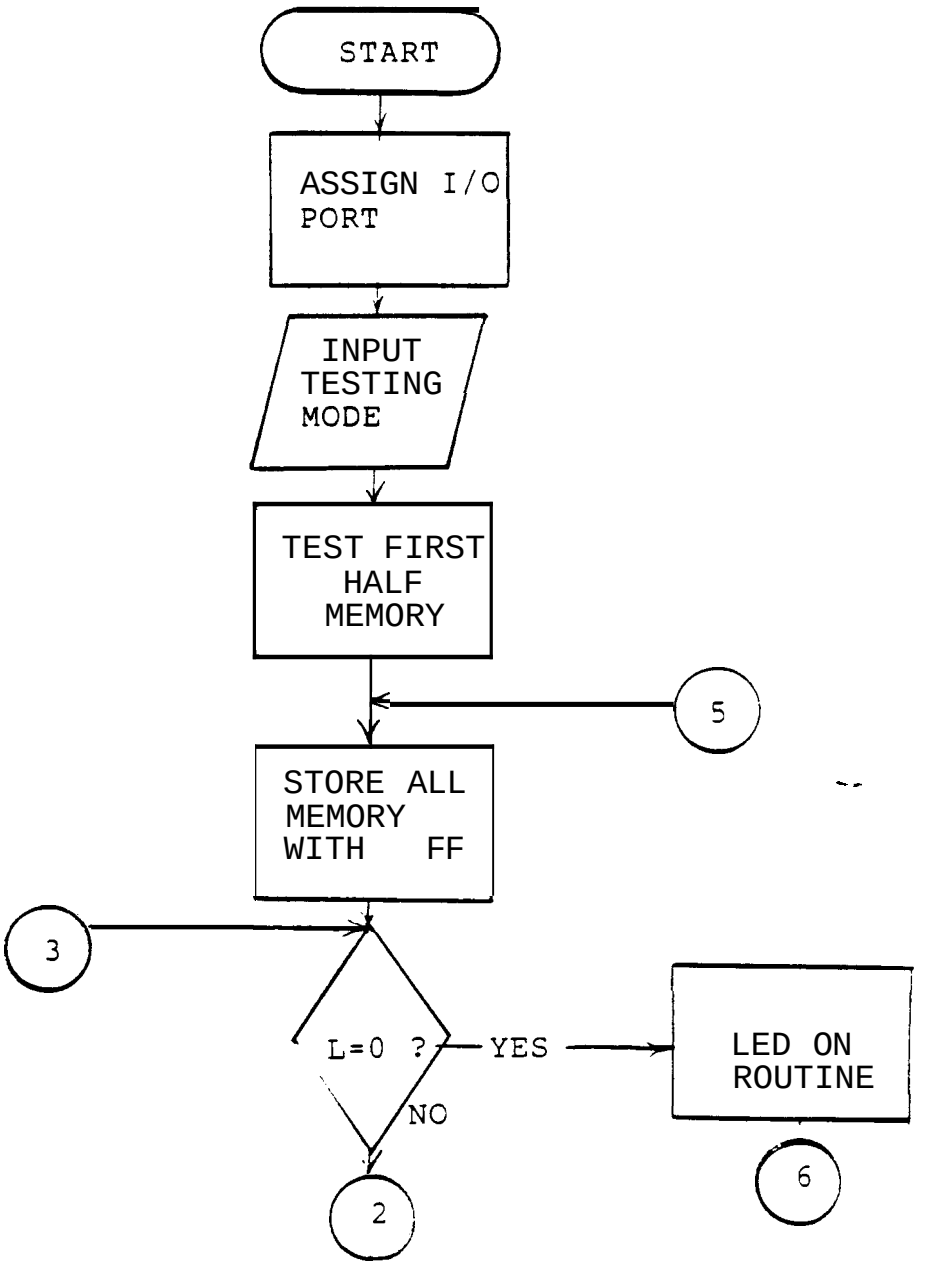


FIGURE 17. 64k DRAM Testing Program Flowchart (continued)

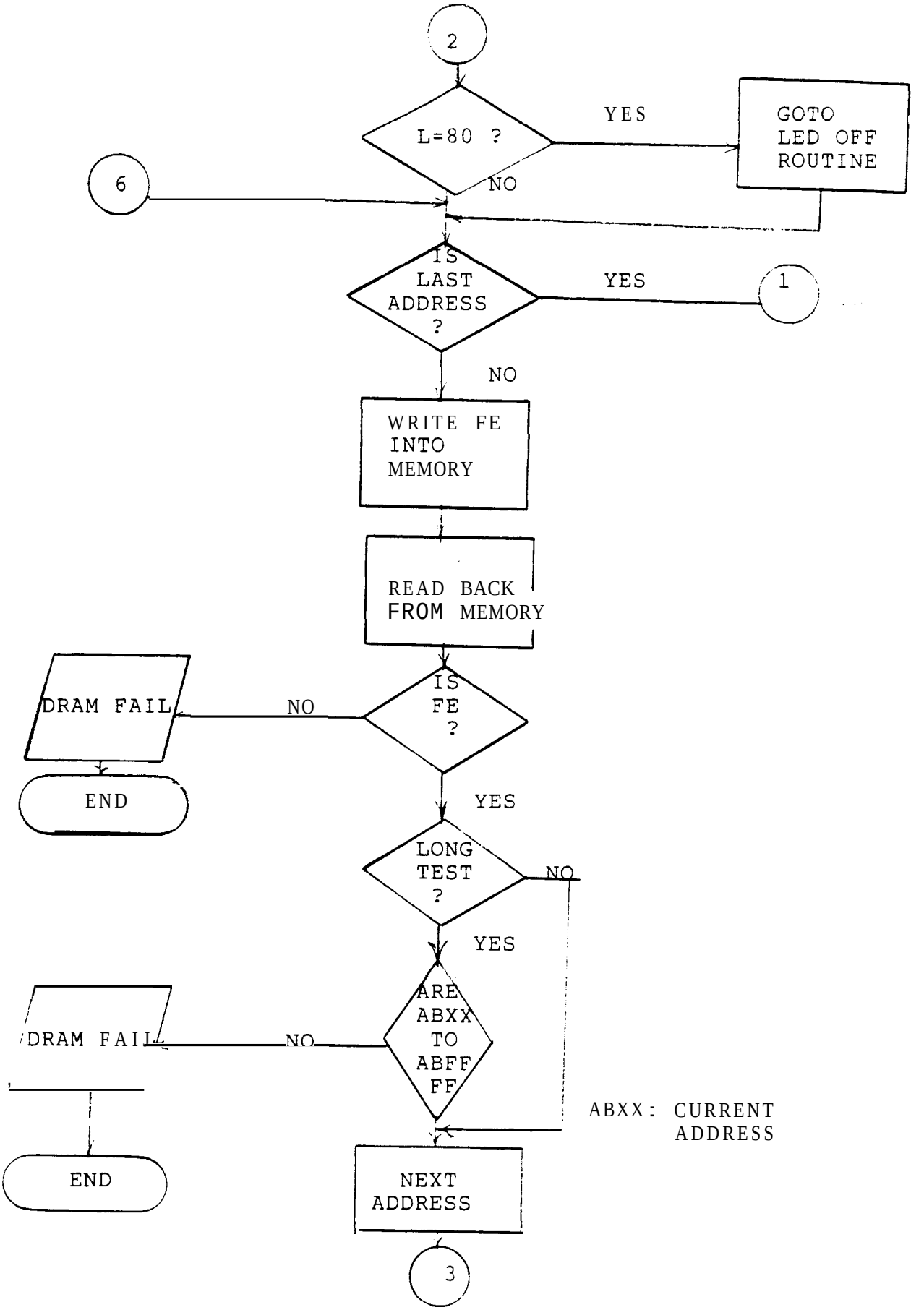


FIGURE 17. 64k DRAM Testing Program Flowchart (continued)

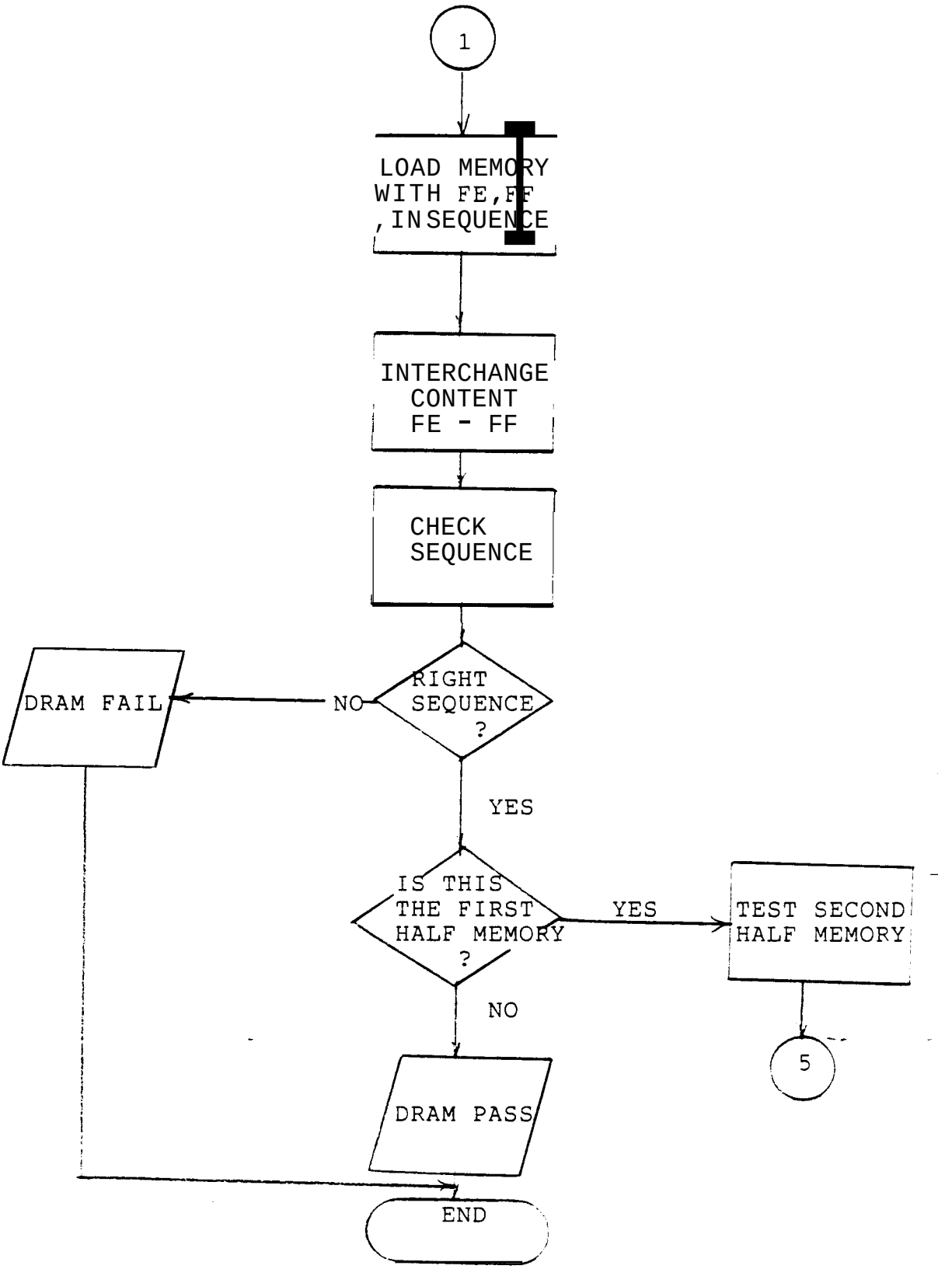


FIGURE 17. 64K DRAM Testing Program Flowchart

CHAPTER 7

SUMMARY

With the aid of a microcomputer design system, three RAM testing boards for a SRAM checker, a 16k DRAM checker, and a 64k DRAM checker respectively were sucessfully designed and built. The basic description of RAMs is discussed in chapter 2, the software system is described in chapter 6 and testing programs are listed in Appendix A, B and C. Many hardware and software problems are easily detected and solved with the use of a MDS, which helps to save a lot of time duringthe development process of the RAM testing boards. With the aid of a MDS, these checkers can be expanded to test additional memory chips.

7.1 Performance Evaluation of The Checkers

These RAM testers are designed to detect both the-- hard memory errors and soft memory errors to a high degree of accuracy. The testing accuracy of the RAM checkers can not be assigned a percentage value for RAMs in general but only for a particular RAM since the fabrication process differ for eachtype of RAM. Every memory chip type has its special characteristic and the failure distribution is different for each one. In Chapter 3, it was pointed out that soft memory errors associated with the system level problem and the rate of failure are hard to quantify. This is why no algorithm has ever been claimed to have a

percentile associated with its performance.

The testing method for SRAM is composed of barber-pole algorithm, sensitivity test algorithm and gallop-read alogrithm. For the DRAM, the same method can not be applied because of the long execution time (at least one hour is needed to test the 64k DRAM under 3.58 Mz with the same method that was applied to the SRAM). That is why only the barber-pole, the sensitivity algorithm and part of the gallop-write algorithms are employed by the DRAM checkers. The performance of the testing method when combining algorithms should be better than using a single algorithm which was discussed in Chapter 4.

7.2 Conclusion

Application of the microcomputer controlled RAM-checkers for the SRAM (8155 and 2114) and the DRAM (4116, 4164) results in detecting memory failures at a low cost and with a high degree of reliability.

In addition to the personal usage, these RAM testers could be very useful when starting up a small electronic assembly plant where an inexpensive tool, instead of a sophisticated ATE, is needed to give a good evaluation of memory chips, if the DC and AC parameters are not critical.

These RAM testers are very easy to use. No special training is needed to operate them. PASS and FAIL indicating-LEDs on the front panel will show the user if the RAM passes or fails the test.

As was indicated in the previous chapters, the RAM

checkers could be expanded to check other memory chips. Software writing may not be easy except for those who have the assembly language programming abiɩity. The memory chips to be tested in the RAM checkers are required to accompany the 8085 CPU. Cther chips that are used with a CPU other than the 8085 could be tested by employing the same technique described in this thesis except that the characteristics of the different types of CPU must be taken into account.

Recently, more powerful microcomputers with supporting hardware and software were developed. For instance, a 32-bit microcomputer was successfully manufactured. It is expected that the memory checker using the microcomputer-controlled program will become more sophisticated as other good testing algorithms evolve.

APPENDIX A

TESTING PROGRAM LISITING FOR SRAM

```
ISIS-II 8080/8085 MACRO ASSEMBLER, V4.1        MODULE   PAGE    1

 LOC  OBJ          LINE        SOURCE STATEMENT

                     1 ;*****************************************************************
                     2 ;*                        STATIC MEMORY TEST                     *
                     3 ;*****************************************************************
                     4 ;                                                    by Jinwei Hun9
                     5 ;                                                       15/11/85
                     6 ;DESCRIPTION:
                     7 ;*****************************************************************
                     8 ;* This testing program is composed of PATTERN TEST and SENSITIVITY
                     9 ;* TEST for the static RAMs (015512114)                          *
                    10 ;* A dip switch is installed on the front Panel, if the 1st switch*
                    11 ;* is at the on position, 2114 will be checked, otherwise 8155 is *
                    12 ;* the unit unuer checked.                                       *
                    13 ;* Port 21122 are being used br tne 8085 to indicate tne testing  *
                    14 ;* result, in any event , it is prohibited to remove 8155.       *
                    15 ;*****************************************************************
                    16 ;
                    17 ;
                    18 ;PART I
                    19 ;*****************************************************************
                    20 ;* Pattern test program is using the similar barber pole and     *
                    21 ;* mapped zeroes algorithm.                                      *
                    22 ;*****************************************************************
                    23 ;
                    24 ;
                    25 ;TEST 8155 memory cnip
0080                26  PAT    EQU     0080H           ;testing pattern stored here
2000                27  STB1   EQU     2000H           ;starting address of 8155
20FF                28  ENB1   EQU     20FFH           ;end address of 8155
0000                29         ORG     CH              ;starting program address
                    30 ;
                    31 ;
                    32 ;*****************************************************************
                    as ;* The following program is to assign the direction of I/O Ports. *
                    34 ;* and clear the panel LE3 ,turn on the 8155 indicator.          *
                    35 ;*****************************************************************
0000 3E01           36         3VI     A,01H           ,
0002 D320           37         OUT     20H
0004 DB22           38         IN      22H             ;read tne switch and select
0005 E601           39         ANI     01H             ;tne unit under test
0008 FE01           40         CFI     01H
OCOA C22001         41         JNZ     TE21            ;if panel=01 so to 2114 test
000D 3EFE           42         ■       A,0FEH          ;turn on tne 8155 indicator.
OCOF D321           43         OUT     21H
                    44 ;
                    45 ;
                    46 ;*****************************************************************
                    47 ;* Set all tne contents of all locations 0 in oruer to set reaur  *
                    48 ;* for the 0 test.                                               *
                    49 ;*****************************************************************
                    50 ;
                    51 ;
0011 210020         52         LXI     H,STB1          ;starting address of 8155
0014 3600           53  0000:  MVI     M,0H            ;move all locations with 0
0016 23             54         INX     H               ,
```

```
LOC  OBJ          LINE        SOURCE STATEMENT
0017 7C             55          30V     A,H
0018 FE21           56          CPI     21H             ;if not excede 2100 goto 0000
001A C21400         57          JNZ     0000            ,
                    58 ;
                    59 ;
                    60 ;*****************************************************************
                    61 ;* Get the Pattern from location PAT one by one , write into the *
                    62 ;* location , and pull it out to do the testing. Go to 0 test when*
                    63 ;* running out of the pattern at each location.                   *
                    44 ;*****************************************************************
                    55 ;
                    66 ;
001D 210020         67          LXI     H,ST81          ;starting address
0020 118000         68 LOOP1:   LXI     D,PAT           ;pattern stored here
0023 EB             69 LOOP2:   XCHG
0024 7E             70          MOV     A,M
0025 FE00           71          CPI     0H              ;if pattern is 0 ,then  do the zero
0027 CA3500         72          JZ      ZERO            ;test.
002A EB             73          XCHG
002B 77             74          MOV     M,A             ;location stored with pattern
002C 46             75          MOV     B,M
002D B8             76          CMP     B               ;check 'location content with pattern
002E C23B000        77          JNZ     FAIL            ;store if not equal then jump to the
0031 13             78          INX     D               ;FAIL souruotine .Otherwise go to next
0032 C32300         79          JMP     LOOP2           ;location.
                    80 ;
                    81 ;
                    82 ;ZEROES TEST
                    33 ;*****************************************************************
                    84 ;* This test is to test tf all those locations otner than the    *
                    85 ;* specified one contain 0 .                                     *
                    86 ;*****************************************************************
0035 EB             87 ZERO :   XCHG
0036 7E             88          MOV     A,M             ;get the compliment of the initial
0337 2F             89          CMA                     ;value to mask this specified locatton.
0038 47             90          nov     B,A
0039 110020         91          LXI     D,ST81
003C EB             92          XCHG
003D 7E             93 OLP  :   MOV     A,M
003E FE00           94          CPI     0H              ;compare all the content:  of locations
                    95                                  ;with zeros
0040 C25500         96          JNZ     MAP             ;if not 0 , then goto MAP  subroutine
                    97                                  ;to check if it is allowed.
0043 23             98 CON1 :   INX     H
0044 7C             99          MOV     A,H
0045 FE21           LOO         CPI     21H
0047 C23D00         131         JNZ     OLP
004A EB             102         XCHG
004B 23             103         INX     H               ;jump to succedins location
004C 7C             104         MOV     A,H             ;check if test complete ?
004D FE21           105         CPI     21H
004F CAHJOO         106         JZ      SETST           ;if complete sot0 sensitivity test
0052 C32000         107         JHP     LOOP1           ;or continue the pattern test
0055 7E             108 MAP  :  MOV     A,M             ;add up the content with that of
0056 90             139     .   ADD     B               ;the specified one
```

```
LOC  OBJ          LINE        SOURCE STATEMENT

0057 FEFF          110          C?I     0FFH            ;check if it is equal FFH
0059 C2B000        111          JHZ     FAIL            ;if not jump to FAIL subroutine
005C 3e00          112          MVI     M,0
005E C34300        113          JMP     CON1
3061 3EF6          114  PASS :  MVI     A,0F6H          ;set the pass light on
0063 D321          115          OUT     21H
0065 76            116          HLT
                   117 ;
                   118 ;
                   119 ;TESTING PATTERN
                   120 ;*****************************************************************
                   121 ;* These are the testing patterns for the 8155 testing program.  *
                   122 ;* OOH is followed to rerrent the end of the patterns.           *
                   123 ;*****************************************************************
0080               124          ORG     PAT
0080 01            125          3B      01H
0081 02            126          DB      02H
0032 04            127          DB      04H
0083 08            128          DB      08H
0034 10            129          DH      10H
0085 20            130          DB      20H
0036 40            131          DB      40H
0087 80            132          DB      80H
0088 FE            133          DB      OFEH
0089 FD            134          DB      0FDH
008A FB            135          DB      0FBH
008B F7            136          DB      0F7H
008C EF            137          DB      0EFH
008D DF            138          DB      0DFH
008E BF            139          DB      OPFH
OOBF 7F            140          DB      07FH
0090 00            141          DB      OOH
                   142 ;
                   143 ;
                   144 ;*****************************************************************
                   145 ;* This is to turn on the FAIL LED display.                      *
                   146 ;*****************************************************************
OOBO               147          ORG     OOBOH
00B0 3EFA          148 'AIL:    MVI     A,0FAH          ;set the FAIL light on.
00B2 D322          149          OUT     22H
OOBJ 76            150          HLT
                   151 I
                   152 ;
                   153 ;PART II
                   154 ;*****************************************************************
                   155 ;* This is to do the SENSITIVITY TEST to ensure the meoory isn't*
                   156 ;* affected by the other locations dur ng the switching period   *
                   157 ;* By storing 0 ~ FF into the location 2000 ~ 20FF i then        *
                   158 ;* reverse the sequence, then  check if the contents  of those   *
                   159 ;* locations  are in the reverse sequence  which ue demand.      *
                   160 ;*****************************************************************
                   161 ;SENSITIVITY TEST:
0085 210020        162  SETST: LXI     H,ST81          ;load 0~ff to t3e locations from
OOBS OE00          163          MVI     C,00H           ;2000~20ff
00BA 71            164  CONT2: MOV     M,C             ;C is tne content of each location.
```

```
LOC  OBJ          LINE        SOURCE STATEMENT

OOBH 23           165          INX    H              ;increase the location .
OOBC 7C           166          MOV    A,H            ;check if done ?
00BD FE21         167          CPI    21H
OOBF CAC600       168          JZ     CHK1           ;yes, go on to  CHK routine to
                  169                                 ;interchange the content of specified
                  170                                 ;locations.
00C2 0C           171          INR    C
00C3 C3BA00       172          JHF    CON72
00C6 11FF20       173  CHK1 :  LXI    D,EN81         ;interchange tne contents of locatons
00C9 210020       174          LXI    H,ST81         ;2000~20FF,2001~20FE,2002~20FD.....
OOCC 46           175  LOOP3:  MOV    B,M
00CD EP           176          XCHG
OOCE 4E           177          nOV    C,M
00CF 70           178          nOV    M,B
OODO EY           179          XCHG
3001 71           180          MOV    M,C
00D2 1B           181          DCX    D
00D3 23           182          INX    H
00D4 7D           183          MOV    A,L            ;check if all done
0005 FEQO         184          CPI    80H
00D7 C2CC00       185          JNZ    LOOP3
                  186 ,
                  187 ,
                  188 ;THE FOLLOWING PROGRAM IS TO CHECK IF THE CONTENT OF THE ARRAY IS
                  189 ;IN THE ORDER FROM LARGE TO SMALL.
00DA 210020       190          LXI    H,ST81
00DD 1600         191          MVI    D,00H          ,
00DF 15           192  LOOP4:  DCR    D              ;
00E0 CA6100       193          JZ     PASS
00E3 97           194          SUB    A              ;reset tne carry flag
00E4 7E           195          MOV    A,M
00E5 23           196          INX    H
00E6 96           197          SUB    M
00E7 DAB000       198          JC     FAIL
OOEA CAR000       199          JZ     FAIL
OOED C3DF00       200          JMP    LOOP4
                  201 ,
                  202 .
0800              203  ST21    EQU    0800H
08FF              204  EN21    EQU    OPFFH
0200              205  PAT2    EQU    0200H
                  206 ;*****************************************************************
                  207 ;* The following program is to test tne 2114 (2k*4) memory , tne*
                  208 ;* algorithm used is tne same as tne one beibg used in tne above*
                  209 ;* program.                                                      *
                  210 ;*****************************************************************
                  211 ,
                  212 ,
                  213 ;TEST 2114 CHIP
                  214 ;PART I
                  215 ;PATTERN TEST FOR 2114
                  216 ;*****************************************************************
                  217 ;* The following program is to reset the indicators and turn on  *
                  218 ;* tne 2114 indicator.                                           *
                  219 ;*****************************************************************
```

```
ISIS-II 8080/8085 MACRO ASSEMBLER, V4.1        MODULE   PAGE    5

 LOC  OBJ          LINE        SOURCE STATEMENT

 0120              220          ORG     0120H
 0120 3EFF         221  TE21 :  MVI     A,0FFH          ;reset the pass indicator
 0122 D322         222          OUT     22H
 0124 3EFD         223          MVI     A,0FDH          ;turn on the 2114 indicator
 0126 D321         224          OUT     21H
                   225
                   226
                   227 ;*****************************************************************
                   228 ;* The following program is to set all the contents of the memory
                   229 ;* location to be 0 in order to set ready for the zero test      *
                   230 ;*****************************************************************
 012B 21000B       231          LXI     H,ST21
 012B 36F0         232  LOOP5: MVI     M,0F0H
 .)LID 23          233          INX     H
 012E 7C           234          MOV     A,H
 012F FE0C         235          CPI     0CH
 0131 C22B01       236          JNZ     LOOP5
                   237 ;
                   238 ;
                   239 ;*****************************************************************
                   240 ;* Get the pattern from location PAT2 one by one , write into the
                   241 ;* location , and pull it out for the testing. Goto 0 test when  *
                   242 ;* run out of the pattern at each location.                      *
                   243 ;*****************************************************************
                   244 ;
                   245 ;
 0134 210009       246          LXI     H,ST21
 9137 110002       247  LOOP6: LXI     D,PAT2
 013A 7D           248          MOV     A,L             ;move L to A
 013B FE00         249          CPI     00H             ;if L=O so to LEDON
 013D CAA801       250          JZ      LEDON
 0140 FE20         251          CPI     20H             ;if L=20 so to LEDOF
 0142 CAA101       252          JZ      LEDOF
 0145 FE40         253          CPI     40H             ;if L=40 so to LEDON
 0147 CAA801       254          JZ      LEDON
 014A FE60         255          CPI     60H             ;if L=60 so to LEDOF
 014C CAA101       256          JZ      LEDOF
 014F FE80         257          CPI     80H             ;if L=80 so to LEDON
 0151 CAA801       258          JZ      LEDON
 0154 FEAO         259          CPI     OAOH            ;if L=A0 so to LEDOF
 0156 CAA101       160          JZ      LEDOF
 0159 FECO         261          CPI     OCOH            ;if L=C0 so to LEDON
 015B CAA801       262          JZ      LEDON
 015E FEE0         263          CPI     OEOH            ;if L=E0 so to LEDOF
 0160 CAA101       264          JZ      LEDOF
 0163 EB           255  LOOP7: XCHG
 0164 7E           266          MOV     A,M
 0165 FEF0         267          CPI     0F0H
 0167 CA7301       268          JZ      ZOTE
 016A EB           269          XCHG
 016B 4F           270          MOV     C,A
 016C 77           271          MOV     M,A
 016D 7E           271          MOV     A,M
 016E F6F0         273          ORI     0F0H
 0170 Y9           274          CMP     C
```

```
ISIS-II 8080/8085 MACRO ASSEMBLER, V4.1        MODULE   PAGE    6

 LOC  OBJ          LINE        SOURCE STATEMENT

 0171 C29C01        275          JNZ     FAI2
 0174 13            276          INX     3
 0175 C36301        277          JMP     LOOP7
                    278 ;
                    279 ;
                    280 ;ZEROES TEST FOR 2114
                    281 ;*****************************************************************
                    282 ;This test is to check if all locations other than the specified*
                    283 ;* one contain zero.                                            *
                    284 ;*****************************************************************
 0178 EB            285  ZOTE : XCHG
 0179 50            296          MOV     E,L
 017A 54            237          MOV     D,H
 017B 23            238          INX     H
 017C 7C            239          MOV     A,H
 017D FE0C          290          CPI     OCH
 017F CA0802        291          JZ      SETS2
 0132 7E            292  LOOPS:  MOV     A,M
 0183 F6F0          293          ORI     0F0H
 0185 FEF0          294          CPI     0F0H
 0107 C29C01        275          JNZ     FAI2
 018A 23            296          INX     H
 018B 7C            297          MOV     A,H
 018C FE0C          298          CPI     OCH
 018E C28201        299          JNZ     LOOPB
 0191 6B            300          MOV     L,E
 0192 62            301          MOV     H,D
 0193 23            302          INX     H
 0174 C33701        303          JMP     LOOP6
 0197 3EF5          304  PSS   : MVI     A,0F5H
 0199 D321          305          OUT     21H
 019B 75            306          HLT
 019C 3EF9          307  FAI2 :  MVI     A,0F9H
 019E D321          308          OUT     21H
 01A0 75            309          HLT
 01A1 3EFD          310  LEDOF:  MVI     A,0FDH
 01A3 9321          311          OUT     21H
 01A5 C36301        312          JMP     LOOP7
 01A8 3EF1          313  LEDON:  MVI     A,0F1H
 01AA D321          314          OUT     21H
 01AC C36301        315          JMP     LOOP7
                    316 ;
                    317 ;
                    318 ;TESTING PATTERN FOR 2114
                    319 ;*****************************************************************
                    320 ;*This is the testing program for the 2114 memory chip, 00H is  *
                    321 ;* followed to repeat the end of the test.                       *
                    322 ;*****************************************************************
 0200               323          ORG     PAT2
 0200 F1            324          DB      0F1H
 0201 F2            325          DB      0F2H
 0202 F4            326          OH      0F4H
 0203 F8            327          DB      0F8H
 0204 FE            328          DB      0FEH
 0205 FD            329          DB      0FDH
```

```
LOC  OBJ          LINE        SOURCE STATEMENT

0206 F7            330          DB     0F7H
0207 F0            331          DB     0F0H
                   332
                   333 ;
                   334 ;PART II
                   335 ;*****************************************************************
                   336 ;* This is to do the SENSITIVITY TEST to ensure the memory is'nt *
                   337 ;* affected by the other memory  during the switching period. *
                   338 ;* By storing 00 ~ 0F into the first  specified locations subset *
                   339 ;* then soon to other subset till the end of the locations     *
                   340 ;* Reverse those contents in the subset n ; it fails unless the*
                   341 ;* array is in the order from large to small unen ue cnecr. the *
                   342 ;* order.                                                       *
                   343 ;*****************************************************************
                   344 ;SENSITITY TEST FOR 2114
0208 21000B        345 SETS2: LXI    H,ST21
020B 11FF0B        346        LXI    D,EN21
020E 0E00          347        MVI    C,00
0210 71            348 LOOP9: MOV    M,C
0211 0C            349        INR    C
0212 23            350        INX    H
0213 7C            351        MOV    A,H
0214 FE0C          352        CPI    0CH
0216 C21002        353        JNZ    LOOP9
0219 210008        354 REV  : LXI    H,ST21
021C 46            355 LOOPA: MOV    B,M
021D EB            356        XCHG
021E 7E            357        MOV    A,M
021F 70            358        MOV    M,B
0220 EB            359        XCHG
0221 77            360        MOV    M,A
0222 1B            361        DCX    D
0223 23            362        INX    H
0224 7C            363        MOV    A,H
0225 FE0A          364        CPI    0AH
0227 CA2D02        365        JZ     CHK
022A C31C02        366        JMP    LOOP?
022D 210008        367  CHK : LXI    H,ST21
0230 46            368 LOOPB : MOV    B,M
0231 7D            369        MOV    A,L
0232 30            370        ADD    B
0233 E60F          371        ANI    0FH
0235 FE0F          372        CPI    0FH
0237 C29C01        373        JNZ    FA12
023A 23            374        INX    H
023B 7C            375        MOV    A,H
023C FE0C          376        CPI    0CH
023E C23002        377        JNZ    LOOPB
0241 C39701        378        JMP    PSS
                   379        END

PUBLIC SYMBOLS
```

EXTERNAL SYMBOLS

USER SYMBOLS

CHK	A	022D	CHK1	A	00C6	CON1	A	0043	CONT2	a	00BA	EN21	A	0BFF	EN81	A	20F
FAIL	A	00B0	LEDOF	A	01A1	LEDON	A	01A8	LOOP1	A	0020	LOOP2	A	0023	LOOP3	A	00C
LOOP5	A	012B	LOOP6	A	0137	LOOP7	A	0163	LOOP8	A	0182	LOOP9	A	0210	LOOPA	A	021
MAP	A	0055	OLP	A	003D	0000	A	0014	PASS	A	0061	PAT	A	0080	PAT2	A	020
REV	A	0219	SETS2	A	020B	SETST	A	00B5	ST21	A	0B00	ST81	a	2000	TE21	A	012
ZOTE	A	0178															

ASSEMBLY COMPLETE, NO ERRORS

APPENDIX B

TESTING PROGRAM LISTING FOR 16K DRAM

```
ASM80 :F1:JL.ASM

ISIS-II 8080/8085 MACRO ASSEMBLER) V4.1         MODULE   PAGE    1

  LOC  OBJ          LINE        SOURCE STATEMENT

                      1 ;*******************************************************
                      2 ;*                 16K   DYNAMIC MEMORY TEST             *
                      3 ;*******************************************************
                      4 ;
                      5 ;
                      6 ;DESCRIPTION:
                      7 ;*******************************************************
                      8 ;* This testing program uses the same algorithm as we  *
                      9 ;* have for the static RAM test. The only difference is*
                     10 ;* that the user can have a choice to select the testing
                     11 ;* method either with or without the MAPPED 1 test by  *
                     12 ;* setting the toggle switch on the front panel.        *
                     13 ;*******************************************************
                     14 ;
                     15 ;
                     16 ;PART I, PATTERN TEST
 4000                17  ST16    EQU     4000H   ;starting address for 4116
 7FFF                18  EN16    EQU     7FFFH   ;end address for 4116
 0000                19          ORG     0H
 0000 3EFF           20          MVI     A,0FFH  ;assign the I/O port
 0002 D302           21          OUT     2H
 0004 3EFE           22          MVI     A,0FEH  ;set the 4116 indicator on
 0006 D300           23          OUT     0H
 0008 3E00           24          MVI     A,0     ;assign the I/O port
 000A D303           25          OUT     3H
 000C DB01           26          IN      01H     ;read the toggle switch position
 000E E601           27          ANI     01H
 0010 4F             28          MOV     C,A     ;store to C
 0011 110040         29          LXI     H,ST16  ;move all the memory locations with
                     30                          ;FF
 0014 36FF           31  LOOP1:  MVI     M,0FFH
 0016 23             32          INX     H
 0017 7C             33          MOV     A,H
 0018 FE80           34          CPI     80H
 001A C21400         35          JNZ     LOOP1
 001D 210040         36          LXI     H,ST16  ;move frrst location to HL,
                     37                          ;get ready for the test.
 0010 7D             38  LOOP2:  MOV     A,L     ;if L=0 go to LENON routine
 0011 FE00           39          CPI     00H
 0023 CA7000         40          JZ      LEDON
 0026 FE80           41          CPI     80H     ;if L=80 go to LENOF routine
 0028 CA7700         42          JZ      LEDOF
 002B 3EFE           43  LOOP3:  MVI     A,0FEH  ;move FE to A
 002D 77             44          MOV     M,A     ;move A to memory location
 002E 7E             45          MOV     A,M     ;move back to A
 002F F6FE           46          ORI     0FEH
 0031 FEFE           47          CPI     0FEH    ;compare with FE
 0033 C26B00         48          JNZ     FAIL    ;not equal, so to FAIL
 0036 C34200         49          JMP     ZERO    ;yes, so to ZERO routine
 0039 7C             50  BBH   : MOV     A,H     ;is test completed ?
 003A FE80           51          CPI     80H
 003C C22000         52          JNZ     LOOP2   ;no, so to LOOP2
 003F C37E00         53          JMP     SENST   ;yes, go to SENST
 0042 79             54  ZERO  : MOV     A,C     ;check the toggle position
```

```
ISIS-II 8080/8085 MACRO ASSEMBLER, V4.1         MODULE   PAGE    2

 LOC  OBJ          LINE        SOURCE STATEMENT

 003B 7E             55          MOV     A,M     ;move back to A
 003C F6FE           56          ORI     0FEH
 003E FEFE           57          CPI     0FEH    ;compare with FE
 0040 C27D00         58          JNZ     FAIL    ;not equal, go to FAIL
 0043 C34F00         59          JMP     ZERO    ;yes, go to ZERO routine
 0046 7C             60  BBB   : MOV     A,H     ;is test completed ?
 0047 FE00           61          CPI     00H
 0049 C22D00         62          JNZ     LOOP2   ;no, go to LOOP2
 004C C39300         63          JMP     SENST   ;yes, go to SENST
 004F 3AFF20         64  ZERO  : LDA     20FFH   ;check the toggle position
 0052 E602           65          ANI     02H
 0054 FE02           66          CPI     02H     ;compare with 02
 0056 CA7300         67          JZ      CCC     ;equal, go to CCC
 0059 5D             68          MOV     E,L     ;no, store HL to DE
 005A 54             69          MOV     D,H
 005B 23             70          INX     H       ;increase HL
 005C 7D             71          MOV     A,L     ;check if L larger than FF
 005D D600           72          SUI     0H
 005F CA7100         73          JZ      AAA     ;yes, go to AAA
 0062 7E             74  LOOP4: MOV     A,M     ;no, start one test
 0063 F6FE           75          ORI     0FEH
 0065 FEFF           76          CPI     0FFH    ;check if is one?
 0067 C27D00         77          JNZ     FAIL    ;no, go to FAIL
 006A 7D             78          MOV     A,L
 006B 23             79          INX     H       ;next location
 006C FEFF           80          CPI     0FFH    ;if it larger than FF
 006E C26200         81          JNZ     LOOP4   ;no, go to LOOP4
 0071 6B             82  AAA   : MOV     L,E     ;yes, mov DE back to HL
 0072 62             83          MOV     H,D
 0073 23             84  CCC   : INX     H       ;increase HL
 0074 C34600         85          JMP     BBB     ;go to BBB
 0077 3AFA20         86  PASS  : LDA     20FAH   ;PASS indicator data
 007A D322           87          OUT     22H
 007C 76             88          HLT
 007D 3AFB20         89  FAIL  : LDA     20FBH   ;FAIL indicator data
 0080 D322           90          OUT     22H
 0082 76             91          HLT
 0083 3AFC20         92  LEDON: LDA     20FCH   ;LEDON indicator data
 0086 D322           93          OUT     22H
 0088 C33800         94          JMP     LOOP3
 008B 3AFD20         95  LEDOF: LDA     20FDH   ;LEDOFF indicator data
 008E D322           96          OUT     22H
 0090 C33800         97          JMP     LOOP3
                     98 ;This part of the test is to verify the sensitivity of
                     99 ;memory
                    100 ;The folling program is to store 0,1,0,1  ... to memory
                    101 ;location
 0093 210080        102  SENST: LXI     H,ST64  ;load 0,1,0,1 ...sequence to memory
 0096 11FFFF        103         LXI     D,EN64
 0099 0E00          104         MVI     C,00
 009B 71            105  LOOP5: MOV     M,C
 009C 0C            106         INR     C
 009D 23            107         INX     H
 009E 7C            108         MOV     A,H     ;if it complete?
 009F FE00          109         CPI     00H
```

```
ISIS-II 8080/8085 MACRO ASSEMBLER, V4.1          MODULE  PAGE   3

  LOC  OBJ          LINE        SOURCE STATEMENT

  009B 70            110          MOV     M,B     ;move M to B
  009C 2B            111          DCX     H       ;decrease H
  009D 77            112          MOV     M,A     ;move A to M
  009E 23            113          INX     H       ;increase H
  009F C39200        114          JMP     LOOPA   ;jump to LOOPA
                     115 ;The following program is to check if the contents of
                     116 ;each location are in the right sequence uhich we demand.
  00A2 210040        117  CHK   : LXI     H,ST16
  00A5 7E            118  LOOPB: MOV     A,M     ;move M to A
  00A6 23            117          INX     H       ;increase H
  00A7 BE            120          CMP     M       ;compare uith M
  00AQ CA6B00        121          JZ      FAIL    ;if not equal go to FAIL
  00AB 7C            122          MOV     A,H     ;check if test complete
  00AC FEB0          133          CFI     B0H
  00AE CA6600        124          JZ      PASS
  00B1 C3A500        125          JMP     LOOFP   ;no, go on
                     126
                     127 END


PUBLIC SYMBOLS

EXTERNAL SYMBOLS


USER SYMBOLS
AAA     A 0060    BBB     A 0039    CCC     A 0062    CHK     A 00A2    EN16    A 7FFF    FAIL    A 006B
LEDON   A 0070    LOOP1   A 0014    LOOP2   A 0020    LOOP3   A 002B    LOOP4   A 0351    LOOP5   A 0036
LOOP'F  A 00A5    PASS    A 0066    REV     A 008F    SENST   A 007E    ST16    A 4000    ZERO    A 0042

ASSEMBLY COMPLETE,  NO ERRORS
```

APPENDIX C

TESTING PROGRAM LISTING FOR 64K DRAM

```
ASM80 :F1:HL.ASM

ISIS-II 8080/8085 MACRO ASSEMBLER, V4.1          MODULE   PAGE    1

 LOC  OBJ          LINE        SOURCE STATEMENT

                    1 ;*******************************************************
                    2 ;*                 64K   DYNAMIC MEMORY TEST             *
                    3 ;*******************************************************
                    4 ;
                    5 ;
                    6 ;DESCRIPTION:
                    7 ;*******************************************************
                    8 ;* This testing program uses the same algorithm as we  *
                    9 ;* have for the static RAM test. The only difference is*
                   10 ;* tnat the user can nave a choice to select tne testing
                   11 ;* method eitner witn or witnout the MAPPED 1 test by  *
                   12 ;* setting tne toggle switch on the front panel.       *
                   13 ;* 4164 has 64k*1 memory capacitr. virtue memory method*
                   14 ;* is needed for the whole test with the 3055. There are
                   15 ;* tuo 3000 to FFFF location s selected by one I/O port*
                   16 ;* line.                                               *
                   17 ;*******************************************************
                   18 ;
                   19 ;
                   20 ;PART I, PATTERN TEST
 8000              21  ST64   EQU     8000H   ;starting address for 4164
 FFFF              22  EN64   EQU     OFFFFH  ;end address for 4154
 0000              23         ORG     0H
 0000 3E02         24         MVI     A,02H   ;assign the 1/0 port
 0001 D320         25         OUT     20H
 0004 3EFE         26         MVI     A,0FEH  ;set the 4164 indicator on
 0006 D322         27         OUT     22H
 0008 32FE20       28         STA     20FEH   ;store for later usage
 000B DB21         29         IN      21H     ;read the toggle switch position
 000D 32FF20       30         STA     20FFH   ;store here
 0010 21FA20       31         LXI     H,20FAH ,
 0013 36FC         32         MVI     M,0FCH  ;store the 1st routine PASS data
 0015 23           33         INX     H
 0016 36FA         34         MVI     M,0FAH  ;store the 1st routine FAIL data
 0018 23           35         INX     H
 0019 36F8         36         MVI     M,0F8H  ;store the 1st routine LLDON data
 001B 23           37         INX     H
 001C 36FE         38         nUI     n,0FEH  ;store the 1st routine LEDOF data
 001E 210080       39  START: LXI     H,ST64  ;move all the memory locations with
                   40                         ;FF
 0021 36FF         41  LOOP1: MVI     n,0FFH
 0023 23           42         INX     H
 0024 7C           43         MOV     A,H
 0025 FE00         44         CPI     00H
 0027 C22100       45         JNZ     LOOP1
 002A 210090       46         LXI     H,ST64  ;move first location to HL,
                   47                         ;set ready for the test.
 002D 7D           48  LOOP2: MOV     A,L     ;if L=0 so to LENON routine
 002E FE00         49         CPI     00H
 0030 CA8300       50         JZ      LEDON
 0033 FE80         51         CPI     80H     ;if L=80 so to LENOF routine
 0035 CA8B00       52         JZ      LEDOF
 0038 3EFE         53  LOOP3: MVI     A,0FEH  ;move FE to A
 003A 77           54         MOV     M,A     ;move A to memory location
```

```
LOC  OHJ       LINE        SOURCE STATEMENT

0043 FE01        55        CFI     01H     ;compare with 01
0045 CA6200      56        JZ      CCC     ;equal, go to CCC
0048 5D          57        MOV     E,L     ;no, store HL to DE
0049 54          58        MOV     D,H
004A 13          59        INX     H       ;increase HL
004B 70          60        MOV     A,L     ;check if L larger than FF
004C D600        61        SUI     CH
004E CA6000      62        JZ      AAA     ;yes, go to AAA
0051 7E          63  LOOP4: MOV     A,M     ;no, start one test
0052 F6FE        64        ORI     OFEH
0054 FEFF        65        CPI     OFFH    ;check if it one?
0056 C26B00      66        JNZ     FAIL    ;no, do to FAIL
0059 7D          67        MOV     A,L
005A 23          68        INX     H       ;next location
005B FEFF        69        CPI     OFFH    ;if it larger than FF ?
005D C25100      70        JNZ     LOOP4   ;no, so to LOOP4
0060 6B          71  AAA   : MOV     L,E     ;yes, aov DE back to HL
0061 62          72        MOV     H,D
0061 23          73  CCC   : INX     H       ;increase HL
0063 C33900      74        JMP     BBR     ;go to BBH
0066 3EFC        75  PASS  : MVI     A,0FCH  ;PASS indicator data
0068 D300        76        OUT     CH
006A 76          77        HLT
006B 3EFA        78  FAIL  : MVI     A,0FAH  ;FAIL indicator data
006D D300        79        OUT     CH
006F 76          80        HLT
0070 3EFB        81  LEDON: MVI     A,0FBH  ;LEDON indicator data
0072 D300        82        OUT     CH
0074 C32B00      83        JMP     LOOP3
0077 3EFE        84  LEDOF: MVI     A,0FEH  ;LEDOFF indicator data
0079 D300        85        OUT     CH
007B C32B00      86        JMP     LOOP3
                 87 ;This part of the test is to verify the sensitivity of
                 88 ;memory
                 89 ;The folling program is to store 0,1,0,1  ... to memory
                 90 ;location
007E 110040      91  SENST: LXI     H,ST16  ;load 0,1,0,1 ...sequence to memory
0031 11FF7F      92        LXI     D,EN16
0084 0EC0        93        MVI     C,00
0085 71          94  LOOP5: MOV     M,C
0087 0C          95        INR     C
0098 23          96        INX     H
0009 7C          97        MOV     A,H     ;if it complete?
009A FE80        98        CPI     30H
0CCC C28600      99        JNZ     LOOP5   ;no, 90 to LOOP5
                100 ;The following program is to interchange the memory
                101 ;content , 4000 ~ 4001 , 4002~4003, ....
008F 210040      102  REV  : LXI     H,ST16
0092 46          103  LOOPA: MOV     B,M
0093 23          104        INX     H
0094 7C          105        MOV     A,H     ,
0095 FE80        106        CPI     80H
0097 CAA200      107        JZ      CHK     ;if reversion is completed so
                 108                        ;to check it.
00YA 7E          109        MOV     A,M     ;move M to A
```

```
ISIS-II 8080/8085 MACRO ASSEMBLER, V4.1        MODULE   PAGE    3

  LOC  OBJ          LINE        SOURCE STATEMENT

  00A1 C29B00        110          JNZ     LOOP5   ;no, So to LOOPS
                     111 ;The following program is to interchange the memory
                     112 ;content , 8000 ~ 8001 , 8002~8003, ....
  00A4 210080        113  REV   : LXI     H,ST64
  00A7 46            114  LOOPA: MOV     B,M
  00A8 23            115          INX     H
  00A9 7C            116          MOV     A,H     ;
  00AA FE00          117          CPI     00H
  00AC CAP700        118          JZ      CHK     Iif reverision is completed so
                     119                          ;to check it.
  00AF 7E            120          MOV     A,M     ;move M to A
  00P0 70            121          MOV     M,B     ;move M to B
  00B1 2B            122          DCX     H       ;decrease H
  00B2 77            123          MOV     M,A     ;move A to M
  00B3 23            124          INX     H       ;increase H
  00B4 C3A700        125          JMP     LOOPA   ;jump to LOOPA
                     126 ;The following program is to check if the contents of
                     127 ;each location are in the right sequence which we demand.
  00B7 210080        128  CHK   : LXI     H,ST64
  00PA 7E            129  LOOPB: MOV     A,M     ;move M to A
  00PR 23            130          INX     H       ;increase H
  00PC RE            131          CMP     M       ;compare with M
  00BD CA7D00        132          JZ      FAIL    Iif not equal so to FAIL
  00C0 7C            133          MOV     A,H     ;check if test complete
  00C1 FE00          134          CPI     00H
  00C3 C2BA00        135          JNZ     LOOPP   ;no, so on
  00C6 3AFE20        136          LDA     20FEH   ;yes, load 20FE to A
  00C9 FE06          137          CPI     06H     ;compare with 6
  00CB CA7700        138          JZ      PASS    ;if it is equal so to PASS
  00CE 21FA20        139          LXI     H,20FAH ;no, reset
  00D1 3604          140          MVI     M,04H   ;PASS indicator data
  00D3 23            141          INX     H
  00D4 3602          142          MVI     M,02H   ;FAIL indicator data
  00D6 23            143          INX     H
  00D7 3600          144          MVI     M,0H    ;LEDON indicator data
  00D9 23            145          INX     H
  00DA 3606          146          MVI     M,06H   ;LEDOF indicator data
  00PC 7E            147          MOV     A,M
  00DD D322          148          OUT     22H     ;reset LED
  00DF 32FE20        149          STA     20FEH   I
  00E2 C31E00        150          JMP     START   ;go to another 8000 to
                     151                          ;FFFF routine.
                     152 END


PUBLIC SYMBOLS


EXTERNAL SYMBOLS


USER SYMBOLS
AAA    A 0071   BBB    A 0046   CCC    A 0073   CHK    A 00B7   EN64   A FFFF   FAIL   A 007D
LEDON  A 0083   LOOP1  A 0021   LOOP2  A 002D   LOOP3  A 0038   LOOP4  A 0062   LOOPS  A 0098
LOOP0  A 00BA   PASS   A 0077   REV    A 00A4   SENST  A 0093   ST64   A 8000   START  A 001E
```

ASSEMBLY COMPLETE, NO ERRORS

APPENDIX D

SPECIFICATION OF CHIPS USED IN THE CHECKERS

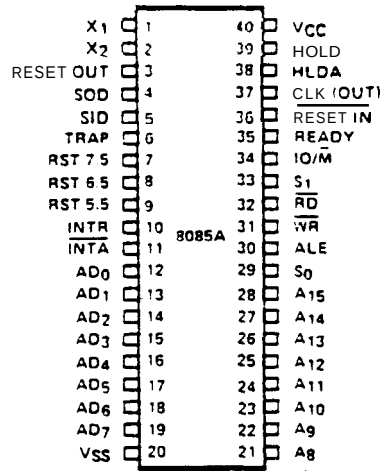


Figure 2 8085A Pinout Diagram

8085A FUNCTIONAL PIN DEFINITION

The following describes the function of each pin:

Symbol	Function
A_8–A_{15} (Output. 3-stat.)	Address Bus: The most significant 8 bits of the memory aaaress or the 8 bits of the I/O address. 3-stated during Hold and Halt modes and durlng RESET.
AD_{0-7} (Input/Output, 3-state)	Multiplexed Address/Data Bus: Lower 8 bits of the memory address (or I/O address) appear on the bus during the first clock cycle (T state) of a machtne cycle. It then becomes the data bus durlng the secona ana third clock cycles.
ALE (Output)	Address Latch Enable It occurs during the first clock state of a machine cycle and enables the address to get latched into the on-chip latch of peripherals The falling edge of ALE is set to guarantee setup and hold times for the address information The fall-ing edae of ALE can also be used to strobe the status information ALE is never 3-stated
So. **S_1**, and **IO/$\overline{M}$** (Output)	Machine cycle status: IO/$\overline{M}$ S_1 So Status 0 0 1 Memory write 0 1 0 Memory read 1 0 1 I/O write 1 1 0 I/O read 0 1 1 Opcode fetch 1 1 1 Interrupt Acknowledge 0 0 Halt X X Hold X X Reset • = 3-state high impedance) X = unspecified
Symbol	Function
	St can oe used as an advanced R/$\overline{W}$ status. IO/$\overline{M}$.S_0 and S_1 become valid at the beginning of a machine cycle and remain stable throughout the cycle The falling edge of ALE mav be used to latch the state of these lines
$\overline{RD}$ (Output. 3-state)	READ control A low level on $\overline{RD}$ indicates the selected memory or I/O device is to be read and that the Data Bus is available lor the data transfer 3-stated during Hold and Halt modes and durtng RESET
$\overline{WR}$ (Output, 3-atate)	WRITE control A low level on $\overline{WR}$ indicates the data on the Data Bus is to be written into the selected memory or I/O location Data is set up at the trailing edge of $\overline{WR}$ 3-stated durlng Hold and Halt modes and durlng RESET
READY (Input)	If READY is high during a read or write cycle. it indicates that the memory or peripheral is ready to send or receive data If READY is low the cpu will wait an integral number of clock cycles for READY to go high before completing the read or write cycle
HOLD (Input)	HOLD indicates that another master is requesting the use of the address and data buses The cpu. upon receiving the hold request. will relinquish the use of the bus as soon as the completion of the current bus transfer Internal processing can continue The processor can regain the bus only alter the HOLD is removed When the HOLD is acknowledged the Address. Data. $\overline{RD}$, $\overline{WR}$, ana IO/$\overline{M}$ lines are 3-stated
HLDA (Output)	HOLD ACKNOWLEDGE Indicates that the cpu has received the HOLD request and that it will relinquish the bus in the next clock cycle HLDA goes low after the Hold request is removed. The cpu takes the bus one half clock cycle alter HLDA goes low
INTR (Input)	INTERRUPT REOUEST is used as a general purpose interrupt It is sampled only during the next to the last clock cycle of an instruction and during Hold and Halt states If it is active the Program Counter PC will be inhibited from incrementing and an $\overline{INTA}$ will be issued During this cycle a RESTART or CALL instruction can be inserted to jump to the interrupt service routine The INTR is enabled and disabled by software It is disabled by Reset and immediately atter an interrupt is acceoted.

8085A FUNCTIONAL PIN DESCRIPTION (Continued)

Symbol	Function
$\overline{INTA}$ (Output)	INTERRUPT ACKNOWLEDGE Is used instead of and has tne same timing as $\overline{RD}$ during the instruction cycle atter an INTR is accepted. It can be used to activate the 8259 Interrupt chip or some other interrupt port.
RST 5.5 RST 6.5 RST 7.5 (Inputs)	RESTART INTERRUPTS. These three inputs nave the same timing as INTR exceot they cause an internal RESTART lo be automatically inserted The priority of these Interrupts is ordered as shown in Table 1 These interrupts have a higner priority than INTR. In addition, they may be individually masked out using the SIM instruction.
TRAP (Input)	Trap Interrupt is a nonmaskable RESTART interrupt. It is recognized at the same time as INTR or RST 5.5-7 5. It is unaffected by any mask or Interrupt Enable. It has the highest priority of any interruot. (See Table 1).
$\overline{RESET\ IN}$ (Input)	Sets the Program Counter to zero and resets the interrupt Enable and HLDA flip-flops. The data and address buses and the control lines are 3-stated during RESET and because of the asynchronous nature of RESET. the processor's internal registers and flags may be altered by RESET with unpredictable results. $\overline{RESET\ IN}$ is a Schmitt-triggered input. allowing connection to an R-C network lor power-on RESET delay The cpu is held in tne reset condition as long as $\overline{RESET\ IN}$ is applied.
RESET OUT (Output)	Indicates cpu is being reset. Can oe used as a system reset The signal is synchronized to the processor clock and lasts an integral numoer of clock periods.
X_1, X_2 (Input)	X_1 and X_2 are connected to a crystal. LC, or RC network to drive the internal clock generator X_1 can also be an external clock input from a logic gate. The input frequency is divided by 2 to give rhe processors internal operating frequency
CLK (Output)	Clock Output for use as a system clock The period of CLK is twice the Xi. X_2 input period
SID (Input)	Serial input data line. The data on this line is loaded into accumulator bit 7 wnenever a RIM instruction is executed.
SOD (Output)	Serial output data line The output SOD is set or reset as specified by the SIM instruction.
V_{CC}	+5 volt supply.
V_{SS}	Ground Reference

TABLE 1. INTERRUPT PRIORITY, RESTART ADDRESS. AND SENSITIVITY

Name	Priority	Address Branched To (1) When Interrupt Occurs	Type Trigger
TRAP	1	24H	Rising edge AND high level until sampled
RST 7 5	2	3CH	Rising edge (latched).
RST 6 5	3	34H	High level until sampled
RST 5 5	4	2CH	High level until sampled
INTR	5	See Note 2	High level until sampled

NOTES.

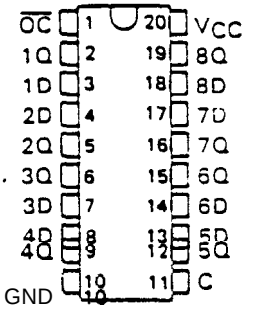
(1) The processor pushes the PC on the stack before branching to the indicated address.
(2: The address branched to depends on the instruction provided to the cpu wnen the interrupt is acknowledged.

TYPES SN54ALS373, SN54AS373, SN74ALS373, SN74AS373
OCTAL D-TYPE TRANSPARENT LATCHES WITH 3-STATE OUTPUTS

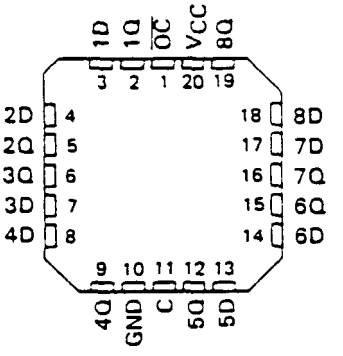
02661. APRIL 1982—REVISED DECEMBER 1983

- 8 Latches in a Single Package
- 3-State Bus-Driving True Outputs
- Full Parallel Access for Loading
- Buffered Control Inputs
- P-N-P Inputs Reduce D-C Loading on Data Lines
- Package Options Include Both Plastic end Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs
- Dependable Texas Instruments Quality and Reliabiiity

SN54ALS373, SN54AS373 . . . J PACKAGE
SN74ALS373, SN74AS373 . . . N PACKAGE
(TOP VIEW)



SN54ALS373, SN54AS373 . . . FH PACKAGE
SN74ALS373, SN74AS373 . . . FN PACKAGE
(TOP VIEW)



Description

These 8-bit latches feature three-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. They are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The eight latches of the 'ALS373 and 'AS373 are transparent D-type latches. While the enable (C) is high the Q outputs will follow the data (D) inputs. When the enable is taken low, the Q outputs will be latched at the levels that were set up at the D inputs.

A buffered output-control input ($\overline{OC}$) can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state the outputs neither load nor drive the bus lines significantly. The high-impedance third state and increased drive provide the capability to drive the bus lines in a bus-organized system without need for interface or pull-up components.

The output control $\overline{OC}$ does not affect the internal operations of the latches. Old data can be retained or new data can be entered while the outputs are off.

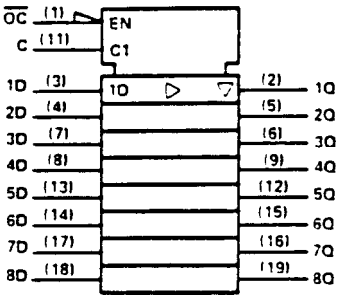
The SN54ALS373 and SN54AS373 are characterized for operation over the full miiitary temperature range of −55 °C to 125 °C. The SN74ALS373 and SN74AS373 are characterized for operation from 0 °C to 70 °C.

FUNCTION TABLE (EACH LATCH)

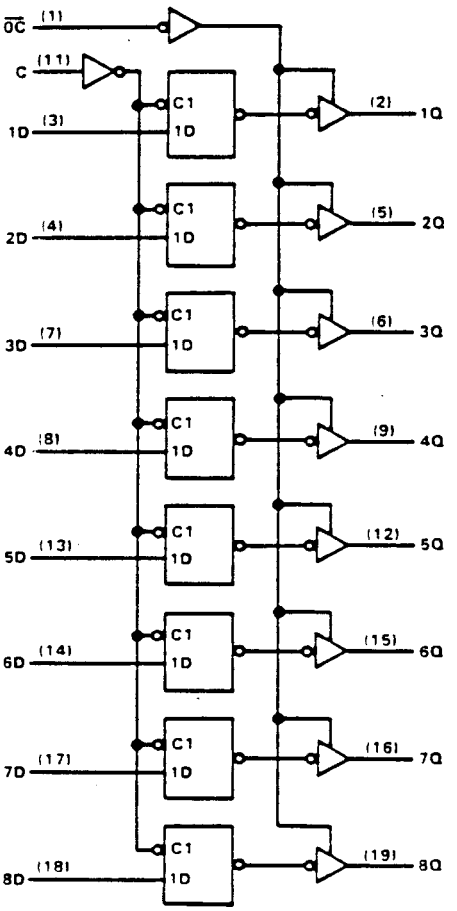
INPUTS			OUTPUT
$\overline{OC}$	ENABLE C	D	Q
L	H	H	H
L	H	L	L
L	L	X	Q_0
H	X	X	Z

TYPES SN54ALS373, SN54AS373, SN74ALS373, SN74AS373
OCTAL D-TYPE TRANSPARENT LATCHES WITH 3-STATE OUTPUTS

Io. c symbol



logic diagram (positive logic)



Pin numbers shown are for J and N packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} 7V
Input voltage 7V
Voltage applied to a disabled 3-state output 5.5V
Operating free-air temperature range: SN54ALS373, SN54AS373 . . . . . −55°C to 125°C
SN74ALS373, SN74AS373 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

8755A/8755A-2
16,384-BIT EPROM WITH I/O

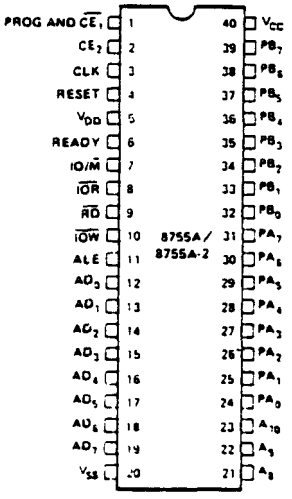
- 2048 Words × 8 Bits
- Single +5V Power Supply (V_{CC})
- Directly Compatible with 8085A and 8088 Microprocessors
- U.V. Erasable and Electrically Reprogrammable
- Internal Address Latch
- 2 General Purpose 8-Bit I/O Ports
- Each I/O Port Line Individually Programmable as Input or Output
- Multiplexed Address and Data Bus
- 40-Pin DIP

The Intel® 8755A is an erasable and electrically reprogrammable ROM (EPROM) and I/O chip to be used in the 8085A and 8088 microprocessor systems. The EPROM portion is organized as 2048 words by 8 bits. It has a maximum access time of 450 ns to permit use with no wait states in an 8085A-CPU.

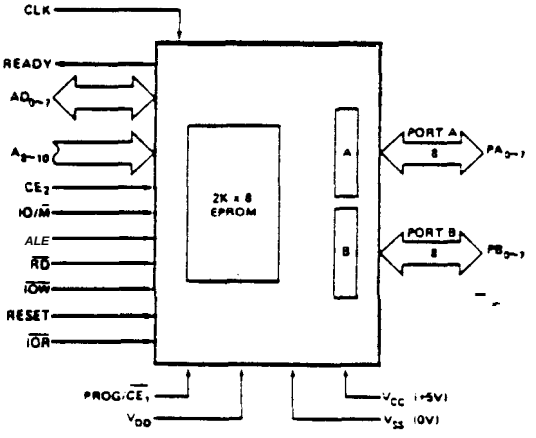
The I/O portion consists ot 2 general purpose I/O ports. Each I/O port has 8 port lines, and each I/O port line is individually programmable as input or oulput.

The 8755A-2 is a high speed selected version ot the 8755A compatible with the 5 MHz 8085A-2 and the full speed 5 MHz 8088.

PIN CONFIGURATION



BLOCK DIAGRAM



8755A FUNCTIONAL PIN DEFINITION

Symbol	Function
ALE (input)	When Address Latch Enable goes high, AD_{0-7}, IO/M, A_{8-10}, CE_2, and $\overline{CE_1}$ enter the address latches. The signals (AD, IO/M, A_{8-10}, CE) are latched in at the trailing edge of ALE.
AD_{0-7} (input/output)	Bidirectional Address/Data bus. The lower 8-bits of the PROM or I/O address are applied to the bus lines when ALE is high. During an I/O cycle. Porr A or 8 are selected based on the latched value of AD_0. If $\overline{RD}$ or $\overline{IOR}$ is low when the latched Chip Enables are actlve. the output buffers present data on the bus.
A_{8-10} (input)	These are the high order bits of the PROM address. They do not affect I/O operations.
PROG/$\overline{CE_1}$ CE_2 (input)	Chip Enable Inputs: $\overline{CE_1}$ is active low and CE_2 is active high. The 8755A can be accessed only when BOTH Chip Enables are active at the time the ALE signal latches them up. If either Chip Enable input is not active, the AD_{0-7} and READY outputs will be in a high Impedance state. $\overline{CE_1}$ is also used as a programming pin. (See section on programmlng.)
IO/$\overline{M}$ (input)	If the latched IO/$\overline{M}$ is high when $\overline{RD}$ is low. the output data comes from an I/O port. If it is low the output data comes from the PROM.
$\overline{RD}$ (input)	If the latched Chip Enables are actlve when $\overline{RD}$ goes low, the AD_{0-7} output buffers are enabled and output either the selected PROM location or I/O port. When both $\overline{RD}$ and $\overline{IOR}$ are high, the AD_{0-7} output buffers are 3-stated.
$\overline{IOW}$ (input)	If the latched Chip Enables are active. a low on $\overline{IOW}$ causes the output port pointed to by the latched value of AD_0 to be written with the data on AD_{0-7}. The state of IO/$\overline{M}$ is ignored.
CLK (input)	The CLK is used to force the READY into its htgh impedance state after it has been forced low by $\overline{CE_1}$ tow. CE_2 high, and ALE high.

Symbol	Functlon
READY (output)	READY is a 3-state output controlled by CE_2, $\overline{CE_1}$, ALE and CLK. READY is lorced low when the Chip Enables are active during the time ALE is high and rematns low until the rising eage of the next CLK. (See Figure 6
PA_{0-7} (input/output)	These are general purpose I/O pins. Their input/output direction is determined by the conlents of Dara Direction Register (DDR). Port A is selected for write operations when the Chip Enables are actlve and $\overline{IOW}$ is low and a 0 was previously latched from AD_0, AD_1. Read operation is selected bv either $\overline{IOR}$ low and active Chip Enables and AD_0 and AD_1 low or IO/$\overline{M}$ hlgh $\overline{RD}$ low. actlve Chip Enables, and AD_0 and AD_1 low
PB_{0-7} (input/output)	This general purpose I/O port is identical to Port A except that it is selected by a 1 latched from AD_0 and a 0 from AD_1.
RESET (input)	In normal operation, an input high on RESET causes all pins in Ports A and B to assume input mode (clear DDR register).
$\overline{IOR}$ (input)	When the Chip Enables are actlve. a tow on $\overline{IOR}$ will output the selected I/O port onto the AD bus $\overline{IOR}$ low performs the same function as the combination of IO/$\overline{M}$ htgh and $\overline{RD}$ low. When $\overline{IOR}$ is not used in a system, $\overline{IOR}$ should be tied to V_{CC} ("1"
V_{CC}	+5 volt supply.
V_{SS}	Ground Reference.
V_{DD}	V_{DD} is a programmlng voltage. and must be tied to +5V when the 8755A is being read. For programmlng. a high voltage is supplied with V_{DD} = 25V. typical See section on programmlng.

8203
64K DYNAMIC RAM CONTROLLER

- Rovides All **Signals** Necessary to Control 64K **(2164)** and **16K (2117, 2118)** Dynamic **Memories**
- Directly Addresses and Drives Up to 64 **Devices** Without External Drivers
- **Provides** Address Multiplexing and **Strobes**
- Rovides a Refresh **Timer** and a Refresh **Counter**
- **Provides Refresh/Access** Arbitration
- **Internal Clock** Capability with **the** 8203-1 and the 8203-3
- Fully Compatible with Intel[a] **8080A, 8085A, iAPX** 88, and **iAPX** 86 Family Microprocessors
- Decodes CPU Status for Advanced Read **Capability** In **16K** mode with the **8203-1** and the **8203-3.**
- Provides System Acknowledge and **Transfer** Acknowledge Signals
- Refresh Cycles May be Internally or **Externally** Requested (For Transparent Refresh)
- Internal Series **Damping Resistors** on **All** RAM Outputs

e Intel[a] 8203 is a **Dynamic** Ram System Controller **designed** to **provide** all **signals** necessary to use 2164.2118 2117 **Dynamic RAMs in** microcomputer systems. The 8203 **provides multiplexed** addresses and address **codes,** refresh **logic, refresh/access arbitration.** Refresh cycles can be started **internally** or externally. The **203-1** and the **8203-3** support an **internal** crystal **oscillator** and Advanced Read Capability. The **8203-3** is a 85% V_{CC} **rt.**

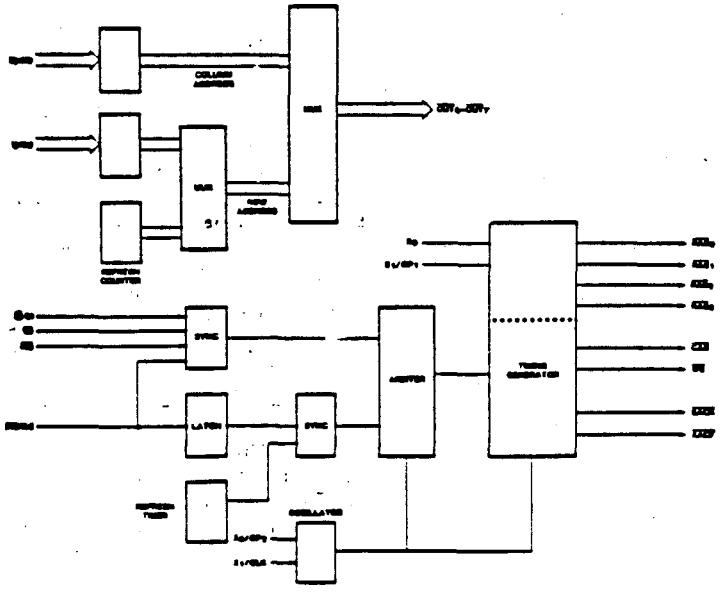


Figure 1. 8203 Block Diagram

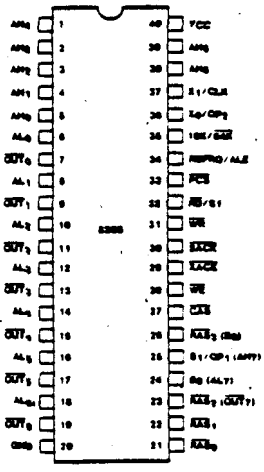


Figure 2. Pin Configuration

JULY 1982
ORDER NUMBER: 210444-002

Table 1. Pin **Descriptions**

Symbol	Pin No.	Type	Name and Function
AL_0	8	I	Addreaa **Low: CPU address** Inputs ured to generate memory row **address.**
AL_2	8	I	
	10	I	
AL_3	12	I	
AL_4	14	I	
AL_5	18	I	
AL_6	18	I	
AH_0	5	I	**Address High:** CPU address Inputs ured to generate memory column **address.**
AH_1	4	I	
AH_2	3	I	
AH_3	2	I	
AH_4	1	I	
AH_5	39	I	
AH_6	38	I	
B_0/AL_7	24	I	Bank Select **Inputs:** Used to **gate** the **appropriate** RAS **output** for a memory cycle. B_1/OP_1 **option** used to **select** the Advanced Read Mode. (Not **available in** 84K mode.) See Figure 5. When **in 64K** RAM Mode. **pins** 24 and 25 operate **as** the AL_7 and AH7 **address inputs.**
$B_1/OP_1/AH_7$	25	I	
$\overline{PCS}$	33	I	Protected **Chip Select:** Used to enable the memory read and **write** Inputs. Once a cycle **is** started. **it will** not **abort** even **if** $\overline{PCS}$ **goes inactive** before cycle completion.
$\overline{WR}$	31	I	**Memory Write Request.**
$\overline{RD}/S1$	32	I	**Memory** Road **Request:** S1 functton used in Advanced Read mode selected by OP_1 **(pin 25).**
REFRQ/ ALE	34	I	**External Refresh Request:** ALE **function** used **in** Advanced Read mode. selected by OP_1 **(pin** 25).
$\overline{OUT}_0$	7	O	**Output** of tho **Multiplexer:** There outputs are **designed** to **drive** the addresses **of** the **Dy**namtc RAM array. (Note that the $\overline{OUT}_{0-7}$ **pins** do not **require** Inverters or **drivers** for proper **operation.)**
$\overline{OUT}_1$	9	O	
$\overline{OUT}_2$	11	O	
$\overline{OUT}_3$	13	O	
$\overline{OUT}_4$	15	O	
$\overline{OUT}_5$	17	O	
$\overline{OUT}_6$	10	O	
	28	O	**Write** Enable: **Drives** the Wnte Enable **inputs of** the **Dynamic RAM array.**
$\overline{CAS}$	27	O	Column **Address** Strobe: **This output is used to latch** the Column **Address into** the Dynamtc RAM array

Symbol	Pin No.	Typo	Name and Function
$\overline{RAS}_0$	21	O	Row Addreaa Strobe: Used to **latch the** Row Address **into the** bank of **dynamic RAMs. select ed** by the 8203 Bank **Select pins** (B_0, B_1/OP_1) In **64K mode.** only $\overline{RAS}_0$ and $\overline{RAS}_1$ are **avail**able: **pin** 23 **operates** as $\overline{OUT}_7$ and **pin** 28 **operates** as the B_0 bank select **input.**
$\overline{RAS}_1$	22	O	
$\overline{RAS}_2/\overline{OUT}_7$	23	O	
$\overline{RAS}_3/B_0$	28	I/O	
$\overline{XACK}$	29	O	**Transfer** Acknowledge: **This output is** a strobe **indicating** valid data durtng a read cycle **or data written** durtng a **write cycle** $\overline{XACK}$ can be used to latch **valid data from** the RAM **array.**
$\overline{SACK}$	30	O	**System** Acknowledge: **This** output **indicates** the **beginning of** a memory access cycle. It **can** be used **as** an advanced **transfer** acknowledge to **eliminate wait states.** (Note. If a **memory access** request **is** made durtng a **refresh cycle,** $\overline{SACK}$ **is delayed until** $\overline{XACK}$ **in** the memory **access cycle).**
X_0/OP_2	36	I/O	**Oscillator Inputs:** These **inputs** are **designed** for a quartz crystal to control the frequency of the **oscillator.** If X_0/OP_2 **is shorted** to **pin** 40 (V_{CC}) or **if** X_0/OP_2 18 connected to $+12V$ through **a 1KΩ resistor** then X_1/CLK **becomes** a TTL **input** for an **external** clock. (Note: Crystal modal for the **8203-1** and the **8203-3 only).**
X_1/CLK	37	I/O	
16K/$\overline{64K}$	35	I	Mode **Select: This** Input **selects 16K** mode (2117, 2118) or **64K** mode **(2164).** Pins **23-26** change functton based on **the** mode of **operation.**
V_{CC}	40		Power Supply: **+5V.**
GND	20		Ground.

Functional Description

The 8203 provides a complete dynamic RAM **controller** for microprocessor systems as well as **expansion** memory boards. All of the necessary control **signals** are **provided** for 2164.2118 and 2117 **dynamic** RAMs.

The 8203 has two modes, one for 16K **dynamic** RAMs and one for **64Ks.** controlled by pin 35.

MOS
LSI

TMS2716
2048-WORD BY 8-BIT ERASABLE PROGRAMMABLE READ-ONLY MEMORIES

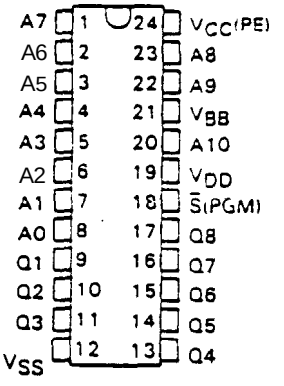
DECEMBER 1979 - REVISED OCTOBER 1983

- 2048 X 8 Organization
- All Inputs and Outputs Fully TTL Compatible
- Static Operation (No Clocks, No Refresh)
- Performance Ranges:

	ACCESS TIME (MAX)	CYCLE TIME (MIN)
TMS2716-30	300 ns	300 ns
TMS2716-45	450 ns	450 ns

- 3-State Outputs for OR-Ties
- N-Channel Silicon-Gate Technology
- 8-Bit Output for Use in Microprocessor-Based Systems
- Low Power. . . 315 mW (Typical)

TMS2716 . . . JL PACKAGE
(TOP VIEW)



PIN NOMENCLATURE	
A0-A10	Addresses
Q1-Q8	Data Out
$\overline{S}$(PGM)	Chip Select (Program)
V_{BB}	−5-V Supply
V_{CC}(PE)	+5-V Supply (Program Enable)
V_{DD}	+12-v Supply
V_{SS}	0 v Ground

description

The TMS2716 is an ultra-violet light-erasable, electrically programmable read-only memory. It has 16.384 bits organized as 2048 words of 8-bit length. The device is fabricated using N-channel silicon-gate technology for high-speed and simple interface with MOS and bipolar circuits. All inputs (including program data inputs) can be driven by Series 74 circuits without the use of external pull-up resistors and each output can drive one Series 74 or 74LS TTL circuit without external resistors. The TMS2716 guarantees 250 mV dc noise immunity in the low stare. Data outputs are three-state for OR-tying multiple devices on a common bus. The TMS2716 is plug-in compatible with the TMS2708 and the TMS27L08. Pin compatible mask programmed ROMs are available for large volume requirements.

This EPROM is designed for high-density fixed-memory applications where fast turn arounds and/or program changes are required. It is supplied in a 24-pin dual-in-line cerpak (JL suffix) package designed for insertion in mounting-hole rows on 600-mil (15,2 mm) centers. It is designed for operation from 0°C to 70°C.

operation (read model

address (A0-A10)

The address-valid interval determines the device cycle time. The 11-bit positivelogic address is decoded on-chip to select one of 2048 words of 8-bit length in the memory array. A0 is the least-significant bit and A10 most-significant bit of the word address.

chip select, program [$\overline{S}$ (PGM)]

When the chip select is low, all eight outputs are enabled and the eight-bit addressed word can be read. When the chip select is high. all eight outputs are in a high-impedance state.

program

In the program mode, the chip select feature does not function as pin 18 inputs only the program pulse. The program mode is selected by the V_{CC}(PE) pin. Either 0 V or +12 V on this pin will cause the TMS2716 to assume program cycle.

data out (Q1-Q8)

The chip must be selected before the eight-bit output word can be read. Data will remain valid until the address is changed or the chip is deselected. When deselected. the three-state outputs are in a high-impedance state. The outputs will drive TTL circuits without external components.

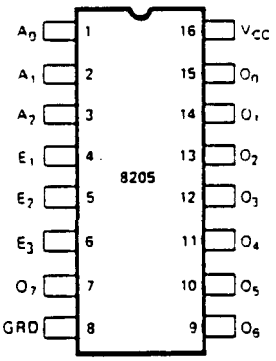
8205
HIGH SPEED 1 OUT OF 8 BINARY DECODER

- 110 Port or Memory Selector
- Simple Expansion — Enable Inputs
- High Speed Schottky Bipolar Technology — 18 ns Max Delay
- Directly Compatible with TTL Logic Circuits
- Low Input Load Current — 0.25 mA Max, 116 Standard TTL Input Load
- Minimum Line Reflection — Low Voltage Diode Input Clamp
- Outputs Sink 10 mA Min
- 16-Pin Dual In-Line Ceramic or Plastic Package

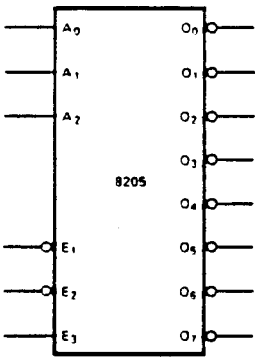
The Intel® 8205 decoder can be used for expansion of systems which utilize input ports. output ports, and memory components with active low chip select input When the 8205 is enabled, one of its 8 outputs goes "low ', lhus a single row of a memory system is selected. The 3-chip enable inputs on the 8205 allow easy system expansion For very large systems, 8205 decoders can be cascaded such that each decoder can drive 8 other decoders for arbitrary memory expansions.

The 8205 is packaged in a standard 16-pin dual in-line package. and its performance is specified over the temperature range of 0°C to +75°C, ambient. The use of Schottky barrier diode clamped transistors to obtain fast switching speeds results in higher performance than equivalent devices made with a gold diffussion process.

PIN CONFIGURATION



LOGIC SYMBOL



PIN NAMES

A_0 A_2	ADDRESS INPUTS
$\overline{E_1}$ $\overline{E_2}$ E_3	ENABLE INPUTS
$\overline{O_0}$ $\overline{O_7}$	DECODED OUTPUTS

ADDRESS			ENABLE			OUTPUTS							
A_0	A_1	A_2	E_1	$\overline{E_2}$	$\overline{E_3}$	0	1	2	3	4	5	6	7
L	L	L	L	L	H	L	H	H	H	H	H	H	H
H	L	L	L	L	H	H	L	H	H	H	H	H	H
L	H	L	L	L	H	H	H	L	H	H	H	H	H
H	H	L	L	L	H	H	H	H	L	H	H	H	H
L	L	H	L	L	H	H	H	H	H	L	H	H	H
H	L	H	L	L	H	H	H	H	H	H	L	H	H
L	H	H	L	L	H	H	H	H	H	H	H	L	H
H	H	H	L	L	H	H	H	H	H	H	H	H	L
X	X	X	H	X	X	H	H	H	H	H	H	H	H
X	X	X	X	H	X	H	H	H	H	H	H	H	H
X	X	X	X	X	H	H	H	H	H	H	H	H	H

*

intel

8155/8156/8155-2/8156-2
2048 BIT STATIC MOS RAM WITH I/O PORTS AND TIMER

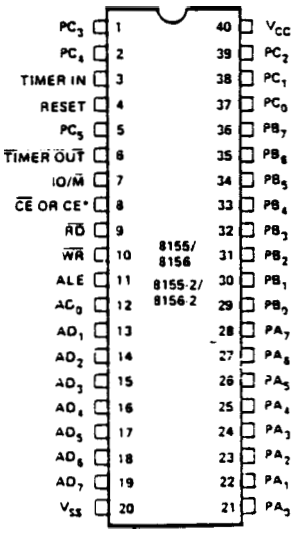
- 256 Word x 8 Bits
  Single +5V Power Supply
  Completely Static Operation
- Internal Address Latch
  2 Programmable 8 Bit I/O Ports
- 1 Programmable 6-Bit I/O Port
- Programmable 14-Bit Binary Counter1 Timer
- Compatible with 8085A and 8088 CPU
- 8 Multiplexed Address and Data Bus
- 40 Pin DIP

The 8155 and 89156 are RAM and I/O chips to be used in the 8085A and 8088 microprocessor systems. The RAM portion is designed with 2048 static cells organized as 256 x 8. They have a maximum access time of 400 ns lo permit use with no wait states in 8085A CPU. The 8155-2 and 8156-2 have maximum access times of 330 ns for use with the 8085A-2 and the full speed 5 MHz 8088 CPU.

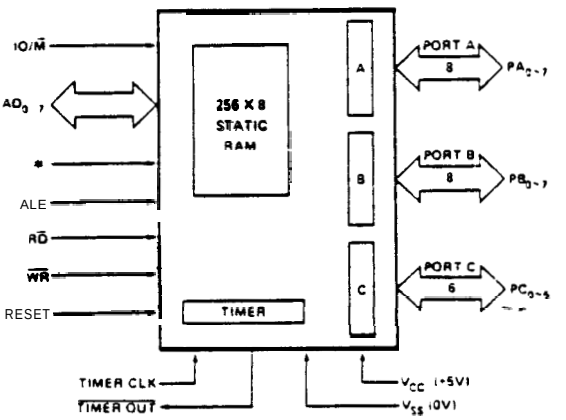
The I/O portion consists of three general purpose I/O ports. One of the three ports can be programmed to be status pins, thus allowing the other two ports to operate in handshake mode.

A 14-bit programmable counter/timer is jalso included on chip to provide either a square wave or terminal count pulse for the CPU system depending on timer mode.

PIN CONFIGURATION



BLOCK DIAGRAM



*: 8155/8155-2 = $\overline{CE}$, 8156/8156-2 = CE

81551'8156 PIN FUNCTIONS

Symbol	Function
RESET (input)	Pulse provided by the 8085A to initialize the system (connect to 8085A RESET OUT. Input high on this line resets the chip and initializes the three I/O ports to input mode. The width of RESET pulse should typically be two 8085A clock cycle times.
AD_{0-7} (input)	3-state Address/Data lines that Interface with the CPU lower 8-bit Address/Data Bus. The 8-bit address is latched into the address latch inside the 3155156 on the falling edge of ALE. The address can be either for the memory section or the I/O section depending on the IO/$\overline{M}$ Input. The 8-bit data is either written into the chip or read from the chip, depending on the $\overline{WR}$ or $\overline{RD}$ input signal.
CE or $\overline{CE}$ (input)	Chip Enable: On the 8155. this pin is $\overline{CE}$ and is ACTIVE LOW. On the 8156, this pin is CE and is ACTIVE HIGH.
$\overline{RD}$ (input)	Read control. Input low on this line with the Chip Enable active enables and AD_{0-7} buffers. If IO/$\overline{M}$ pin is low. the RAM content will be read out to the AD bus. Otherwise the content of the selected I/O port or command/status registers will be read to the AD bus.
$\overline{WR}$ (input)	Write control: Input low on this line with the Chip Enable active causes the data on the Address/Data bus to be written to the RAM or I/O ports and command/status register depending on IO/$\overline{M}$.

Symbol	Function
ALE (input)	Address Latch Enable: This control signal latches both the address on the AD_{0-7} lines and the stare of the Chip Enable and IO/$\overline{M}$ into the chip at the falling edge of ALE.
IO/$\overline{M}$ (input)	Selects memory if low and 1/0 and command/status registers if high
PA_{0-7} (8) (input/output)	These 8 pins are general ouroose I/O pins. The in/out direction is selectea by programming the command register
PB_{0-7} (8) (input/output)	These 8 pins are general ouroose I/O pins. The in/out direction is selected by programming the command register
PC_{0-5} (6) (input/output)	These 6 pins can function as either input port. output port, or as control signals for PA and PB. Programming is done through the command register. When PC_{0-5} are used as control signals, they will provide the following: PC_0 — A INTR (Port A Interrupt) PC_1 — $\overline{ABF}$ (Port A Buffer Full, PC_2 — $\overline{A\ STB}$ (Port A Strobe PC3 — $\overline{B}$ INTR (Port 9 Interrupt PC_4 — $\overline{B\ BF}$ (Port B Buffer Full) PC5 — $\overline{B}$ STB (Port B Strooe)
TIMER IN (input)	Input to the counter-timer
$\overline{TIMER\ OUT}$ (output)	Timer output. This output can be either a square wave or a oulse depending on the timer mode.
V_{CC}	+5 volt supply
V_{SS}	Grc ınd Reference.

MOS
LSI

TMS2114, TMS2114L
1024-WORD BY 4-BIT STATIC RAMS

DECEMBER 1979 - REVISED AUGUST 1983

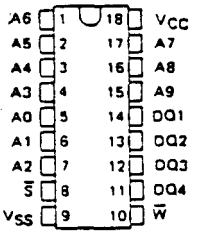
- Previously Called TMS4045/TMS40L45
- 1024 X 4 Organization
- Single +5-V Supply
- High Density 300-mil (7.62 mm) 18-Pin Package
- Fully Static Operation (No Clocks. No Refresh. No Timing Strobe)
- 4 Performance Ranges:

	ACCESS TIME (MAX)	READ OR WRITE CYCLE (MINI
TMS2114-15, TMS2114L-15	150 ns	150 ns
TMS2114-20, TMS2114L-20	200 ns	200 ns
TMS2114-25, TMS2114L-25	250 ns	250 ns
TMS2114-45, TMS2114L-45	450 ns	450 ns

- 400-mV Guaranteed DC Nolse Immunity with Standard TTL Loads - No Pull-up Resistors Required
- Common I/O Capability
- 3-State Outputs and Chip Select Control for OR-Tie Capability
- Fan-Out to 2 Series 74. 1 Series 74S, or 8 Series 74LS TTL Loads
- Low Power Dissipation

	MAX (OPERATING)
TMS2114	550 mW
TMS2114L	330 mW

TMS2114, TMS2114L . . . NL PACKAGE
(TOP VIEW)



PIN NOMENCLATURE	
A0 - A9	Addresses
DQ1 - DQ4	Data In/Data Oul
S̄	Chip Select
VCC	+6-V Supply
VSS	Ground
W̄	Write Enable

dascriptlon

This series of static random-access memories is organized as 1024 words of 4 bits each. Static design results in reducing overhead costs by elimination of refresh-clocking circuitry and by simplification of timing requirements. Because chis series is fully static. chip select may be tied low to further simplify system timing. Output data is always available during a reed.cycle.

All inputs and outputs are fully compatible with Series 74. 74S or 74LS TTL. No pull-up resistors are required. This 4K Static RAM series is manufactured using TI's reliable N-channel silicon-gate technology to optimize the cost/performance relationship.

The TMS2114/2114L series is offered In the 18-pin duel-in-line plastic (NL suffix) package designed for insertion in mounting-hole rows on 300-mrl (7.62 mm) centers. The series is guaranteed for operation from 0°C to 70°C.

MOS
LSI

TMS4116
16,384-BIT DYNAMIC RANDOM-ACCESS MEMORY

OCTOBER 1977 – REVISED MAY 1982

- 16,384 X 1 Organization
- 10% Tolerance on All Supplies

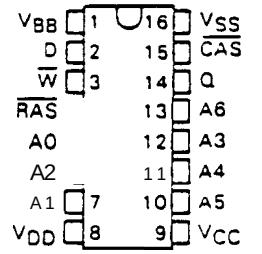
  All Inputs Including Clocks TTL-Compatible

  Unlatched Three-State Fully TTL-Compatible Output
- 3 Performance Ranges:

	ACCESS TIME ROW ADDRESS (MAX)	ACCESS TIME COLUMN ADDRESS (MAX)	READ OR WRITE CYCLE (MINI	READ. MODIFY-WRITE CYCLE (MIN)
TMS4116-15	150 ns	100 ns	375 ns	375 ns
TMS4116-20	200 ns	135 ns	375 ns	375 ns
TMS4116-25	250 ns	165 ns	410 ns	515 ns

- Page-Mode Operation for Faster Access Time
- Common I/O Capability with "Early Write" Feature
- Low-Power Dissipation
  - Operating 462 mW (Max)
  - Standby 20 mW (Max)
- 1-T Cell Design, N-Channel Silicon-Gate Technology
- 16-Pin 300-Mil (7.62 mm) Package Configuration

TMS4116 . . . NL PACKAGE
(TOP VIEW)



PIN NOMENCLATURE	
A0-A6	Addresses
CAS	Column Address Strobe
D	Data Input
Q	Data Output
RAS	Row Address Strobe
VBB	–5-V Power Supply
VCC	+5-V Power Supply
VDD	+12-V Power Supply
VSS	Ground
W	Write Enable

description

The TMS4116 series is composed of monolithic high-speed dynamic 16,384-bit MOS random-access memories organized as 16,384 one-bit words, and employs single-transistor storage cells and N-channel silicon-gate technology.

All inputs and outputs are compatible with Series 74 TTL circuits including clocks: Row Address Strobe RAS (or R) and Column Address Strobe CAS (or C). All address lines (A0 through A6) and data in (D) are latched on chip to simplify system design. Data out (Q) is unlatched to allow greater system flexibility.

Typical power dissipation is less than 350 milliwatts active and 6 milliwatts during standby (V_{CC} is not required during standby operation). To retain data. only 10 milliwatts average power is required which includes the power consumed to refresh the contents of the memory.

The TMS4116 series is offered in a 16-pin dual-in-line plastic (NL suffix) package and is guaranteed for operation from 0°C to 70°C. Package is designed for insertion in mounting-hole rows on 300-mil (7.62 mm) centers.

MOS
LSI

TMS4164, SMJ4164
65,536-BIT DYNAMIC RANDOM-ACCESS MEMORY

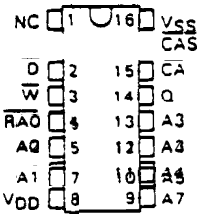
JULY 1980 - REVISED OCTOBER 1983

- 65.536 X 1 Organization
- Single +5-V Supply (10% Tolerance)
- JEDEC Standardized Pin-Out in Dual-In-Line Packages
- Upward Pin Compatible with TMS4116 (16K Dynamic RAM)
- First Military Version of 64K DRAM
- Available Temperature Ranges:
  - M . . . −55°C to 125°C
  - S . . . −55°C to 100°C
  - E . . . −40°C to 85°C
  - L . . . 0°C to 70°C
- Long Refresh Period . . . 4 milliseconds
- Low Refresh Overhead Time . . . As Low As 1.8% of Total Refresh Period
- All Inputs, Outputs, Clocks Fully TTL Compatible
- 3-State Unlatched Output
- Common I/O Capability with "Early Write" Feature
- Page-Mode Operation for Faster Access
- Low Power Dissipation
  - Operating . . . 125 mW (TYP)
  - Standby . . . 17.5 mW (TYP)
- Performance Ranges (S, E, L Temperature Ranges):

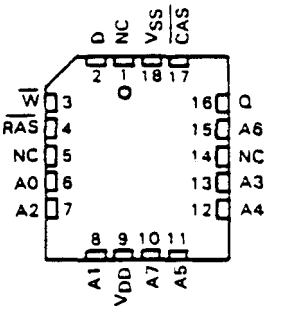
	ACCESS TIME ROW ADDRESS (MAX)	ACCESS TIME COLUMN ADDRESS (MAX)	READ OR WRITE CYCLE (MINI	READ-MODIFY-WRITE CYCLE IMINI
'4164-12	120 ns	70 ns	230 ns	260 ns
'4164-15	150 ns	85 ns	260 ns	285 ns
'4164-20	200 ns	135 ns	326 ns	345 ns

- New SMOS (Scaled-MOS) N-Channel Technology

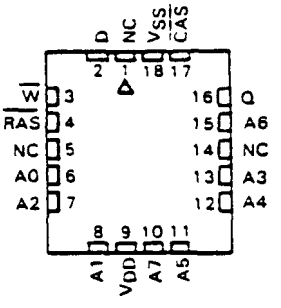
TMS4164 . . . NL PACKAGE
SMJ4164 . . . JD PACKAGE
(TOP VIEW)



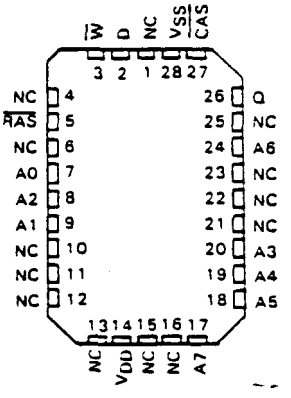
TMS4164 . . . FPL PACKAGE
(TOP VIEW)



SMJ4164 . . . FG PACKAGE
(TOP VIEW)



SMJ4164 . . . FE PACKAGE
(TOP VIEW)



PIN NOMENCLATURE	
AO-A7	Address Inputs
$\overline{CAS}$	Column Address Strobe
D	Data-In
NC	No-Connection
Q	Data-Out
$\overline{RAS}$	Row Address Strobe
V_{DD}	+5-V Supply
V_{SS}	Ground
$\overline{W}$	Write Enable

description

The '4164 is a high-speed. 65,536-bit, dynamic random-access memory, organized as 65.536 words of one bit each. It employs state-of-the-art SMOS (scaled MOS) N-channel double-level polysilicon gate technology for very high performance combined with low cost and improved reliability.

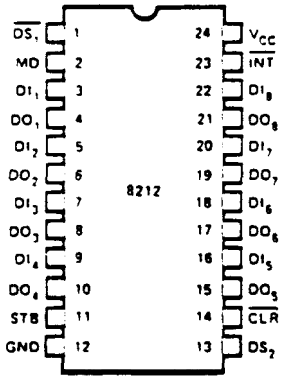
8212
8-BIT INPUT/OUTPUT PORT

- Fully Parallel 8-Bit Data Register and Buffer
- Service Request Flip-Flop for Interrupt Generation
- Low Input Load Current — .25mA Max.
- Three State Outputs
- Outputs Sink 15mA
- 3.65V Output High Voltage for Direct Interface to 8008, 8080A, or 8085A CPU
- Asynchronous Register Clear
- Replaces Buffers. Latches and Multiplexers in Microcomputer Systems
- Reduces System Package Count

The 8212 input/output port consists of an 8-bit latch with 3-state output buffers along with control and device selection logic. Also included is a service request flip-flop for the generation and control of interrupts to the microprocessor.

The device is multimode in nature. It can be used to implement latches, gated buffers or multiplexers. Thus, all of the principal peripheral and input/output functions of a microcomputer system can be implemented with this device.

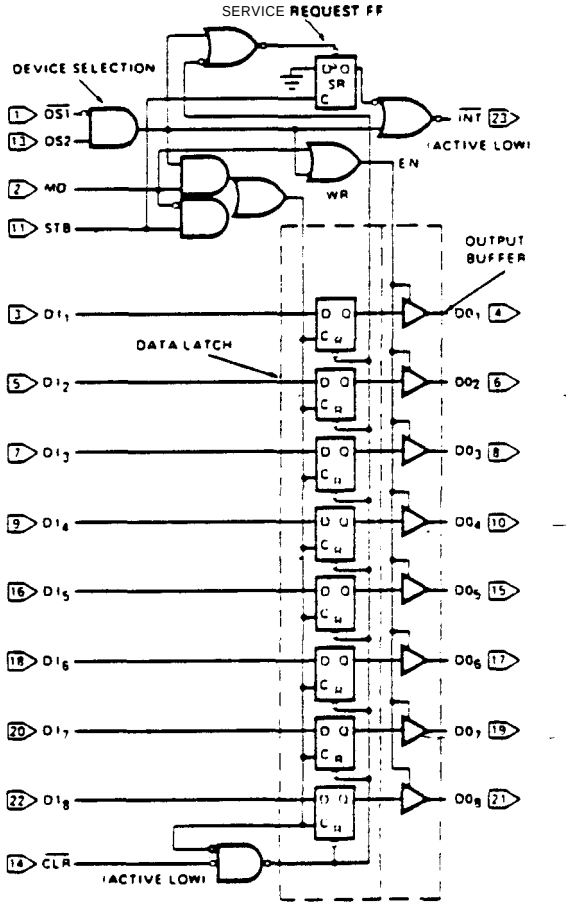
PIN CONFIGURATION



PIN NAMES

DI_1, DI_8	DATA IN
DO_1, DO_8	DATA OUT
$\overline{DS_1}$, DS_2	DEVICE SELECT
MD	MODE
STB	STROBE
$\overline{INT}$	INTERRUPT (ACTIVE LOW)
$\overline{CLR}$	CLEAR (ACTIVE LOW)

LOGIC DIAGRAM



FUNCTIONAL DESCRIPTION

Data Latch

The 8 flip-flops that make up the data latch are of a "D" type design. The output (Q) of the flip-flop will follow the data input (D) while the clock input (C) is high. Latching will occur when the clock (C) returns low.

The latched data is cleared by an asynchronous reset input ($\overline{CLR}$). (Note: Clock (C) Overrides Reset ($\overline{CLR}$).)

Output Buffer

The outputs of the data latch (Q) are connected to 3-state, non-inverting output buffers. These buffers have a common control line (EN); this control line either enables the buffer to transmit the data from the outputs of the data latch (Q) or disables the buffer, forcing the output into a high impedance state. (3-state)

The high-impedance state allows the designer to connect the 8212 directly onto the microprocessor bi-directional data bus.

Control Logic

The 8212 has control inputs $\overline{DS1}$, DS2, MD and STB. These inputs are used to control device selection, data latching, output buffer state and service request flip-flop.

$\overline{DS1}$, DS2 (Device Select)

These 2 inputs are used for device selection. When $\overline{DS1}$ is low and DS2 is high ($\overline{DS1} \cdot DS2$) the device is selected. In the selected state the output buffer is enabled and the service request flip-flop (SR) is asynchronously set.

MD (Mode)

This input is used to control the state of the output buffer and to determine the source of the clock input (C) to the data latch.

When MD is high (output mode) the output buffers are enabled and the source of clock (C) to the data latch is from the device selection logic ($\overline{DS1} \cdot DS2$).

When MD is low (input mode) the output buffer state is determined by the device selection logic ($\overline{DS1} \cdot DS2$) and the source of clock (C) to the data latch is the STB (Strobe) input.

STB (Strobe)

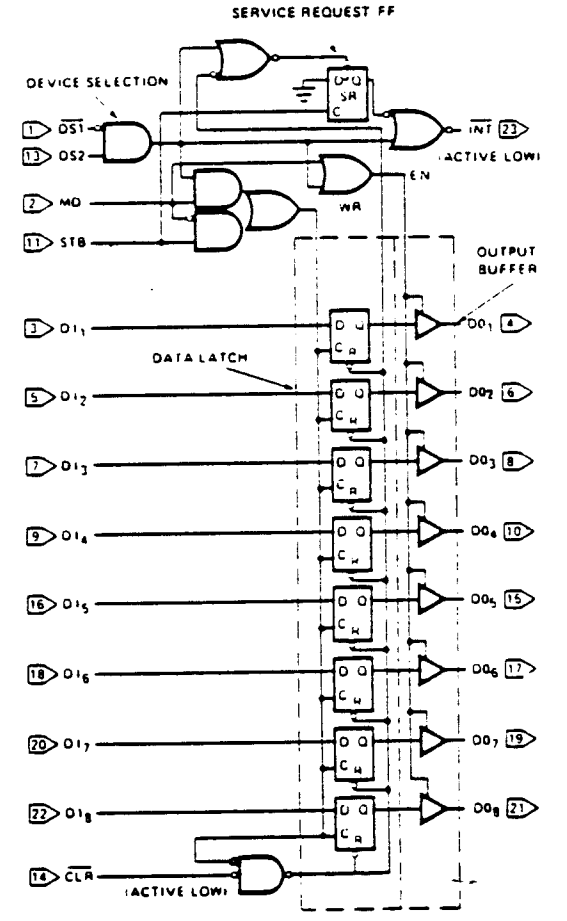
This input is used as the clock (C) to the data latch for the input mode MD = 0) and to synchronously reset the service request flip-flop (SR).

Note that the SR flip-flop is negative edge triggered.

Service Request Flip-Flop

The (SR) flip-flop is used to generate and control interrupts in microcomputer systems. It is asynchronously set by the $\overline{CLR}$ input (active low). When the (SR) flip-flop is set it is in the non-interrupting state.

The output of the (SR) flip-flop (Q) is connected to an inverting input of a "NOR" gate. The other input to the "NOR" gate is non-inverting and is connected to the device selection logic ($\overline{DS1} \cdot DS2$). The output of the "NOR" gate ($\overline{INT}$) is active low (interrupting state) for connection to active low input priority generating circuits.



STB	MD	$\overline{DS_1}$ DS_2	DATA OUT EQUALS
0	0	X	LAST STATE
1	0	X	LAST STATE
0	1	0	DATA LATCH
1	1	0	DATA LATCH
0	0	1	DATA LATCH
1	0	1	DATA IN
0	1	1	DATA IN
1	1	1	DATA IN

CLR	$\overline{DS_1}$ DS_2	STB	*SR	INT
0	0	X	1	1
0	1	X	1	1
1	1	↓	0	0
1	1	0	1	0
1	0	0	1	1
1	1	↓	1	0

*INTERNAL SR FLIP FLOP

$\overline{CLR}$ - RESETS DATA LATCH
SETS SR FLIP FLOP
(NO EFFECT ON OUTPUT BUFFER)

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