# Electrical Properties of Molybdenum Silicon Carbide Schottky Barrier Diodes

by

Sai Bhargav Naredla

Submitted in Partial Fulfillment of the Requirements

for the Degree of

Master of Science in Engineering

in the

Electrical Engineering

Program

YOUNGSTOWN STATE UNIVERSITY

May 2019

**Electrical Properties of Molybdenum Silicon Carbide Schottky Barrier Diodes**

Sai Bhargav Naredla

I hereby release this thesis to the public. I understand that this **thesis** will be made available from the OhioLINK ETD Center and the Maag Library Circulation Desk for public access. I also authorize the University or other individuals to make copies of this thesis as needed for scholarly research.

Signature:

_Sai Bhargav Naredla_, Student Date

Approvals:

_Dr. Tom Nelson Oder_, Thesis Advisor

_Dr.Jalal Jalali_, Committee Member Date

_Dr. Faramarz D. Mossayebi,_ Committee Member Date

Dr. Salvatore A. Sanders, Dean of Graduate Studies Date

**ABSTRACT**

Molybdenum (Mo) is one of the metals categorized as refractory metal due to its thermal properties. For that reason, it is very attractive for high temperature applications. This thesis covers the investigation of silicon carbide (SiC) Schottky diodes fabricated using Mo as the Schottky contact. The Mo Schottky contacts were deposited using magnetron sputtering on the n-type 4H-SiC. The temperature of the SiC substrates was varied from 25 $^{o}$C to 900 $^{o}$C. The electrical properties of the diodes were determined by current-voltage, capacitance voltage and current-voltage-temperature measurements. Structural properties of Schottky contacts deposited at different temperatures were also characterized using x-ray diffraction spectroscopy.

The results obtained reveal that the as-deposited diodes had energy barrier heights that ranged from 1.02 to 1.67 eV and ideality factors varying from 1.04 to 1.23. Contacts deposited at 600 $^{o}$C produced the optimum property consisting of a barrier height of 1.34 eV and ideality factor of 1.05. The diodes were further thermally processed by keeping them exposed to 500 $^{o}$C for 24 hours diodes in vacuum. From these, the barrier height ranging from 1.00 eV to 1.70 eV was obtained. The variation in electrical properties is explained as due to changes in crystal quality. Current voltage temperature measurements to further characterize electrical properties of diodes at different temperatures were performed. Contacts deposited at 500$^{o}$ C produced the largest Richardson's constant (A**) of 3.74 A/K-cm$^2$ and a barrier height of 1.32 eV. Changes in ideality factors and barrier heights are observed due to the formation of interfacial silicide layers. X-ray diffraction results show the formation of $MoSi_2$ and $Mo_5Si_2$.

# ACKNOWLEDGMENT

I wish to express my heart felt gratitude to my advisor Dr. Tom Nelson Oder for the assistance and support he provided to me to complete my master's program. I am very thankful for his patience, motivation, enthusiasm, and immense knowledge. His guidance helped me in all the time of performing this research and writing of the thesis. I could not have imagined having a better advisor and mentor for my master's thesis.

I would also like to thank the rest of my thesis committee: Dr. Faramarz D. Mossayebi and Dr. Jalal Jalali for their support and guidance. Their passionate participation and input were immensely instrumental in helping me successfully complete this thesis preparation. I wish also to thank Dr. Jalal Jalali and Youngstown State University for giving me an opportunity to work in the Department of Physics and Astronomy as a graduate research assistant. I also want to thank Mr. Ray Hoff, a staff in the Department of Chemistry at YSU who never hesitated to help when I needed it especially for the x-ray diffraction measurements. My special thanks to the National Science Foundation for supporting this work through grant (DMR#1428334).

Finally, I must express my very profound gratitude to my parents and to my brothers for providing me with unfailing support and continuous encouragement throughout my years of study and through the process of researching and writing this thesis. This accomplishment would not have been possible without them. Thank you.

Table of Contents

ABSTRACT ..... iii

ACKNOWLEDGMENT ..... iv

CHAPTER 1 ..... 1

1.1 Introduction ..... 1

1.2 Structure of Silicon Carbide (SiC) ..... 2

1.3 Properties of Silicon Carbide ..... 5

1.4 Doping ..... 8

1.5 Etching ..... 9

1.6 Current Status of SiC Technology ..... 10

1.7 Refractory metals ..... 11

1.8 Molybdenum (Mo) ..... 12

CHAPTER 2 ..... 15

Science of Silicon Carbide Schottky Barrier Diodes (SBD) ..... 15

2.1 Silicon Carbide Schottky Barrier Diodes ..... 15

2.2 Metal-Semiconductor contacts ..... 16

2.2.1 Ohmic Contact ..... 17

2.2.2 Schottky contact ..... 17

2.3 Theory and Operation of Schottky Barrier Diode (SBD) ..... 19

2.3.1 Forward bias and Reverse Bias of Schottky Barrier Diode (SBD) ..... 22

2.4 Conduction Mechanisms in Metal-Semiconductor Contacts ..... 23

2.4.1 Thermionic Emission ..... 23

2.4.2 Thermionic-Field Emission ..... 24

2.4.3 Field Emission ..... 24

2.5 Electrical Characterization ..... 25

2.5.1 Current-Voltage (I-V) Characterization ........ 25
2.5.2 Capacitance–Voltage (C-V) Characterization ........ 26
2.6 Molybdenum on SiC Schottky Barrier Diodes ........ 27
CHAPTER 3 ........ 29
Growth Techniques for Schottky Barrier Diode Fabrication ........ 29
3.1 Photolithography ........ 29
3.2 Magnetron Sputter Deposition ........ 31
3.3 Ohmic Contact and Schottky Contact ........ 34
3.4 Electrical Characterization ........ 37
3.4.1 Current-Voltage (I-V) Measurements ........ 37
3.4.2 C-V Measurements ........ 40
3.4.3 I-V-T Measurements ........ 41
3.5 Structural Characterization (X-ray diffraction) ........ 42
3.6 Annealing ........ 44
CHAPTER 4 ........ 45
Results ........ 45
4.1 I-V Measurements ........ 45
4.2 C-V Measurements ........ 50
4.3 I-V-T Measurements ........ 52
4.4 XRD Measurements ........ 56
CHAPTER 5 ........ 58
5.1 Conclusion ........ 58
5.2 Future Work ........ 58
References ........ 60

**LIST OF FIGURES**

Figure 1. The fundamental structure of silicon carbide ..................................................... 3

Figure 2: Crystal structure of SiC: (a) wuirtzite structure and (b) zinc blend structure . ... 3

Figure 3. Crystal structure and the of SiC polytypes: a) 3C-SiC (zinc blende structure), b) 4H-SiC (wurtzite structure), c) 6H-SiC (wurtzite structure) ............................................. 4

Figure 4: Energy gap diagram of a semiconductor. ........................................................... 6

Figure 5: Breakdown voltage versus drift region width of different substrates ................ 6

Figure 6. Uses of molybdenum in different sectors ........................................................ 13

Figure 7. Rectifying and non-rectifying plot [ref 21] ..................................................... 17

Figure 8: Energy band diagram of metal-semiconductor before contact.......................... 19

Figure 9. Energy level diagram of metal-semiconductor after contact and before equilibrium ........................................................................................................................ 20

Figure 10. Energy level diagram of metal and semiconductor at equilibrium.................. 21

Figure 11. Energy level diagram of metal-semiconductor junction (a) forward bias and (b) reverse bias ................................................................................................................. 22

Figure 12. Thermionic emission ...................................................................................... 23

Figure 13. Thermionic-field emission.............................................................................. 24

Figure 14. Field emission.................................................................................................. 25

Figure 15. I-V Plot. ........................................................................................................... 26

Figure 16. The structure of SiC (Mo/4H-SiC) ................................................................. 30

Figure 17. (a) Spin coater (b) Heater (c) Mask aligner ................................................... 31

Figure 18. Magnetron sputtering technique ..................................................................... 32

Figure 19. (a) Sputter deposition chamber (b) Metal target (c) Cathode assembly setup 33

Figure 20. Rapid thermal processor (RTP) ...................................................................... 35

Figure 21. Ohmic contact and Schottky contact illustration............................................ 36

Figure 22. (a) Sample holder (b) Heater .......................................................................... 36

Figure 23. (a) Sample mounted on the copper plate (b) Sample mounted on a copper plate with probe ........ 38

Figure 24. (a) Probe station (b) Keithley 2410 source meter ........ 39

Figure 25. (a) LCR meter (b) Sample arranged on a copper plate (c) Isolation container 40

Figure 26. I-V-T measurement setup ........ 41

Figure 27. Bragg's law sketch ........ 42

Figure 28. Sample holder ........ 43

Figure 29. Bruker X8 prospector ........ 43

Figure 30. Heater base with stainless-steel ........ 44

Figure 31. Samples mounted on heater ........ 44

Figure 32. Plot of turn-on voltages at different temperatures (26 – 900 ........ 46

Figure 33. Plot of Current-Voltage at different temperatures (26 – 900°C) ........ 47

Figure 34. Plot of change in ideality factor and barrier height at various temperatures ... 48

Figure 35. Plot of change in ideality factor and barrier height at various temperatures ... 49

Figure 36. Plot of $N_D$ versus $\varphi_B$ at different deposition temperatures ........ 51

Figure 37. Plot of $1/C^2$ versus V at different deposition temperatures ........ 51

Figure 38. I-V-T plot of samples 26 °C - 900 °C ........ 53

Figure 39. Richardson plot of sample deposited at 500 °C ........ 54

Figure 40. XRD pattern of samples deposited from 26 °C to 900 °C ........ 56

Figure 41. XRD pattern of samples deposited from 26 °C to 900 °C annealed at 500 °C for 24 hours ........ 57

**LIST OF TABLES**


Table 1: Comparison between 4H- and 6H-SiC [ref 1]. .................................................... 5

Table 2: Electrical properties of different substrate materials ........................................... 7

Table 3: Important properties of refractory metals .......................................................... 12

Table 4: Rectifying contacts on n-type 4H-SiC ................................................................ 18

Table 5: Molybdenum Schottky contacts on SiC ............................................................. 28

Table 6: Chemical mixtures for cleaning SiO2 [ref 29] .................................................. 30

Table 7: Ohmic Contact Parameters ................................................................................. 34

Table 8: Schottky contact parameters ............................................................................... 35

Table 9: Turn-on voltages of samples deposited at different temperatures ...................... 46

Table 10: Electrical Characteristics at different temperatures before annealing ............. 48

Table 11: Electrical characteristics of samples annealing at 500 $^{o}$C for 24 hours ............ 49

Table 12: Doping Concentration and Barrier Height at different Temperatures .............. 50

Table 13: Richardson Constant and Barrier height of different samples .......................... 54

Table 14: Ideality factor and barrier height of 500 $^{o}$C I-V-T sample…………….............55

# CHAPTER 1

## 1.1 Introduction

Silicon carbide (SiC), is a wide band gap semiconductor material that holds extremely good properties such as a wide band gap (3.24 eV), a high breakdown voltage (3.0 mV/cm), a high thermal conductivity (3.7 W/cm $^{o}$C), lower intrinsic carrier concentration, a good oxide formation ability These lead to operations at elevated temperatures (up to 1200 $^{o}$C) [1]. These properties of SiC make it attractive for making devices for high power, high frequency, high temperature, and high radiation tolerant applications.

Silicon (Si) is the most common material used in electronics because of its elemental properties which are ideal in a large array of circumstances. However, there are limitations with Si, such as the process of miniaturization can prove to make silicon unreliable to a high temperature environment. During this process, the potential to withstand desired operating conditions has been a big concern. This means that devices that use silicon are not favorable to operate at temperatures exceeding 250 $^{o}$C. However operating above this temperature can be possible with SiC due to its large bandgap. It has been shown to function properly at 350 - 600 $^{O}$C and have higher breakdown voltages ranging from 300-1200 V because of its stronger bonds [1]. SiC is a promising material to provide an advantage when high temperature and high voltage devices are necessary. It even holds the potential to make devices more compact by incorporating smaller builds and faster operations. Exceptional properties of SiC brought its presence commercially available in the Schottky barrier diode (SBD), field-effect transistor (FET), and other semiconductor devices used in high power and high switching applications. The band gap

(3.24) makes SiC to be a promising candidate in the fabrication of sensors that are used in high temperature and high radiation environments like satellites and nuclear power plants. SiC have shown profound impact on rectifiers that are used in inverters, solar power modules, traction control devices, and power factor correction boost converters which can improve switching frequency with larger power output leading to a higher efficiency gain [1-2].

It is clearly evident that SiC has found a wide array of industrial applications. Such applications include, heat exchangers, furnaces, wear resistant covers, slide bearings, rocket nozzle, geothermal wells, and heating elements. SiC can even be found in the semiconductor support material due to its high standards of hardness, thermal shock resistance [3]. Even as an indirect bandgap semiconductor, SiC has replaced GaP (gallium phosphide) in some applications in optical sector devices. Insensitivity of SiC to longer spectrum regions and less dark current levels at high temperatures ($10^{-11}$ A at -1 V, 200 $^{o}$C) finds an attractive place in the fabrication of photo diodes desired to detect ultra violet wavelengths up to 299 nm [3].

**1.2 Structure of Silicon Carbide (SiC)**

SiC crystal is the compound of Si and carbon (C) having a good bonding energy which allows to form a very strong tetrahedral covalent bond. 4 atoms of silicon combine with 1 carbon atom to form SiC compound and the spacing between silicon-silicon, silicon-carbon is 3.04 Å and 1.89 Å respectively, as shown in Figure 1 [3]. Moissanite is the natural form of SiC exhibit one dimensional polymorphism which are available in 250 crystalline forms known as polytypes and difference between them is the stacking

sequence in a certain direction. The most frequently used polytypes are 3C, 4H, 6H, 15R, the numbers 3,4, 6, 15 represent layers required to form atomic geometry (periodicity) and cubic (C), hexagonal (H), rhombohedral (R) represent a crystallographic classification. 3C-SiC is cubic which holds zinc blende structure whereas 4H, 6H, 15H possess wurtzite structure (hexagonal), as shown in Figure 2 and the stacking sequence is ABCB, ABCACB for 4H and 6H, as shown in Figure 3. Presently, 4H, 6H are commercially available in bulk form and epitaxial layer [4, 5].

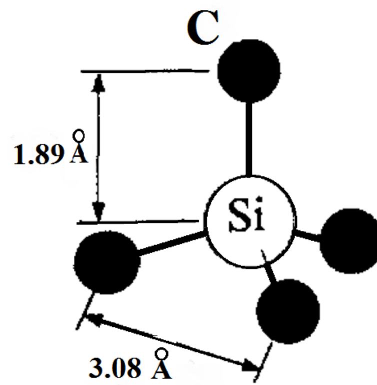



**Figure 1.** The fundamental structure of silicon carbide (SiC) [ref 6].

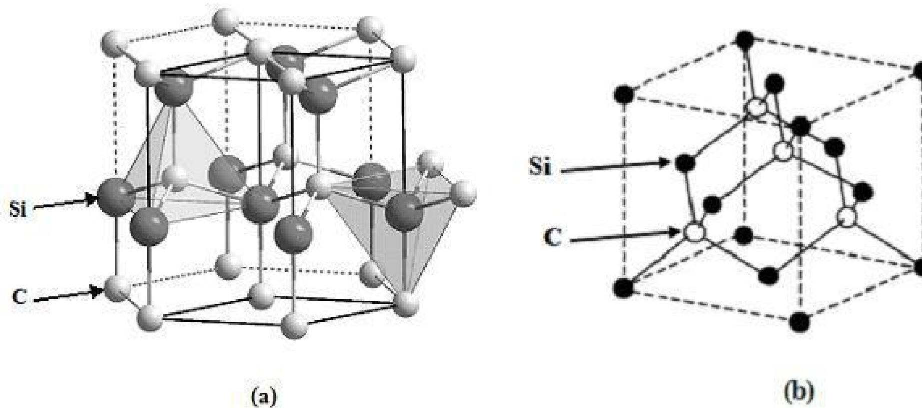



**Figure 2:** Crystal structure of SiC: (a) wuirtzite, (b) zinc blend structure [ref 7, 8].

SiC structure plays an important role in atomic environment which alters the electron transport configuration. 4H-SiC has an equal number of wurtzite and zinc blend bonds while 6H-SiC has 33.3 percent of hexagonal and 67.77 percent of cubic bond which forms a decent atomic geometry [5].

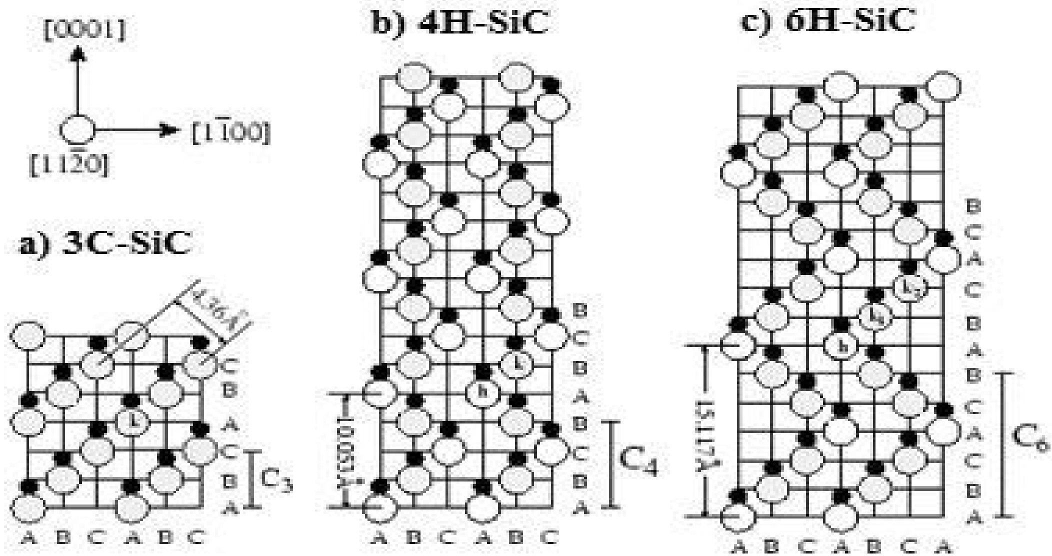



**Figure 3.** Crystal structure and the of SiC polytypes: a) 3C-SiC (zinc blende structure), b) 4H-SiC (wurtzite structure), c) 6H-SiC (wurtzite structure) [ref 9]

4H-iC is chosen over 6H-SiC as a base material in device fabrication because of its higher electron mobility (800 $cm^2/V$-s), high anisotropic mobility which is greater than 6H-SiC at optimum ionization potentials and forms thinner drift regions at certain doping levels operates in low on-state resistance which resulted in lower conduction losses, as shown in Table 1. As the devise gets thinner there is less place for minority charge carriers (less reverse recovery loss) leading to better power handling capability and better efficiency.

**Table 1:** Comparison between 4H- and 6H-SiC [ref 13]

| Property | 4H-SiC | 6H-SiC |
| --- | --- | --- |
| Energy Bandgap (eV) | 3.26 | 3.0 |
| Intrinsic Carrier-Concentration ($cm^{-3}$) | $10^{-7}$ | $10^{-5}$ |
| Electron mobility at $N_D$=$10^{16}$ ($cm^2$/V-s) | ∥ c-axis: 800<br>⊥ c-axis: 800 | ∥ c-axis: 60<br>⊥ c-axis: 400 |
| Dopant Ionization Energy (MeV) | 45 | 50 |

### 1.3 Properties of Silicon Carbide

Wide bandgap materials (SiC, GaN, and AlN) are a suitable option for electronic applications because of its moderate bandgap. Energy gap or bandgap plays an important role in the selection of a device material and it is defined as an energy gap difference between conduction level ($E_c$) and valence level ($E_v$), as shown in Figure 4. Conductors have no bandgap because their energy levels overlap whereas in the semiconductors band gap depends on energy level difference and the number of electrons in conduction band decides resistance. The band gap of SiC depends on polytype, among these 4H-SiC has higher band gap compared to other polytypes and has three times greater band gap than silicon. Additionally, a low doping ionization energy and high mobility of carriers in a certain direction (c-axis) makes it to sustain high temperatures, as shown in Table 1 [10]. As the width of drift layer increases, breakdown voltage of substrate (Si, 4H-SiC, 3C-SiC, GaN) increases, as shown in Figure 5.

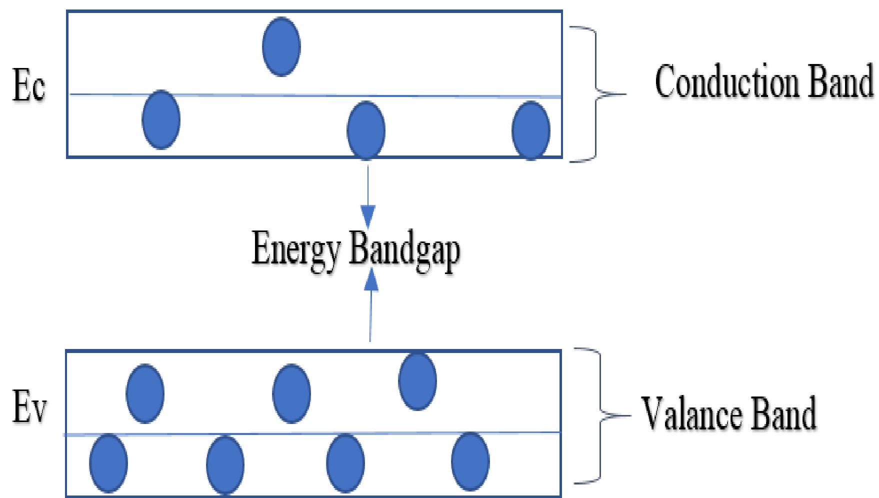



**Figure 4:** Energy gap diagram of a semiconductor.

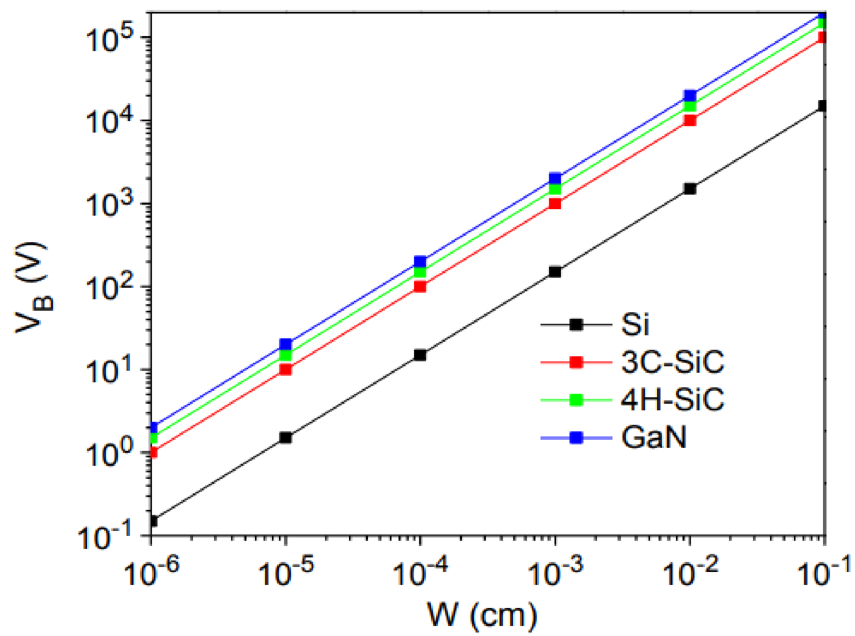



**Figure 5:** Breakdown voltage versus drift region width of different substrates. [Ref 16]

**Table 2:** Electrical properties of different substrate materials [from ref 10].

| Property | Si | GaAs | 4H-SiC | 6H-SiC | GaN |
|---|---|---|---|---|---|
| Bandgap, $E_g$ (eV) | 1.12 | 1.4 | 3.26 | 3.02 | 3.4 |
| Electron mobility $\mu_n$ at 300K, ($cm^2$/V-s) | 1500 | 8500 | 800 | 470 | 900 |
| Hole mobility, $\mu_p$ at 300K ($cm^2$/V-s) | 450 | 400 | 115 | 101 | 50 |
| Breakdown Elec Field, $E_c$ (MV/cm) | 0.3 | 0.4 | 3 | 3.2 | 3.3 |
| Thermal Conductivity, $\Theta$ (W/cm °C) | 1.5 | 0.5 | 3.7 | 4.9 | 1.3 |
| Max. Operating temperature (°C) | 300 | 400 | 1200 | 1000 | 600 |
| Sat. electron drift velocity, $V_s$ ($10^7$ cm/s) | 1 | 1 | 2 | 2 | 2.5 |
| Dielectric constant, $\varepsilon_r$ | 11.9 | 13.1 | 10.3 | 10.3 | 9 |

4H-SiC has a saturation electron drift velocity of $2 \times 10^7$ cm/s, which is 2 times greater than Si that engenders a high channel current which can influence frequency. SiC has higher breakdown electric field 3 MV/cm which is 3 times greater than Si attaining a thinner epitaxial drift layer and resulting to have higher breakdown voltages. SiC has high thermal conductivity (3.7 W/cm °C), as shown in Table 2, where it can sustain higher voltages and currents eliminating the use of heat sinks. Low dielectric constant exhibit low parasitic capacitance which helps the device to operation at high frequencies [10].

## 1.4 Doping

Doping is a process of adding impurities to a material to enhance the electrical properties of the material. Shockley patented the concept of ion implantation in 1956 after Pfann introduced the concept of diffusion in 1954 [11]. SiC is doped using three methods, they are thermal diffusion, controlled epitaxial doping and ion implantation method. Thermal diffusion is a traditional method which involves high temperature annealing and it is considered as an incompetent process of doping. In case of electronics, high conductivity and low resistance are the major factors required to attain low power loss conditions. Trivalent and pentavalent impurities are used to dope SiC, nitrogen and phosphorous are used to dope SiC for n-type while aluminum and boron are used as p-type dopants. a Generally, activation level plays a crucial role in doping. . Ion implantation and epitaxial controlled doping are both important for SiC device fabrication, but ion implantation is a good choice for selective doping because of high controllability of ion energy and a low temperature for affordable cost. Epitaxial controlled doping is incorporated with no lattice damage which is inexpensive [11].

M. A. Capano studied the effect of dopants on 4H-SiC and 6H-SiC in 1998 and he noticed the damage of lattice structure with high beam ions and annealed samples at different temperatures (1500-1700 $^{o}$C) to heal lattice structure damage. 4H-SiC is doped with boron annealed at 1750 $^{o}$C for 40 min in a non-reactive gas environment (argon) covered the electrically active lattice spots to eliminate (compensated) the lattice damage. Diffusion involves elevated temperature but it is considered as an efficient process to achieve complete activation [12].

### 1.5 Etching

Micro patterning of SiC involves etching, it is a process of removing layers from substrate. Etching can be performed in two ways, one is the wet etching which involves chemicals and the other is dry etching engages plasma. Wet etching is done using strong acids and chemicals which is inexpensive while dry etching is done using plasma. Wet etching is categorized into two types one is chemical etching and the other is electro-chemical etching [13]. Micro patterning methods involve oxidation on the surface of the substrate resulting in a chance of surface defects. SiC single crystal is chemically inert, very difficult to proceed with wet etching because it involves molten salts such as potassium hydroxide (KOH), sodium hydroxide (NaOH) and elevated temperatures (600 $^{o}$C) in alkaline mixtures. Additionally, it is very difficult to control line width, so it is productive to use plasma etching such as reactive ion etching (RIE), electron cyclotron resonance (ECR), inductive coupled etching (ICP) to get higher etching rates greater than 1000 Å/min. Reactive ion etching involving chlorine ($Cl_2/SiCl_4/O_2$) is used for 6H-SiC with silicon dioxide mask (etch rates of 1900 Å/min) [14].

Generally reactive ion etching is used for 4H-SiC and 6H-SiC because of optimum etching rates (100's of Å/min) and selectivity. 3C-SiC, 4H-SiC 6H-SiC is etched using fluorinated plasmas ($SF_6/O_2$, $CF_4/O_2$, $NF_3/O_2$, $CHF_3/O_2$) with a $H_2$ (hydrogen) additive to avoid micro masking effect (residue formation), to attain high etch rate, anisotropic profile, good selectivity and residue free environment [14,15].

## 1.6 Current Status of SiC Technology

Current technology is in need of devices that are small and fast to fulfil the purpose of high power, high temperature, high frequency, radiation resistant applications. Rough environments are creating a situation to look for materials that can compensate existing failures. Si devices commercialized in 1957 are still in the market serving the need of various applications and performance. The impact of Si devices are limited to lower operating conditions which are facing failures at elevated temperatures. Wide bandgap semiconductor material like SiC devices operating at high voltage and high power (> 600 V) and gallium nitride (GaN) devices operating at low voltage low power applications (< 600V) made their presence in the market serving the need of faster switching speeds and able to withstand high junction temperatures. Presently, silicon-based devices can be operated below 175 $^{o}$C due to its intrinsic properties of material pertaining certain limited junction potential [16].

SiC finds an attractive place in power semiconductor modules due to its balance in terms of electrical conductivity, mechanical stability, chemical inertness and radiation resistant applications. Currently 6-inch SiC wafers are available in the market fabricated by Cree Incorporate and Infineon [16]. SiC devices are available in increased voltage and increased current ratings according to application, recently a 1000 V SiC based metal oxide semiconductor field effect transistor was released into the market for the application of hybrid electric vehicles (HEV) replacing a traditional 900 V silicon battery providing reliability and adequate voltage margin. Usage of SiC TO-247-4 pin package resultant common source inductor < 5nH parasitic inductance which can be operated at 1200-1700 V, 400 ampere eliminated the use of heat sinks and provides weight/size

reduction. A 600 V 1- 40 ampere 4H-SiC Schottky diodes are released into the market by CREE Incorporate exhibiting superior dynamic performance in serving the need of reduced switching losses, power factor correction in switch mode power supplies, elimination of active and passive snubber circuits attaining gains [16].

In the year 2013, GeneSiC semiconductors have introduced a high temperature Schottky rectifiers with an on-state drop of 1.90 eV at 100 Amperes to drive 15 V IGBT gate drivers [17]. SiC devices are employed in high speed motor drive systems, high-performance solid-state transformers, solid state fault current limiter, circuit breakers, grid systems, industrial motor drives, power module, packaging for power quality improvement and system stability enhancement [18].

### 1.7 Refractory metals

Refractory metals are a group of materials which possess exceptional qualities such as, corrosion resistance, wear and abrasion resistance, thermal shock resistant, improved electrical, thermal properties, higher melting points and hardness. The group of metals with unique properties are tungsten (W), molybdenum (Mo), tantalum (Ta), rhenium (Re), titanium (Ti) and the most common property among these is higher melting points [14]. Refractory metals find an active role in an industrial sector like processing of molten metals such as glass, incandescent lamp filaments with high resistance to thermal shock, cutting tools, acts as radiation shield to chemical catalysts, electronics, aerospace, military, nuclear power stations, stainless steel, gyroscopes, mining and drilling mechanical parts [19].

**Table 3:** Important properties of refractory metals

| Metal | Density ($gm/cm^3$) | Melting Point ( $^{O}C$ ) | Electrical Conductivity %IACS | Electrical Resistivity (microhms -cm) | Thermal Conductivity ( $Cal/^{O}C$ ) |
|---|---|---|---|---|---|
| W | 19.3 | 3410 | 31 | 5.5 | 0.39 |
| Re | 21.04 | 3180 | 9.3 | 19.1 | 0.17 |
| Ta | 16.6 | 2996 | 13.9 | 13.5 | 0.13 |
| Mo | 10.22 | 2610 | 34 | 5.7 | 0.35 |
| Ti | 4.5 | 1668 | 5.5 | 42 | 0.052 |

The most common factor among these materials is higher melting points which allows the material to operate at high temperature and hostile environments. Electrical conductivity of refractory metals is high according to international annealed copper standards (IACS) and resistivity differs due to bandgap, as shown in Table 3. Thermal conductivity of refractory metals are high which is a good sign for high temperature and high-power applications [19].

### 1.8 Molybdenum (Mo)

Molybdenum (Mo) is a transition metal with outstanding properties such as high electrical conductivity ($2\times10^{7}$ S/m), low coefficient of thermal expansion ($5.0 \times 10^{-6}$/ K), high thermal conductivity (140 W/mK), resistant to thermal shock, high oxidation resistance, and chemical inertness [16]. Higher melting points (2610 $^{o}C$) of Mo making it

attractive for high temperature, high power application devices. Mo holds better electrical conductivity and thermal stability among all refractory metals which clears its way into electrical and electronic applications, in turn making equipment to handle harsh environments. Mo is used in stainless steel to facilitate steel free from oxidation and corrosion resistant at high temperatures [19, 20].

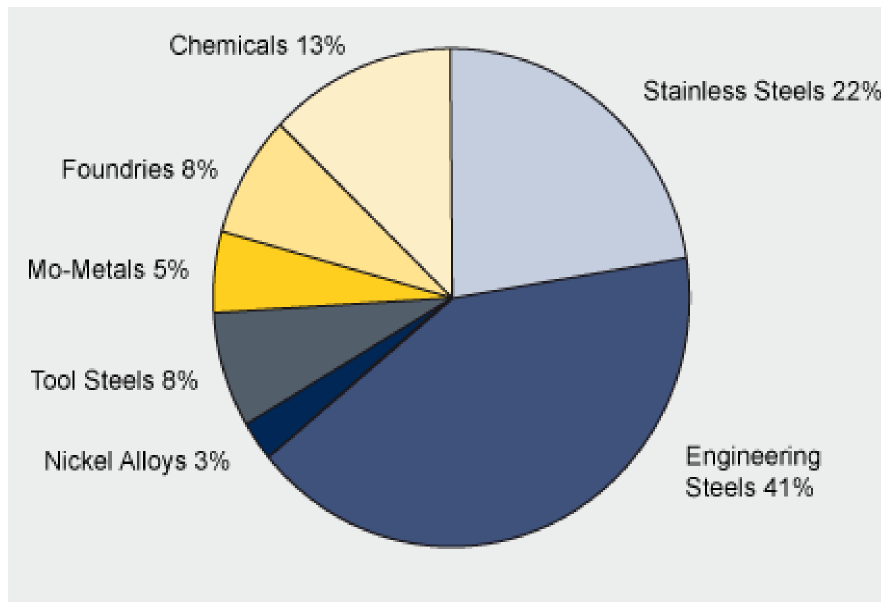



**Figure 6.** Uses of molybdenum in different sectors [ref 16]

Mo plays an important role in production of thin films, integrated circuits which can be operated at elevated temperatures and acts as a wear resistant. Chemical inertness of molybdenum makes it to be a good candidate as contact material for thin film solar cells. Mo is used as a back contact material (diffusion barrier) for Cu (In, Ga) $Se_2$ (CIGS) solar cells, providing good adhesion and chemical inertness [9]. Mo as a Schottky contact on SiC resulted in a decent ideality factor (< 1.1), barrier height (1.04 eV) at room

temperature (26 $^{o}$ C). The Mo Schottky barrier diode provides a greater operating stability at high temperatures [18]. Micro-electro mechanical system devices like relays, switches, micro mirror arrays use molybdenum to alter its operation and promotes reliability, as shown in Figure 6 [21, 22].

# CHAPTER 2

## Science of Silicon Carbide Schottky Barrier Diodes (SBD)

### 2.1 Silicon Carbide Schottky Barrier Diodes

SiC based Schottky barrier diodes has an attractive place in power semiconductor devices employed for low forward voltage, fast switching speeds, larger breakdown voltages, a Table electrical conductivity over a wide range of operating temperatures. Low junction capacitance, low forward voltage in SBD eliminates the use of heat sinks, reduces conduction losses and improves the gain in on-state. Trials to improve silicon based Schottky barrier diode characteristics leads to increase its weight/size ratios, not addressing the issues of efficiency [23]. The metal-semiconductor combinations were invented in 1874 by F. Braun while dealing with radio wave detectors. Radio waves were also used in between 1939-1945 (Second World War) as microwave detectors and frequency converters [19]. Walter H. Schottky investigated metal point contacts and replaced unreliable contact with metallic thin film, later in 1938 diode was named after him. In the year 1950, the metal semiconductor investigation took a step back due to the development of p-n junction devices, later in 1960's planner process came in to the picture to successfully predict interface conditions between metal-semiconductors, the invention of computers accelerated the investigation of Schottky contacts in need of fast switching devices. Hunger to feed the challenges faced by technological inventions in the $19^{th}$ century paved a way to improved metal semiconductor devices which can be operated at elevated power, frequency applications. Commercially first SiC Schottky

barrier diode came into the market in 2001 with 4”, 6” wafers and grossed $48 M by 2008 [23, 24].

SiC Schottky barrier diodes are employed in switch mode power supplies (SMPS) for real power factor correction control in boost converters lowering switching losses approximately 60 percent more than traditional silicon diodes eliminating the use of the snubber circuit [24]. Lower switching losses allow the system to operate at a high frequency and elimination of complex circuits reduces size, promotes efficiency. A 600 V 40 ampere SiC Schottky barrier diodes were released into the market by Cree Inc. had passed the reverse recovery charge failures, promoting low junction capacitance, low $Q_{rr}$ which helped in reducing switching losses in continuous conduction mode (CCM) switch mode power supplies (SMPS). SiC Schottky barrier diodes are used in solar modules to stop reverse current and protect against discharge during dusk. They are used in detectors, sensors, mixers and other high frequency, low conduction loss applications [24].

## 2.2 Metal-Semiconductor contacts

Metal semiconductor contact plays an important role in an electron transport configuration between semiconductor and metal and they are categorized into two types:

1. Ohmic contact (non-rectifying contact)
2. Schottky contact (rectifying contact)

### 2.2.1 Ohmic Contact

Ohmic contact is a low resistance junction between metal and semiconductor to provide a linear current conduction, as shown in Figure 7. Ohmic contact is formed when the work function of a metal is less than n-type semiconductor work function. Least resistant contact depends on impurity concentration, if the doping concentration is high ($N_D > 10^{18}$) then contact acts as ohmic, usually ohmic contact is deposited on the back side of SiC which is on a highly doped surface in the fabrication of Schottky barrier diode [25].

$\Phi_M < \Phi_S$ (Ohmic) $\Phi_{M}$ = Work function of metal

$\Phi_M > \Phi_S$ (Schottky) $\Phi_{S}$ = Work function of semiconductor

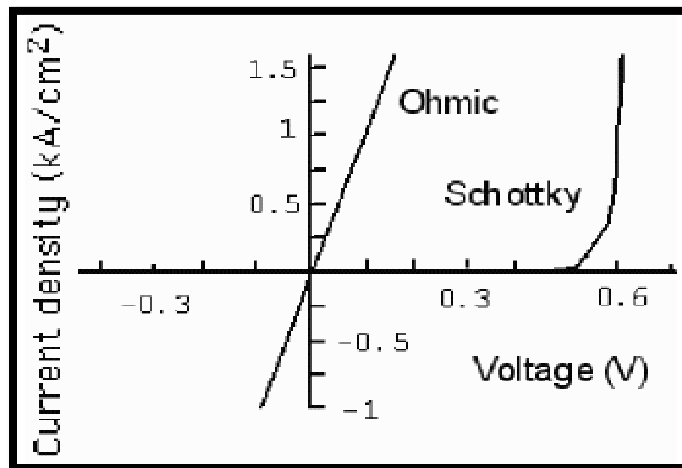



**Figure 7.** Rectifying and non-rectifying plot [ref 21]

### 2.2.2 Schottky contact

Schottky contact is formed when the work function of metal is larger than the semiconductor work function, usually larger bandgap metals (Pt, Ni, Au, Pd) are chosen to attain a higher barrier height and thermal stability which are important factors for

Schottky contact. Schottky contact is formed on the front side of SiC [26]. 4H-SiC is preferred over 6H-SiC because of its higher and more isotropic electronic mobility.

**Table 4:** Rectifying contacts on n-type 4H-SiC [from ref 26 and 27]

| 4H-SiC Face | Metal | SBH (eV) IV | CV | Ideality Factor(n) | Comments |
|---|---|---|---|---|---|
| Si | Ti | 0.56 | | 1.26 | As deposited |
| Si | Ti | 0.91 | | 1.10 | RTA 300 °C/5min |
| Si | Ti | 1.18 | | 1.08 | RTA 500 °C/5min |
| Si | Ti | 1.19 | | 1.23 | RTA 700 °C/5min |
| Si | Ti | 0.77 | | 1.46 | RTA 900 °C/5min |
| Si | Ti | 0.95 | 1.17 | 1.02~0.20 | |
| C | Ti | 1.16 | 1.30 | 1.02~0.20 | |
| Si | Ti | 0.80 | | 1.15 | As deposited |
| Si | Ti/Au | 1.17 | | 1.09 | |
| Si | Ti | 1.17 | | 1.06 | |
| Si | TiW | 1.22 | 1.23 | 1.05 | As deposited |
| Si | TiW | 1.18 | 1.19 | 1.10 | 500 °C/30min |
| Si | Ni2Si | 1.40 | | <1.10 | |
| Si | Cu | 1.60 | | <1.10 | As deposited |
| Si | Cu | 1.80 | | <1.10 | 500 °C/5min |
| Si | Au | 1.73 | 1.85 | 1.02~0.20 | |
| C | Au | 1.80 | 2.10 | 1.02~0.20 | |
| Si | Ni | 1.62 | 1.75 | 1.02~0.20 | |
| C | Ni | 1.60 | 1.90 | 1.02~0.20 | |
| Si | Ni | 1.30 | | 1.21 | Measured at 20 °C |
| Si | Ni | 1.40 | | 1.12 | Measured at 122 °C |
| Si | Ni | 1.50 | | 1.12 | Measured at 225 °C |
| Si | Ni | 1.59 | | 1.05 | |
| Si | Ni | 1.35 | | 1.05 | |
| Si | Ni | | 1.70 | 1.07 | |
| Si | Ni | 1.63 | | 1.10 | |
| Si | Pt | 1.36 | | 1.01 | |

Titanium deposited on 4H-SiC at deposition temperature 200 $^{o}$C showed a decent ideality factor of 1.04 and a potential barrier height 1.13 eV [28].

**2.3 Theory and Operation of Schottky Barrier Diode (SBD)**

Work function (Φ) plays an important role in choosing a metal and it is defined as energy required to remove an electron from the surface of the conductor, to a point outside the conductor where the kinetic energy of an electron is zero. $\Phi_{M,}$ $\Phi_S$ are used to denote metal-semiconductor work function [28]. Rectifying contact (Schottky contact) is formed when the metal work function exceeds semiconductor work function ($\Phi_M > \Phi_S$), ohmic contact is formed when the semiconductor work function dominates the metal work function ($\Phi_M < \Phi_S$). Semiconductor material can be doped to change the fermi level and it is characterized by electron affinity ($\chi_s$) defined as the energy gap difference between conduction level and vacuum level. Metal-semiconductor interface is described using energy band diagram Figure 8 [29].

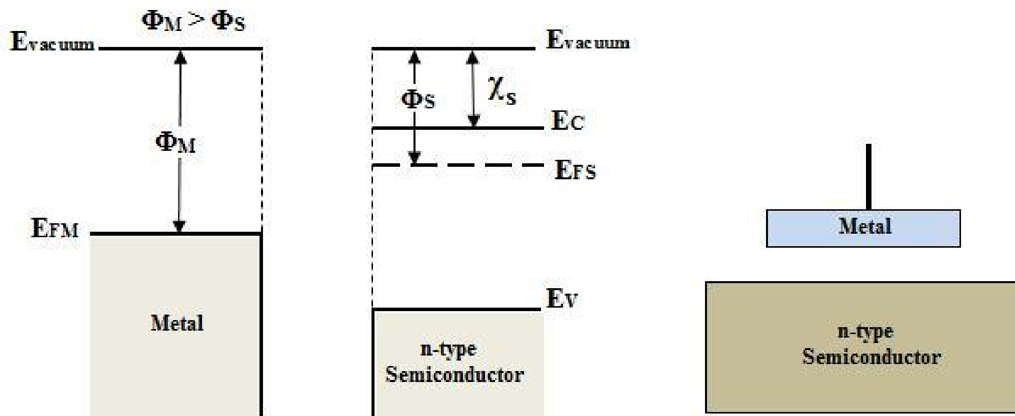



**Figure 8:** Energy band diagram of metal-semiconductor before contact [ref 29].

Electron affinity of the semiconductor does not depend on doping concentration and it is assumed to be unchanged even after the vacuum level matching. There are more than 250 polytypes are available in SiC, 4H-SiC and 6H-SiC are more suitable options for electronic devices because of their higher isotropic electron mobility. Fermi levels of the metal-semiconductor comes close after contact formation [1]. Potential barrier height can be estimated using equation (2.1).

$$\Phi_B = \Phi_M - \chi_S \qquad (2.1)$$

As metal and semiconductor move close to form a contact, the high energy electrons from the conduction band of semiconductor moves to metal, bending the junction to lineup fermi levels of metal and semiconductor. Fermi levels lineup to form a potential barrier known as equilibrium contact potential $V_{BI}$ given by equation (2.2). At equilibrium, the total current across the junction is zero, as shown in Figure 9 [28].

$$V_{BI} = \Phi_M - \Phi_S \qquad (2.2)$$

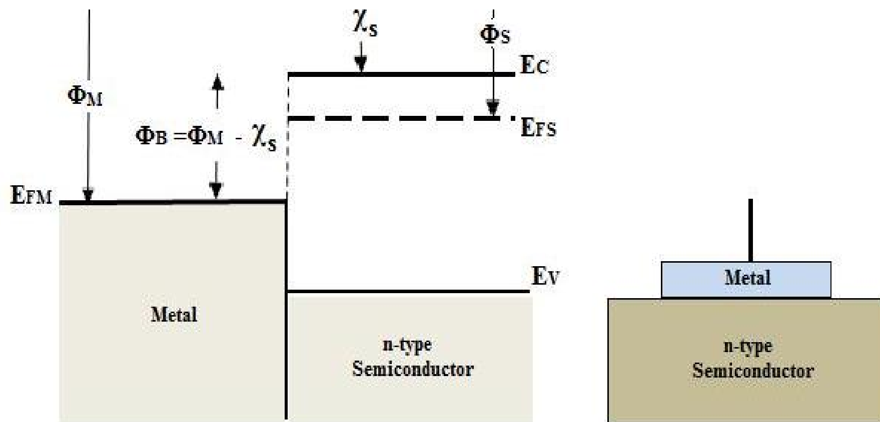



**Figure 9.** Energy level diagram of metal-semiconductor after contact and before equilibrium [ref 29].

As the electrons move from semiconductor to metal, leaving a positive charge due to ionized donor atoms behind, provides a negative field and lowers the band edges of semiconductor. At this point the system is said to be in equilibrium forming a depletion region across metal-semiconductor junction, as shown in Figure 10. The width of the depletion region is given by equation (2.3).

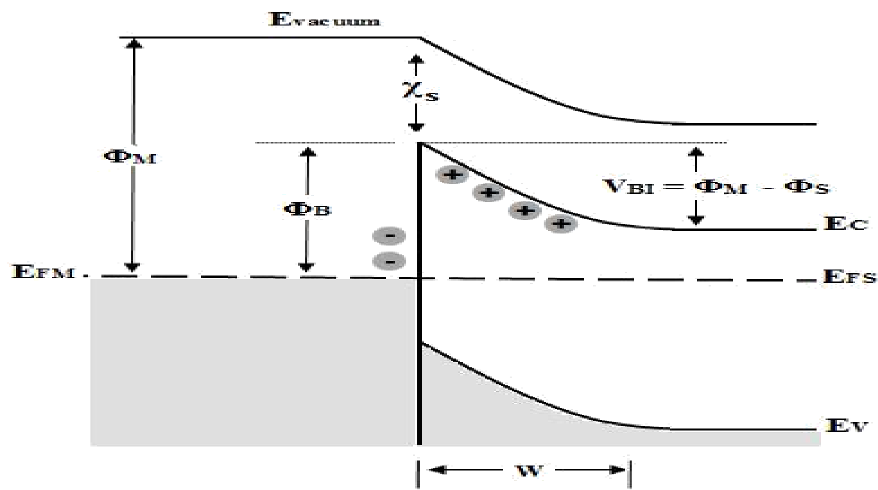



**Figure 10.** Energy level diagram of metal and semiconductor at equilibrium [ref 28].

$$W = \sqrt{\frac{2\epsilon\,(V_{bi}-V_a}{N_D}} \tag{2.3}$$

Where,

W = Width of the depletion region.

$V_{bi}$ = Built-in potential

$V_a$ = Voltage applied

$\epsilon$ = Permittivity of substrate

$N_d$ = Impurity concentration or doping concentration

### 2.3.1 Forward bias and Reverse Bias of Schottky Barrier Diode (SBD)

In case of the forward bias condition, a voltage ($V_a$) is applied across the junction, then the fermi energy level of metal is brought down to the fermi level of semiconductor making the width of depletion region small, allowing electrons to flow over a potential barrier to the metal as shown in Figure 11 (a). A large current flows during the forward bias condition. In case of reverse bias condition, a negative voltage is applied to the metal side which creates an impact on built-in voltage making the width of the potential barrier wider [30]. The potential barrier, which doesn't allow the flow of electrons to the metal side remains unchanged so that the barrier doesn't depend on the applied voltage, limiting the flow of electrons, as shown in Figure 11.

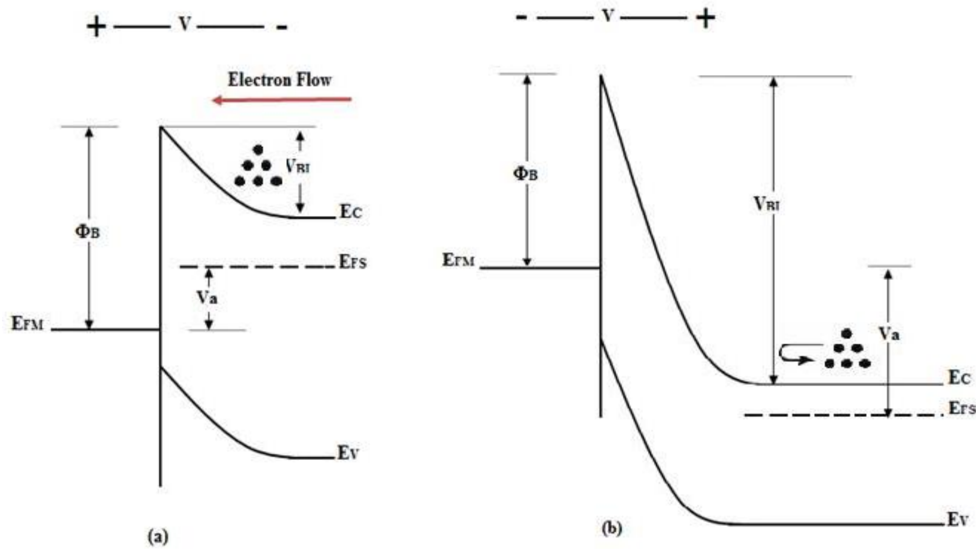



**Figure 11.** Energy level diagram of metal-semiconductor junction (a) forward bias and (b) reverse bias

## 2.4 Conduction Mechanisms in Metal-Semiconductor Contacts

There are three types of conduction mechanisms in metal-semiconductor contacts, they are:

1. Thermionic Emission
2. Thermionic-Field Emission
3. Field Emission

### 2.4.1 Thermionic Emission

Thermionic emission occurs when the potential barrier is wide and the only possible way for an electron to pass is to leap over the barrier with maximum emission. This type of emission is generally seen in rectifying contacts and the potential barrier width depends on doping concentration. The probability of tunneling is less and emission is valid for low doping ($N_D < 10^{17}$ cm$^{-3}$), as shown in Figure 12.

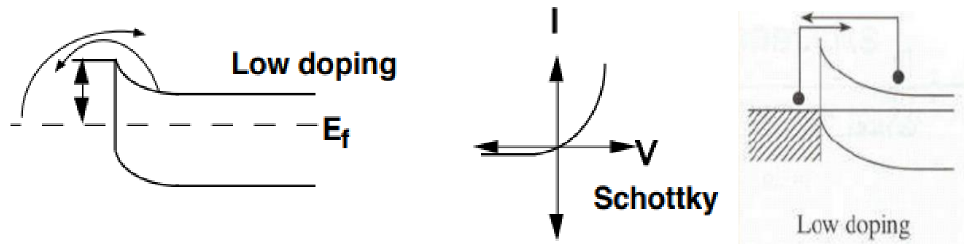



**Figure 12.** Thermionic emission

I-V relation in thermionic emission is given by

$$I_F = A\ A^*\ T^2\ e^{\frac{-q\phi_B}{kT}} \left(e^{\frac{q(V_a - IR_S)}{nkT}}\right)\left(1 - e^{\frac{q(V_a - IR_S)}{nkT}}\right) \quad (2.4)$$

$$I_F = I_0 \left(e^{\frac{qV_a}{nkT}} - 1\right) \quad (2.5)$$

$$I_0 = A\ A^*\ T^2\ e^{\frac{-q\phi_B}{kT}} \quad (2.6)$$

Where,

$I_F$ = Forward current

$A^*$ = Richardson's constant for the material

A = active area of metal contact on the semiconductor

T = the temperature of the material

$\Phi_B$ = barrier height between metal and semiconductor

$V_a$ = Voltage (under high bias $V_a >> 3kT/q$)

### 2.4.2 Thermionic-Field Emission

Thermionic field emission occurs when depletion layer is moderately narrow and valid for moderate doping ($10^{17}$ cm$^{-3}$ < $N_D$ <$10^{18}$ cm$^{-3}$), thermal energy is used by electrons to tunnel over the barrier, as shown in Figure 13.

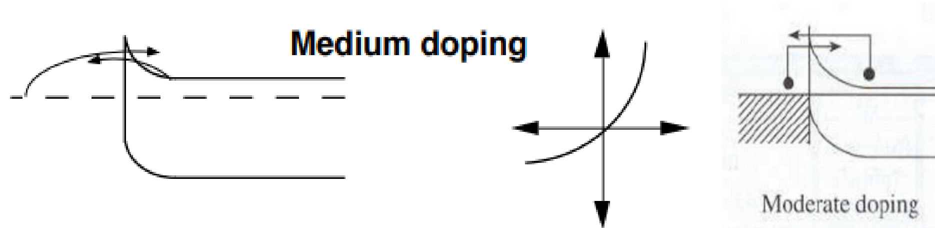



**Figure 13.** Thermionic-field emission

### 2.4.3 Field Emission

Field emission is also called as quantum mechanical tunneling, it occurs in case of heavily doped conditions ($N_D > 10^{18}$ cm$^{-3}$), tunneling occurs due to a low depletion region width and acts as ohmic, as shown in Figure 14.

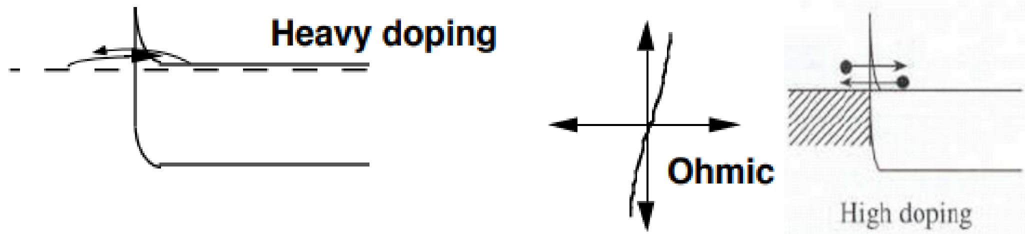



**Figure 14.** Field emission

## 2.5 Electrical Characterization

Electrical characterization of diode includes current-voltage measurements, capacitance-voltage measurements and current-voltage-temperature measurements.

### 2.5.1 Current-Voltage (I-V) Characterization

Current voltage characteristics for thermionic emission is considered for high bias conditions neglecting smaller values like series resistance.

$$I_F = I_0 \left(e^{\frac{qV_a}{nkT}}\right) \; (V_a >> 3kT/q) \tag{2.7}$$

$$I_0 = A \; A^* \; T^2 \, e^{\frac{-q\emptyset_B}{kT}} \tag{2.8}$$

Apply natural logs on both sides

$$\ln(I_F) = \ln(I_0) + \frac{q}{nkT} V_a \tag{2.9}$$

$$\ln(I_0) = \ln(A \, A^* \, T^2) - \frac{q}{kT} \emptyset_B \tag{2.10}$$

A plot of $\ln(I_F)$ against $V_a$ creates a straight line whose slope is q/nkT and $\ln(I_0)$ is the intercept obtained by extrapolating the line to $V_a$ to zero, as shown in Figure 15. Substituting values for Schottky contact cross section area A, Richardson constant $A^{**}$

and the temperature, ideality factor (n) and potential barrier height ($\Phi_B$) can be calculated.

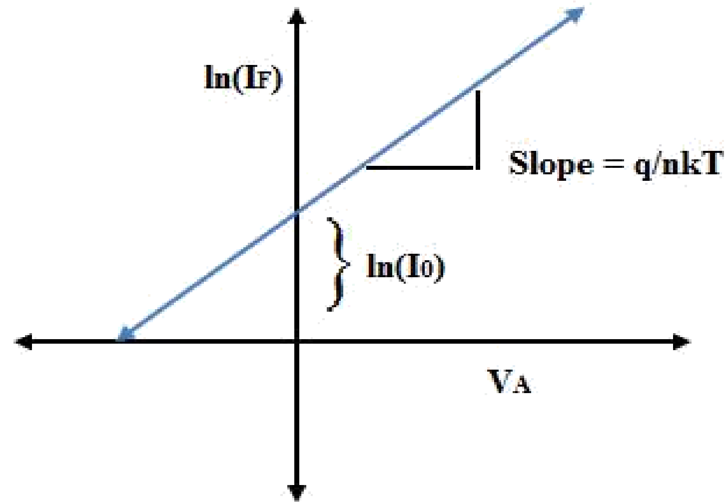



**Figure 15.** I-V Plot.

### 2.5.2 Capacitance–Voltage (C-V) Characterization

The presence of varying voltages at depletion layer creates capacitance in Schottky barrier diode and it is measured by superimposing alternating voltages at a particular frequency as a function of reverse bias voltage is given by equation (2.11).

$$C(V) = \frac{\varepsilon A}{W(V)} = A\sqrt{\frac{\varepsilon N_D}{2(V_{BI}-V_a)}} \tag{2.11}$$

$1/C^2$ vs voltage V gives a straight-line plot, slope of the plot gives the doping concentration of semiconductor and effective zero bias potential barrier height.

$$\left(\frac{A}{C}\right) = 2\,\frac{\left[V_{BI}-\frac{kT}{q}\right]}{qk_s\,\varepsilon_0 N_D} + \frac{2V}{qk_s\,\varepsilon_0 N_D} \tag{2.12}$$

$$\varphi_B = V_i + \left(\frac{kT}{q}\right)\left[1 + \ ln\left(\frac{N_0}{N_D}\right)\right] \tag{2.13}$$

Where,

A = Area of cross section of Schottky contact

W = Depletion layer width

$N_D$ = the doping concentration of the material

$N_0 = 1.6 \text{ x } 10^{19} \text{ cm}^{-3}$

$V_{BI}$ = built in potential

T = Temperature

k = Boltzmann constant ($1.3806 \times 10^{-23} \text{ m}^2 \text{ kg s}^{-2} \text{ K}^{-1}$)

**2.6 Molybdenum on SiC Schottky Barrier Diodes**

In the previous investigation, Mo is deposited on 4H-SiC shows an ideality factors ranging from 1.04 - 1.07 and barrier height ranges from 1.04 – 1.10 eV. Mo was used as a contact material on 4H-SiC at room temperature, thermal annealing temperature varied to 400 $^{o}$ C produced ideality factors close to unity and barrier heights ranging from 0.85 - 1.20 eV, as shown in Table 5 [31, 32]. In our investigation, the samples deposited at room temperature (26 $^{o}$C) exhibited an average energy barrier height of 1.66 eV which are better than previous investigation and ideality factor of 1.23 and the samples subjected to thermal annealing at 500 $^{o}$ C for 24 hours in vacuum show an average energy barrier height of 1.65 eV and ideality factor of 1.18 and the major concern here is to improve the ideality factor by optimizing annealing conditions and cleaning procedures.

**Table 5:** Molybdenum Schottky contacts on SiC

| Contact Material | Ideality Factor (n) | Barrier Height $^{I-V}$ (eV) | Barrier Height $^{C-V}$ (eV) | Temperature($^{o}$C) |
|---|---|---|---|---|
| Mo | 1.23 | 1.66 | 1.90 | 26 |
| Mo | 1.07 | 0.91 | 1.10 | 26 |
| Mo | 1.05 | 0.97 | 1.15 | 26 |
| Mo | 1.05 | 1.10 | 1.21 | 26 |
| Mo | 1.04 | 1.04 | 1.08 | 26 |
| Mo | 1.07 | 1.10 | 1.21 | 26 |

## CHAPTER 3

## Growth Techniques for Schottky Barrier Diode Fabrication

This chapter involves growth techniques used to fabricate Mo/SiC Schottky barrier diode such as sample preparation techniques, magnetron sputter deposition technique, rapid thermal processing, etching, current-voltage characterization, capacitance-voltage characterization, annealing techniques, structural behavior evaluation.

### 3.1 Photolithography

Photolithography is a method of transferring geometrical shapes from mask to substrate material, which involves cleaning procedures followed by spinning, baking, mask aligning, developing. SiC substrate material used in fabrication were purchased from CREE research incorporated, they are n-type epitaxial layers grown $4^{o}$ off the axis with (0001) orientation. There are two epitaxial layers in 4H-SiC substrate, one is 0.5µm thick with a doping concentration of $1 \times 10^{18}$ and the other layer is 11.6 µm with a doping concentration of $5.06 \times 10^{15}$ and samples were cut into $10 \times 10$ $cm^2$ square pieces, generally a silicon dioxide ($SiO_2$) sacrificial layer is formed on the substrate can be removed using different chemical mixtures, as shown in Figure 16 [32]. Radio Corporation of America (RCA) cleaning process is used to remove unwanted dust particles from substrate which is also known as degreasing, involves boiling the sample in acetone for 3 minutes, boiling in isopropyl alcohol for 180 seconds followed by rinsing in deionized water. Lastly, the sample is placed in buffer oxide etchant to remove the

silicon dioxide ($SiO_2$) sacrificial layer followed by rinsing in deionized water and dried using nitrogen gas.

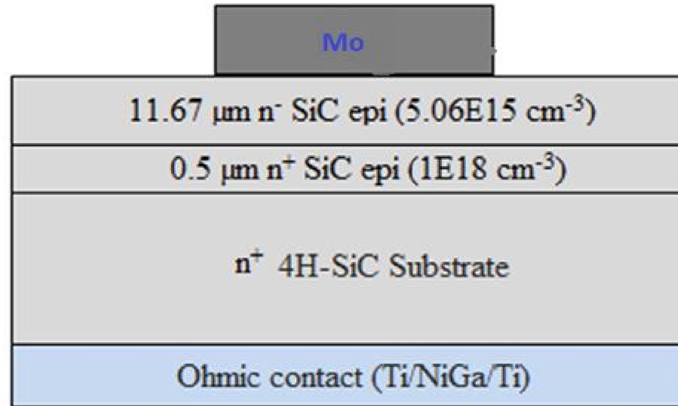



**Figure 16.** The structure of SiC (Mo/4H-SiC)

Sample is placed on spin coater with a drop of photoresist (AZ-4620) and spun at 5000 rpm for 1 min, then the sample is baked to evaporate coating solvent, to densify photoresist at 90 °C for 1 min and sample is exposed to ultra violet rays with a mask aligner setup, as shown in Figure 17. Sample is developed with 300 MIF developer solution until it is completely developed. Additional standard chemical mixtures to degrease are provided in Table 6.

**Table 6:** Chemical mixtures for cleaning SiO2 [ref 29]

| Chemical mixture | Temperature/Time | Comments |
|---|---|---|
| $H_2O$: $NH_4OH$: $H_2O_2$ (5:1:1) | 75 °C for 5 mins | RCA SC1 |
| $H_2O$: HCL: $H_2O_2$ (5:1:1) | 75 °C for 5 mins | RCA SC2 |
| $H_2SO_4$: $H_2O_2$ (2.5:1) | 100 °C for 5 mins | Seven-up |
| $H_2O$: HF:$CH_3CH(OH)CH_3$(100:3:1) | 25 °C for 100 secs | IMEC |
| HCL: $HNO_3$ (3:1) | 50 °C for 5 mins | Aqua Regia |
| HF: $H_2O$ (1:10) | 25 °C | Dilute HF |
| HF: $NH_4F$ (1:7) | 25 °C | BOE/BHF |
| $H_2O$: $NH_4OH$: $H_2O_2$ (5:1:1) | 75 °C for 5 mins | RCA SC1 |

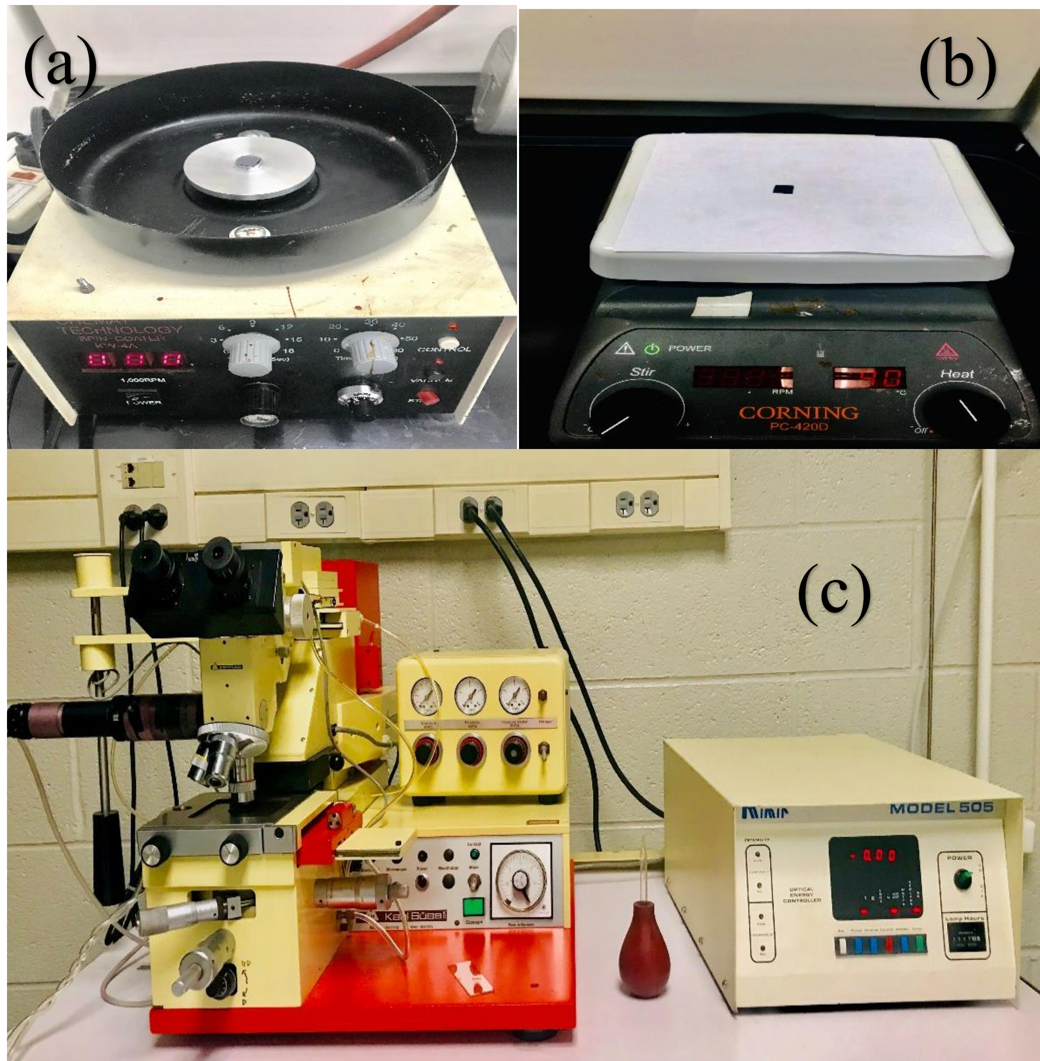



**Figure 17**. (a) Spin coater (b) Heater (c) Mask aligner

### 3.2 Magnetron Sputter Deposition

The magnetron sputtering technique is a simple and cost-effective process to deposit thin films on substrate. Physical vapor deposition (PVD), metal organic chemical vapor deposition (MOCVD), molecular beam epitaxy (MBE), sol-gel method, ion beam deposition, magnetron sputter deposition, pulsed laser deposition, plasma enhanced chemical vapor deposition (PECVD), low pressure chemical vapor deposition (LPCVD) are other techniques used to deposit [33]. A magnetron sputtering chamber consists of

cathode equipped guns which creates a helical magnetic field. Under a negative pressure environment (≈ $10^{-7}$ Torr) excitation of cathode in the presence of an inert gas such as argon (Ar) creates an electric field across cathode which produces plasma. The positive ions accelerated from discharge are accelerated towards the cathode, eroding target to deposit on substrate resulting in the formation of a thin film coating, as shown in Figure 18 [34].

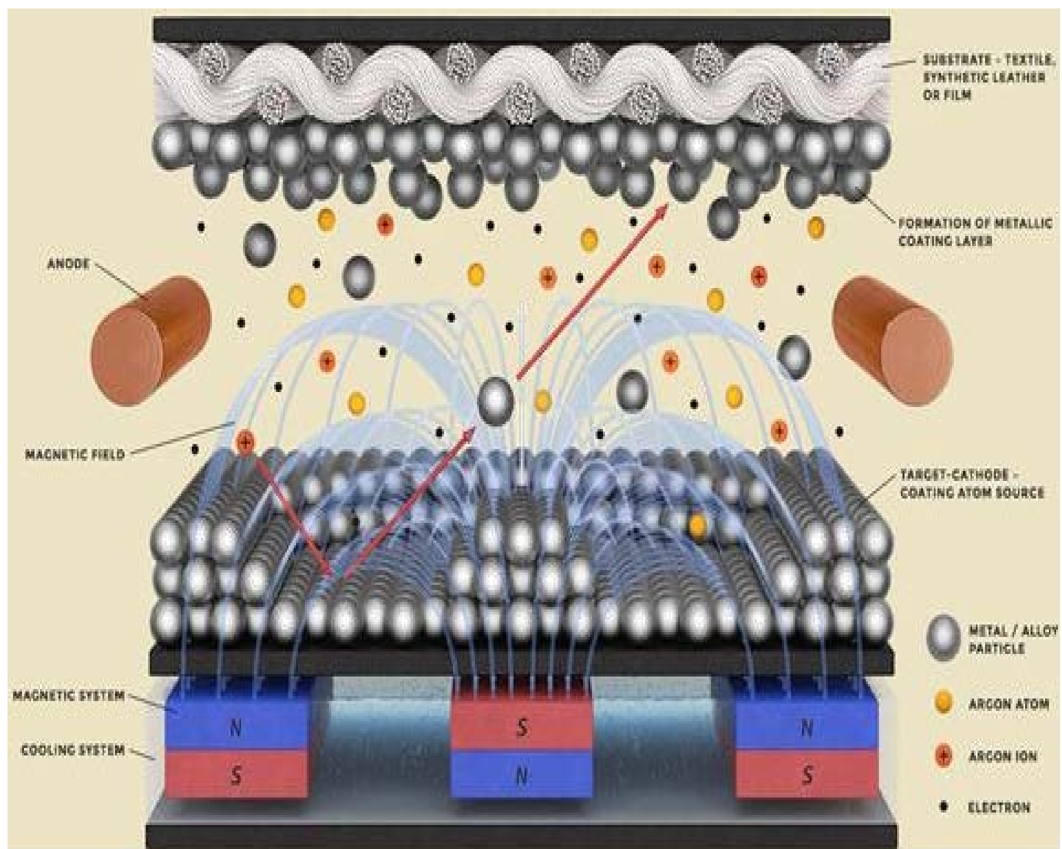



**Figure 18.** Magnetron sputtering technique [ref 35].

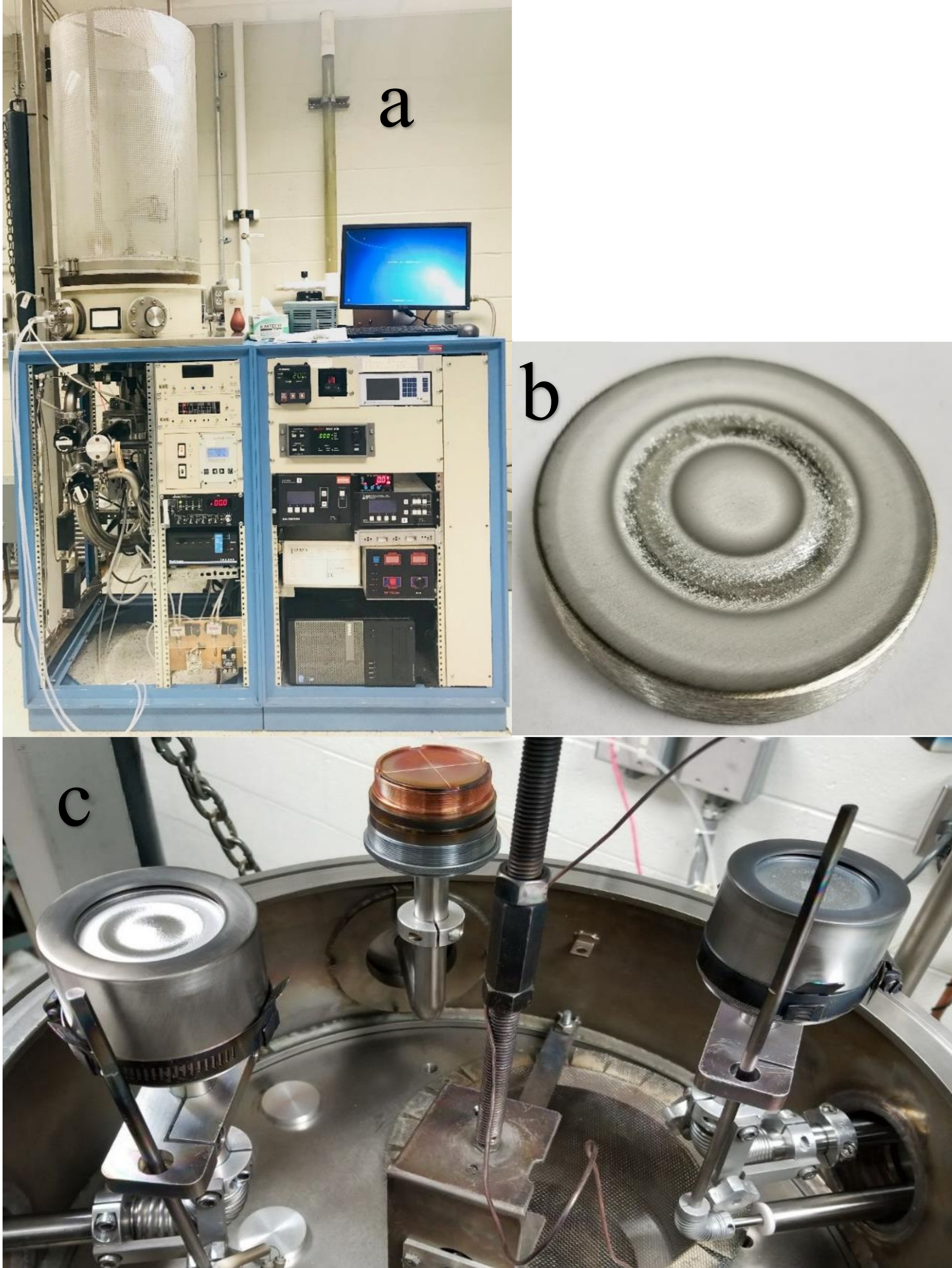



**Figure 19. (**a) Sputter deposition chamber (b) Metal target (c) Cathode assembly setup [ref 35].

### 3.3 Ohmic Contact and Schottky Contact

Ohmic contact is deposited on the backside of SiC to have a low resistance electrical contact, the sample is cleaned using Radio Corporation of America (RCA) process and mounted on a sample holder using double sided carbon tape, allowed deposition chamber to pump down to vacuum ( $\approx 10^{-7}$ ). Titanium (Ti), nickel gallide (90 % Ni and 10 % Ga) are metals used to deposit in the presence of an inert gas argon (Ar) with a flow rate of 10 sccm (standard cubic centimeter per minute) and chamber pressure maintained at 10 mTorr during sputtering, as shown in Table 7 [35].

**Table 7:** Ohmic Contact Parameters

| Metal | Flow rate (sccm) | Chamber Pressure (mTorr) | Current (A) | Base Pressure (mTorr) | Thickness /Time (nm/min) |
|---|---|---|---|---|---|
| Titanium (Ti) | 10 | 3 | 0.1 | $3 \times 10^{-7}$ | 25/13 |
| Nickel gallide ($Ni_{0.9}Ga_{0.1}$) | 10 | 3 | 0.1 | $3 \times 10^{-7}$ | 65/55 |
| Titanium (Ti) | 10 | 3 | 0.1 | $3 \times 10^{-7}$ | 10/7 |

After sputtering, the sample is cleaned using RCA process and annealed at 950 $^{o}C$ in nitrogen ($N_2$) gas for three minutes to reduce contact resistance of ohmic contact, as shown in Figure 20.

**Figure 20.** Rapid thermal processor (RTP)

Schottky contact is deposited on the front side of SiC, the sample is cleaned using (RCA process, sacrificial $SiO_2$ layer is cleaned using a buffer oxide etchant (BOE) and the sample is mounted on the heater, set up is seen in Figure 21, 22. Schottky contact is deposited on multiple samples at 26$^{o}$C, 100 $^{o}$C, 200 $^{o}$C, 300 $^{o}$C, 400 $^{o}$C, 500 $^{o}$C, 600 $^{o}$C, 700 $^{o}$C, 800 $^{o}$C, 900 $^{o}$C, using the conditions mentioned in Table 8. Photolithography cannot be done before deposition because it involves high temperatures which can alter photoresist pattern.

**Table 8:** Schottky contact parameters

| **Metal** | **Flow rate (sccm)** | **Chamber Pressure (mTorr)** | **Current (A)** | **Base Pressure (mTorr)** | **Thickness /Time (nm/min)** |
|---|---|---|---|---|---|
| Mo | 10 | 5.5 | 0.1 | $3 \times 10^{-7}$ | 200/85 |

Schottky Contact

SiC Epi 11 µm,5E15 $cm^{-3}$

SiC Epi 0.5 µm,1E18 $cm^{-3}$

Semiconductor Substrate (0.019 Ω-cm)

Ohmic Contact

**Figure 21.** Ohmic contact and Schottky contact illustration

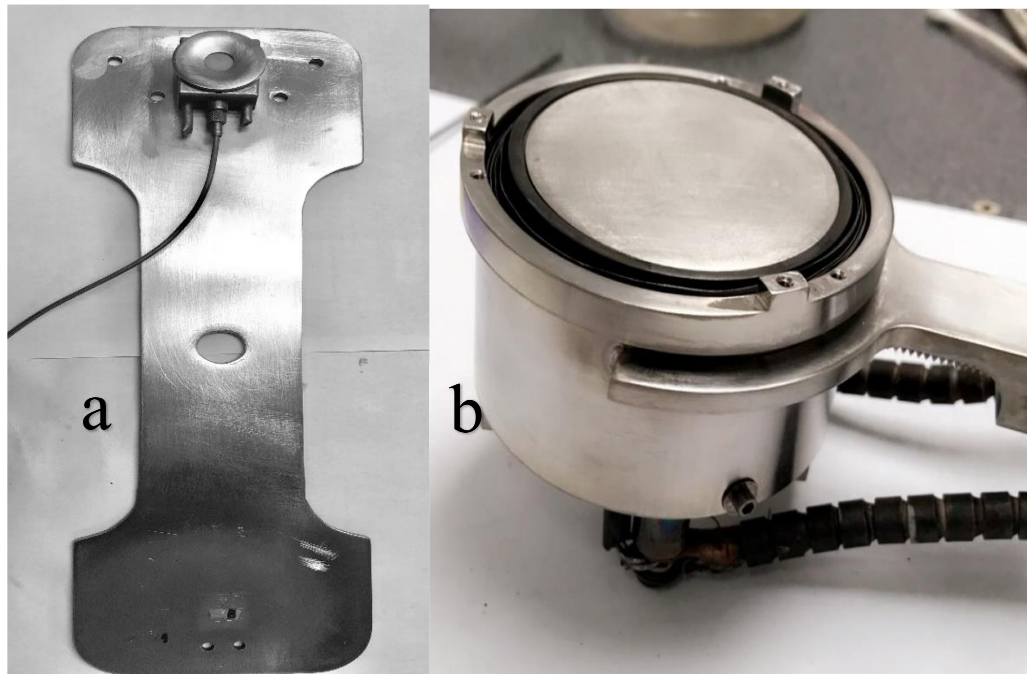



**Figure 22.** (a) Sample holder (b) Heater

### 3.4 Electrical Characterization

Electrical characterization involves current-voltage characteristics, capacitance-voltage characteristics, current-voltage-temperature (I-V-T) characteristics performed on the samples and equipment used.

#### 3.4.1 Current-Voltage (I-V) Measurements

Current-voltage measurements were performed using Keithley source meter model 2410. Keithley source meter model 2410 has a voltage source ranges from 200 mV to 1100 V, measure current ranges from 1µA to 1A and resistance ranges from 20Ω to 200 MΩ. Samples deposited at different temperatures are tested using a procedure as follows: the sample is glued on a copper plate with a conductive silver paste, the base of copper plate act as a negative terminal and probe mounting on the Schottky contact act as a positive terminal during the forward bias condition, as shown in figure 23(a) and (b). A LabVIEW software is programmed to analyze current-voltage (I-V) plots with a variable voltage from 0 – 3 V at 300 regular data points. Measurements were performed on different diodes using probe station equipped with the microscope, the procedure is repeated on five diodes of each sample from 26 $^{o}$C to 900 $^{o}$C and results are analyzed, as shown in Figure 24(a) and (b).

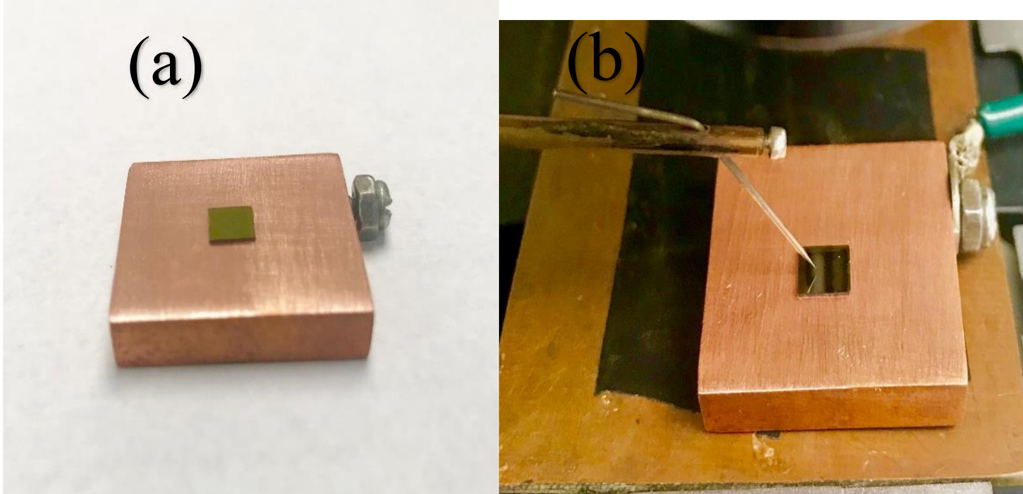



**Figure 23.** (a) Sample mounted on the copper plate (b) Sample mounted on a copper plate with probe

Ideality factor and barrier height are obtained by analyzing data with thermionic equation, ideality factor decides the quality of diode, usually ideality factor is in between 0 - 2, 1 represents the best and barrier height is the contact energy difference between metal and semiconductor and measured in eV. Later, samples are annealed for 24 - 48 hours and characterization is carried as mention before. Reverse bias measurements are done using the same setup Keithley 2410 source meter to measure the reverse breakdown voltage on all the samples.

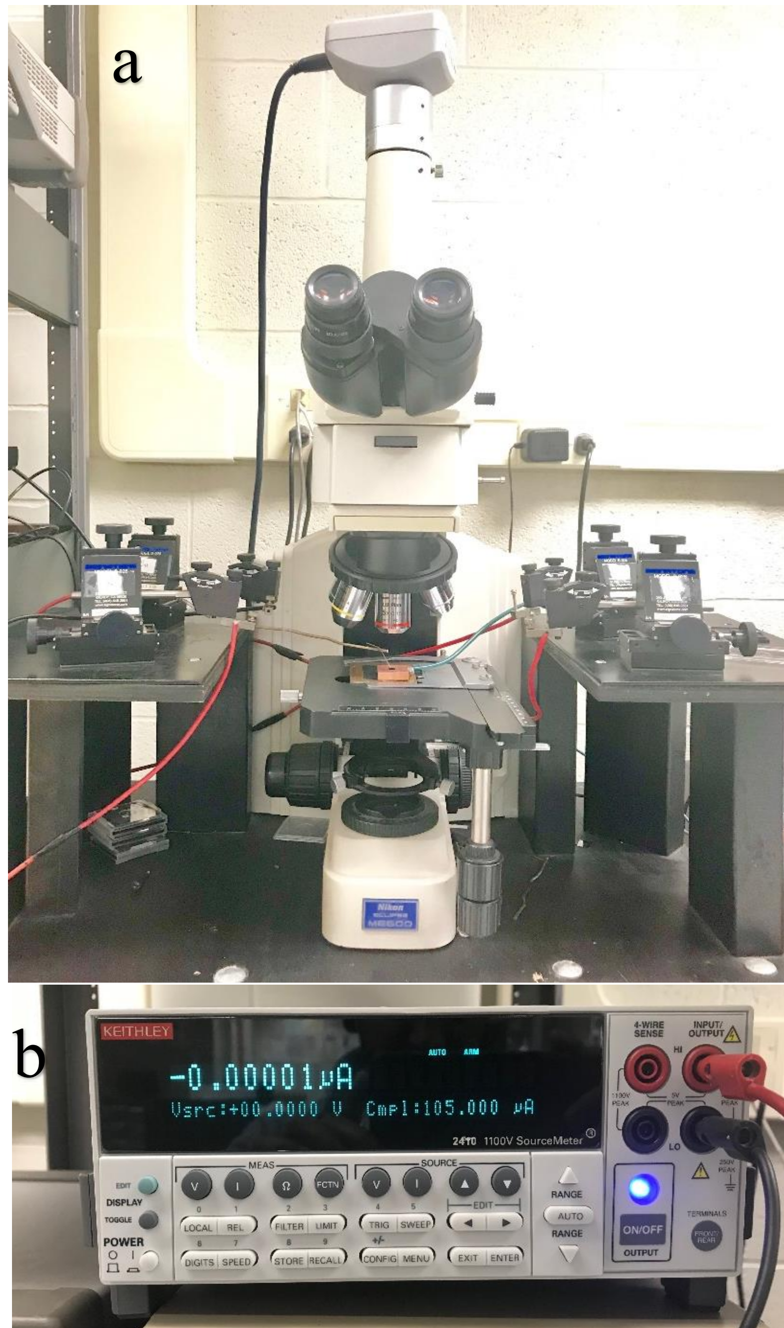



**Figure 24.** (a) Probe station (b) Keithley 2410 source meter

### 3.4.2 C-V Measurements

Capacitance-voltage measurements were performed using Agilent precision LCR meter model E4980A to analyze doping concentration and barrier height. LCR meter has four output probes, two terminals are low terminals ($L_{cur}$ $L_{pot}$) and other two terminals are high terminals ($H_{cur}$ $H_{pot}$). LCR and the computer are joined using general purpose interface bus (GPIB) controlled using a LabVIEW software, this software is used to analyze C-V characteristics according to given input parameters. Samples are arranged on a copper plate using silver conductive paste, setup is covered with a lid and probe pointing on the diode, as shown in figure 25. Capacitance-voltage (C-V) quantifications are very much sensitive to atmospheric noises and light so the experiment was performed in dark to have a linear curve. A DC reverse bias voltage of -5 to 0 V is applied by superimposing alternating voltage of 10 mV at a frequency of 1 MHz.

**Figure 25.** (a) LCR meter (b) Sample arranged on a copper plate (c) Isolation container

### 3.4.3 I-V-T Measurements

I-V-T measurements were performed to evaluate the diode characteristics by changing the temperature at regular intervals. Keithley source meter (model 2410) used for measurements which has a voltage source ranges from 200 mV to 1100 V, current source ranges from 1μA to 1A. Sample is mounted on a stainless-steel plate using silver paste and stainless-steel plate is mounted on a ceramic heater excited with a variable autotransformer to regulate the temperature with voltage. The base terminal of stainless steel is connected to the negative terminal of the source meter and the positive terminal of source meter is connected to probe with a needle pointed on to the diode surface. A thermocouple is attached under stainless steel plate to monitor temperature, as shown in figure 26. Repeated measurements are carried by changing the voltage from 0 to 3 V at 300 data points for every 25 $^{o}$ C rise in temperature. The date is analyzed using thermionic equation and graphs are plotted.

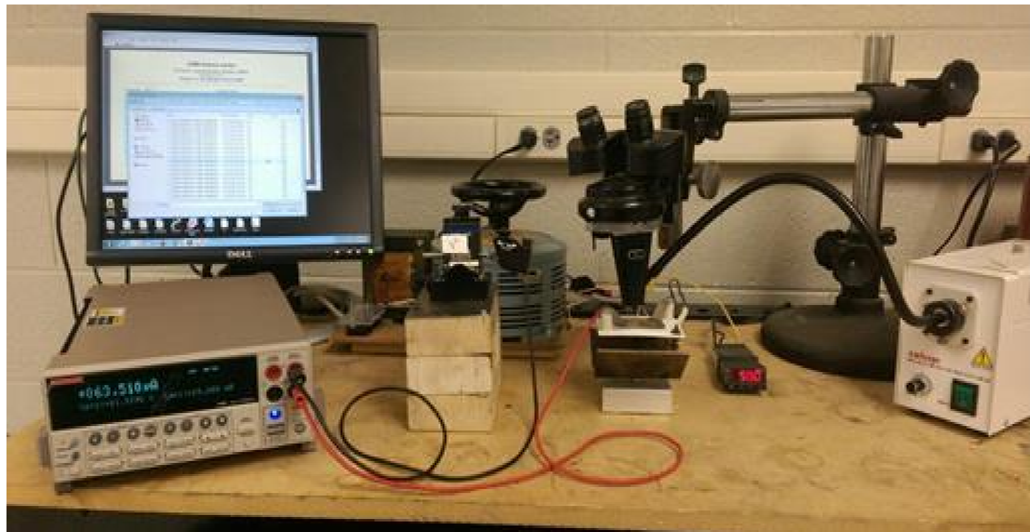


**Figure 26.** I-V-T measurement setup

### 3.5 Structural Characterization (x-ray diffraction)

Structural characterization of 4H-SiC Schottky contact is performed using Bruker X8 prospector to analyze the crystal structure, atomic arrangement, identify phase and dimension of unit cell in 2θ – geometry, as shown in Figure 27 [39]. The fundamental principle of x-ray diffraction is Bragg's law which relates electromagnetic radiation hitting object to the lattice arrangement according to diffraction angle and it is given by equation (3.1) [38]. The main components of setup are a cathode that produces a beam of x-rays, holder and detector to collect reflected rays from the sample, as shown in Figure 28, 29.

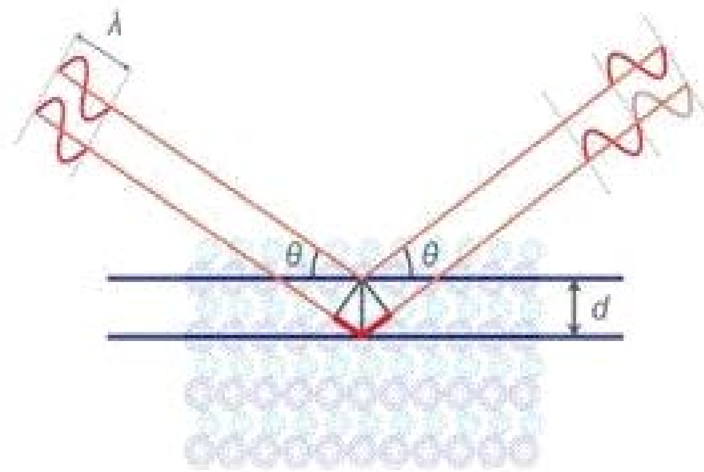



**Figure 27.** Bragg's law sketch [ref 38]

$$n\lambda = 2d \sin \theta \qquad (3.1)$$

Where,

n= Order of reflection

λ= Wavelength

d=Spacing between crystal planes

Θ=Angle between incident beam and reflected lattice plane

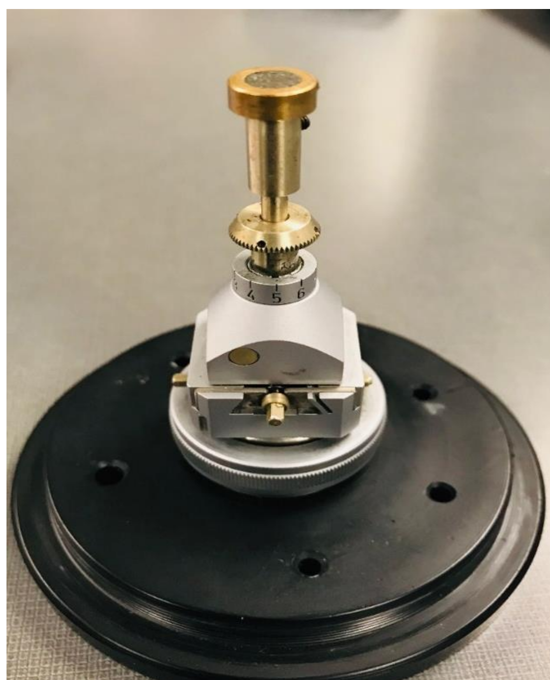


**Figure 28.** Sample holder

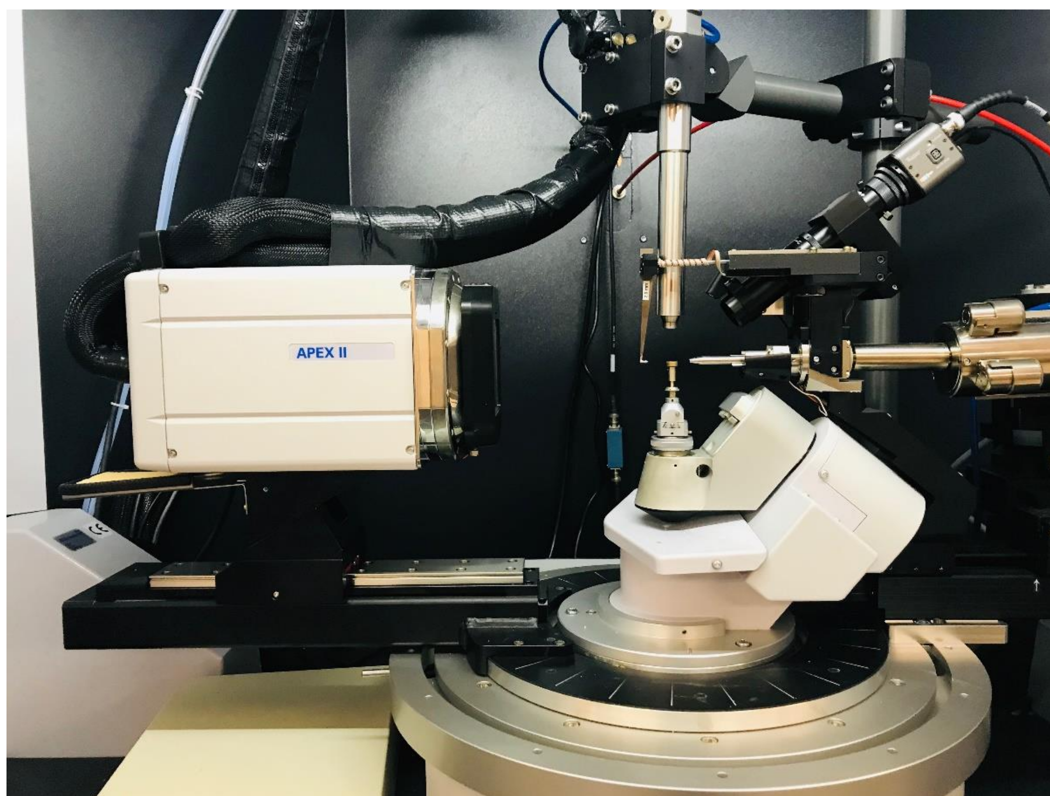



**Figure 29.** Bruker X8 prospector

### 3.6 Annealing

Annealing is a process of heating the material in a vacuum environment for a certain time to improve the crystal structure of diode. Samples are placed in a stainless-steel container and positioned on graphite filament, loaded the chamber to pump down, as shown in Figure 30, 31. After electrical characterization, samples deposited at 900 $^{o}$C, 800 $^{o}$C, 700 $^{o}$C, 600 $^{o}$C, 500 $^{o}$C, 400 $^{o}$C, 300 $^{o}$C, 200 $^{o}$C, 100 $^{o}$C, 26$^{o}$C are annealed for 24 hours at 500 $^{o}$C in a vacuum and re-characterized.

**Figure 30.** Heater base with stainless-steel

**Figure 31.** Samples mounted on heater

# CHAPTER 4

# Results

## 4.1 I-V Measurements

Current-voltage measurements were performed on Mo/SiC Schottky barrier diodes deposited at different temperatures, 900 $^oC$, 800 $^oC$, 700 $^oC$, 600 $^oC$, 500 $^oC$, 400 $^oC$, 300 $^oC$, 200 $^oC$, 100 $^oC$, 26$^oC$ analyzed using OriginPro software. Current-voltage measurements were plotted using OriginPro, gives a clear picture of the relationship between current and voltage, as shown in Figure 32. It is evident from the figure that as deposition temperature increases, turn on voltage of the diode decreases, as shown in Table 8. The diodes deposited at lower temperatures have higher turn on voltage, but as temperature increases the voltage required to activate the diode has decreased, as shown in Figure 33. Samples deposited at higher temperatures are able to perform well and we can say high temperature application looks possible in this case. The Ideality factor of samples deposited at different temperatures are decent from 26 - 900 $^oC$, while the barrier height seems to be decreasing and an optimum barrier height is observed in samples 500, 600 $^oC$ with a decent ideality factor. In the next step, samples are subjected to thermal annealing at 500 $^oC$ for 24 hours in a vacuum and characterized. The ideality factor looks decent and barrier height did not have a noticeable change, optimum barrier heights are observed at 500 $^oC$, 600 $^oC$.

**Table 9:** Turn-on voltages of samples deposited at different temperatures

| Temperature (º C) | Turn-on Voltage ( eV) |
|---|---|
| 26 | 1.51 |
| 100 | 1.48 |
| 200 | 1.07 |
| 300 | 0.95 |
| 400 | 0.92 |
| 500 | 0.89 |
| 600 | 1.03 |
| 700 | 0.98 |
| 800 | 0.94 |
| 900 | 0.66 |

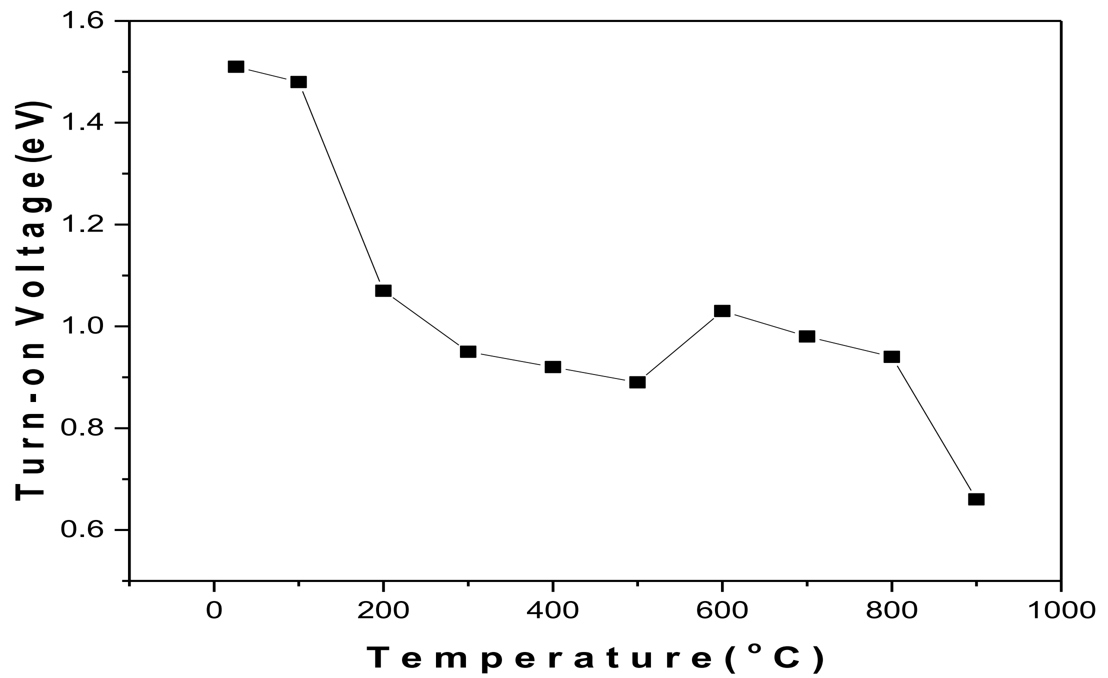



**Figure 32.** Plot of turn-on voltages at different temperatures (26 – 900 ºC)

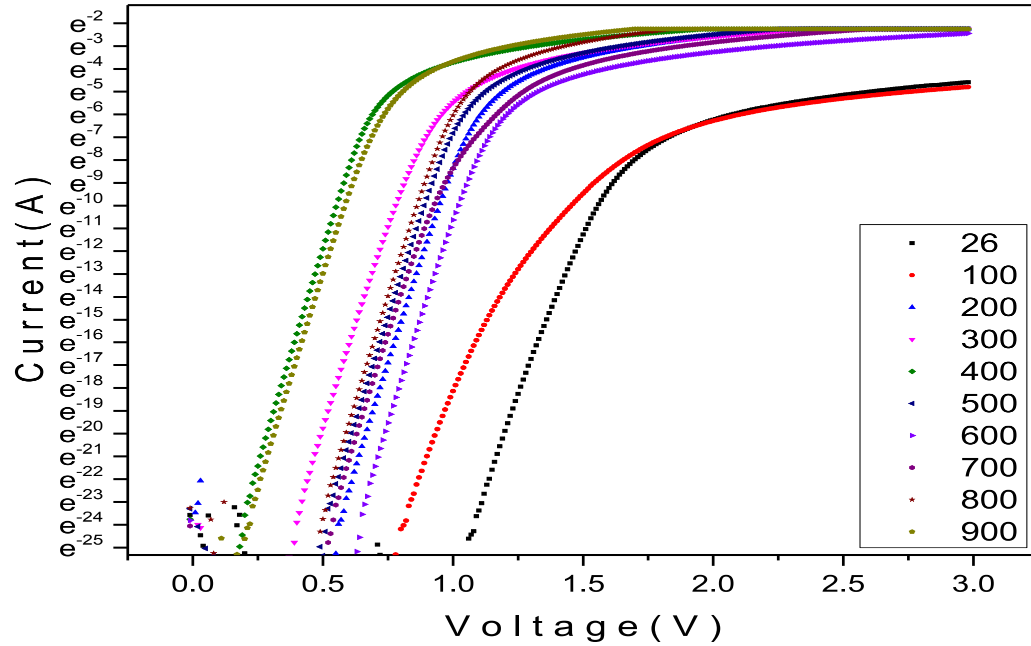



**Figure 33.** Plot of Current-Voltage for contacts deposited at different temperatures (26 – 900°C)

The diodes deposited at different temperatures exhibited energy barrier heights ranging from 1.02 to 1.67 eV and ideality factors varying from 1.04 to 1.23, as shown in Figure 34. Contacts deposited at 600 °C produced the optimum barrier height of 1.34 eV and ideality factor of 1.05 as shown in Table 9. Thermal processing of the samples at 500 °C for 24 hours resulted in barrier heights ranging from 1.00 to 1.70 eV and ideality factors varying from 1.05 to 1.20. The samples deposited at 200, 500, 600 °C diodes shows an optimum barrier height of 1.48, 1.30, 1.30 eV, ideality factors of 1.05, 1.08, 1.07 each, as shown in Table 10 and we believe that variation in electrical properties is due to change in crystal quality.

**Table 10:** Electrical Characteristics at different temperatures before annealing

| Temperature (°C) | Ideality Factor, n | Barrier Height, $\varphi_B$ (eV) |
|---|---|---|
| 26 | 1.23 | 1.67 |
| 100 | 1.17 | 1.67 |
| 200 | 1.10 | 1.34 |
| 300 | 1.08 | 1.34 |
| 400 | 1.04 | 1.23 |
| 500 | 1.07 | 1.21 |
| 600 | 1.05 | 1.34 |
| 700 | 1.08 | 1.28 |
| 800 | 1.06 | 1.27 |
| 900 | 1.05 | 1.02 |

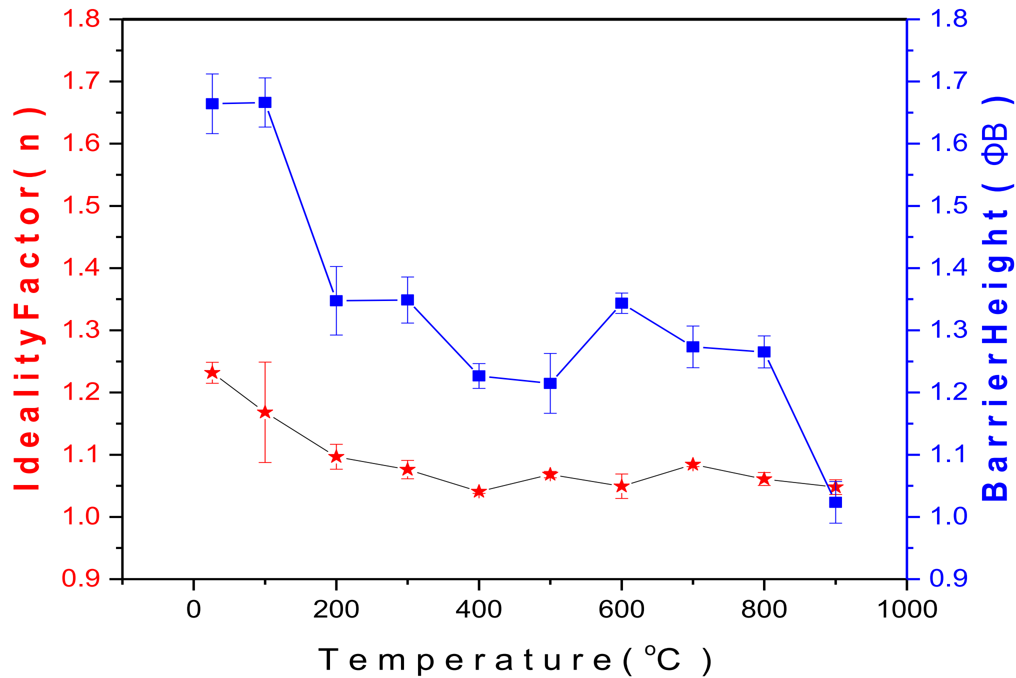



**Figure 34.** Plot of change in ideality factor and barrier height at various temperatures

**Table 11:** Electrical characteristics of samples annealing at 500 °C for 24 hours

| Temperature ( °C_) | Ideality Factor, n | Barrier Height, $\varphi_B$ (eV) |
|---|---|---|
| 26 | 1.19 | 1.56 |
| 100 | 1.20 | 1.70 |
| 200 | 1.05 | 1.48 |
| 300 | 1.12 | 1.24 |
| 400 | 1.06 | 1.25 |
| 500 | 1.08 | 1.30 |
| 600 | 1.07 | 1.30 |
| 700 | 1.09 | 1.29 |
| 800 | 1.05 | 1.25 |
| 900 | 1.05 | 1.00 |

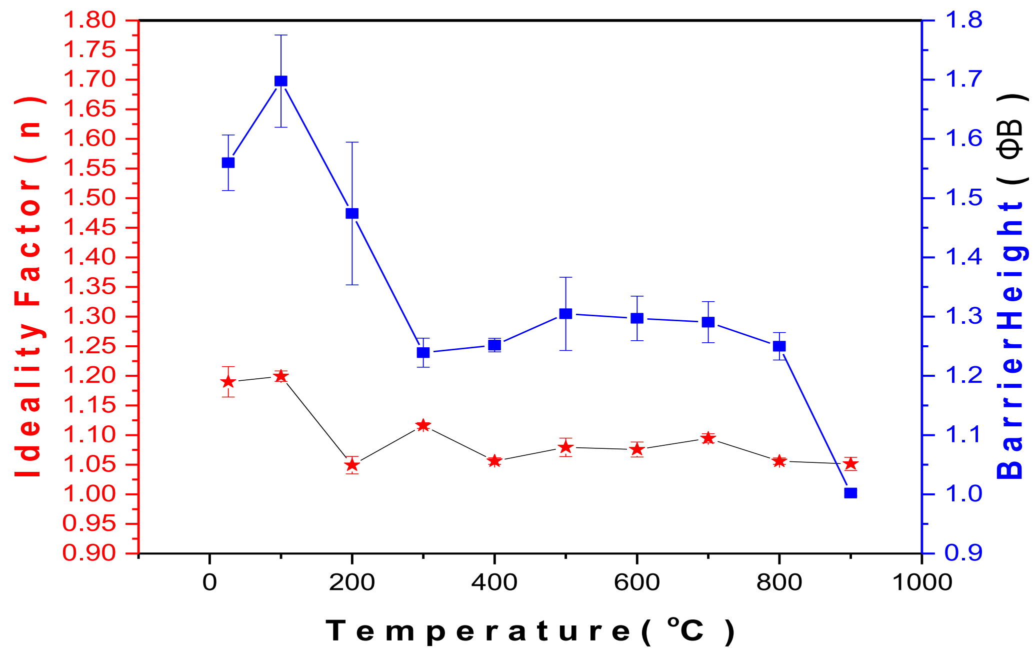



**Figure 35.** Plot of change in ideality factor and barrier height at different deposition temperatures after annealing at 500 °C for 24 hours

### 4.2 C-V Measurements

Capacitance- voltage measurements were performed under reverse bias condition to evaluate doping concentration and barrier height of 4H-SiC Schottky barrier diode. Figures 36, 37 show capacitance voltage characteristics, a plot of $1/C^2$ versus V gives a straight line where we can evaluate slope and intercept to get doping concentration and barrier height. Doping concentration of samples deposited at different temperature shows a thermionic emission ($N_D < 10^{17}$ cm$^{-3}$) which are close to the actual SiC vendor (Cree Inc) value of $5.06 \times 10^{-15}$ cm$^{-3}$. It is observed that barrier height from C-V measurements are higher than I-V measurements due to the concept of image force lowering and in homogeneities between SiC substrate and molybdenum metal interface.

**Table 12:** Doping Concentration and Barrier Height at different Temperatures

| TEMPERATURE (°C) | Doping Concentration, $N_D$ (cm$^{-3}$) | Schottky Barrier Height, $\varphi_B$ (eV) |
|---|---|---|
| 26 | 1.32E+16 | 1.90 |
| 100 | 6.97E+15 | 1.80 |
| 200 | 6.34E+16 | 1.85 |
| 300 | 1.02E+16 | 1.54 |
| 400 | 1.07E+16 | 1.30 |
| 500 | 1.26E+16 | 1.43 |
| 600 | 1.34E+16 | 1.51 |
| 700 | 8.61E+15 | 1.73 |
| 800 | 1.19E+16 | 1.60 |
| 900 | 1.12E+16 | 1.14 |

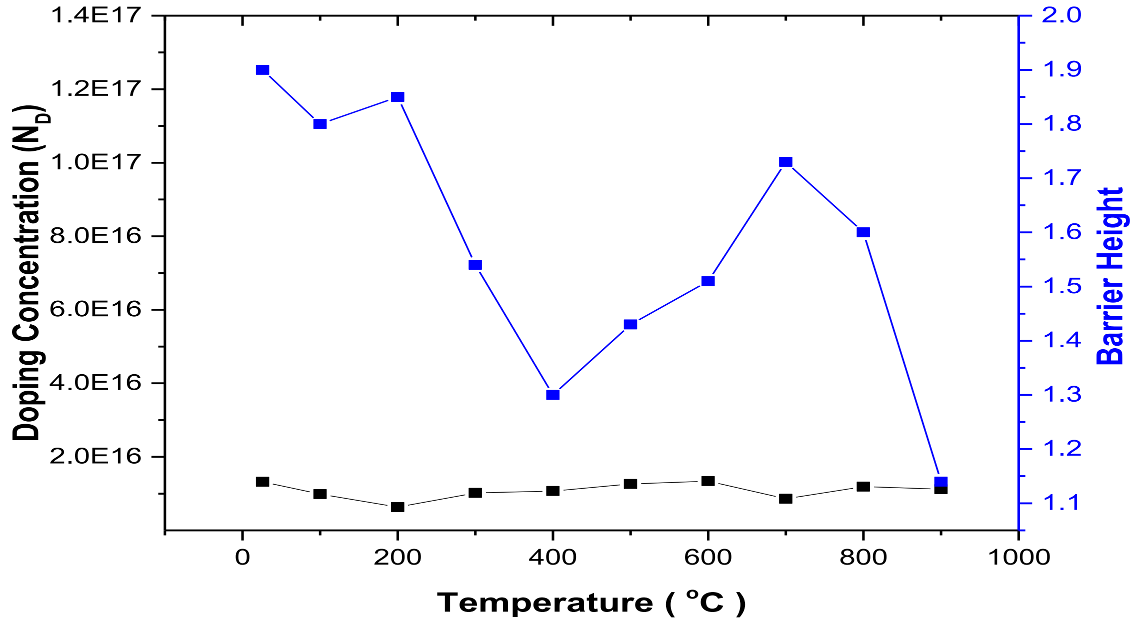



**Figure 36.** Plot of $N_D$ versus $\varphi_B$ at different deposition temperatures

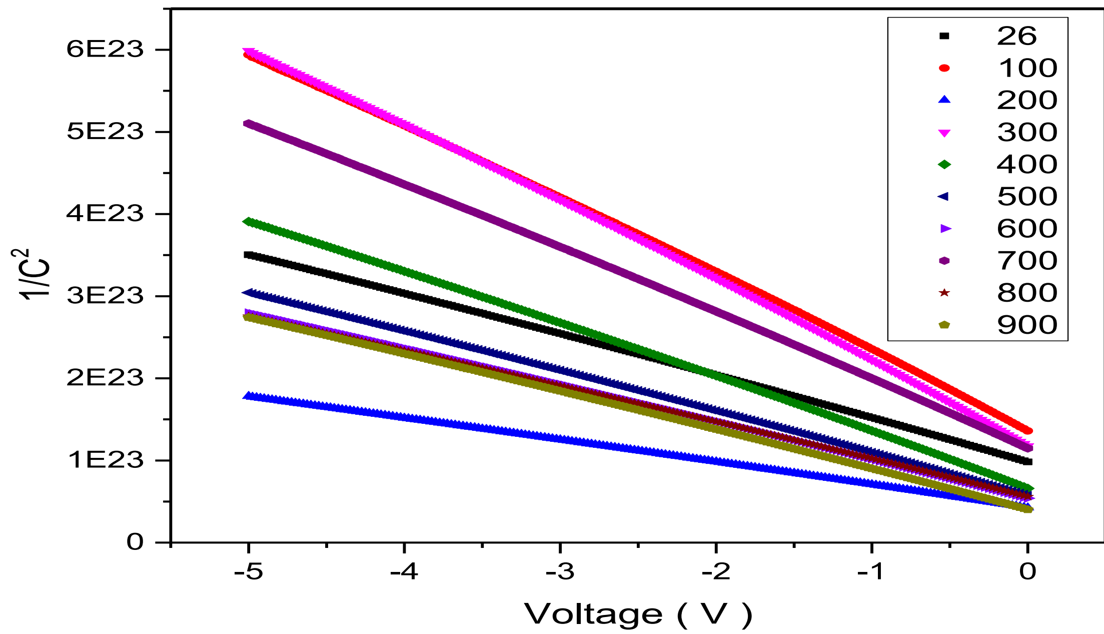
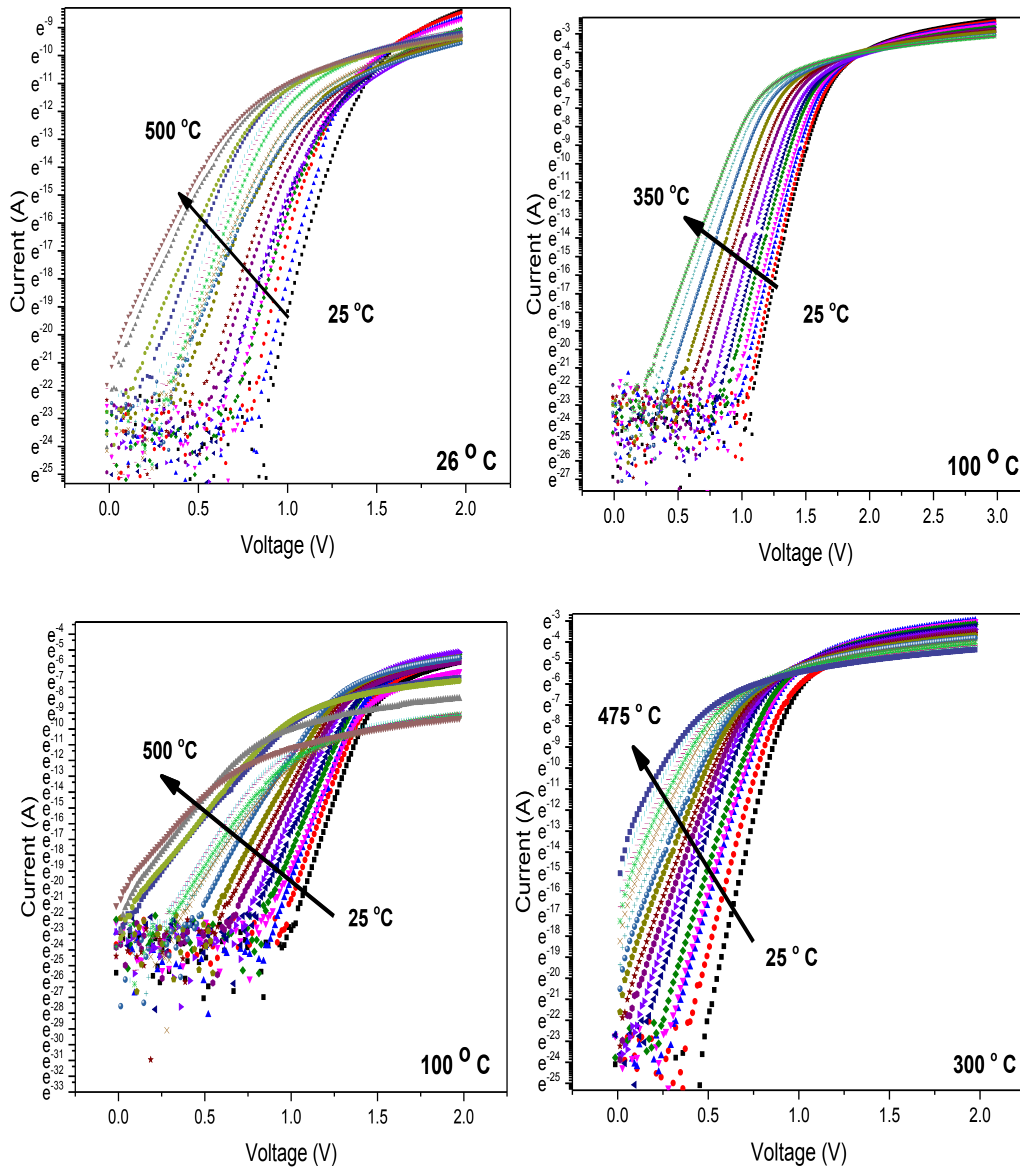



**Figure 37.** Plot of $1/C^2$ versus V at different deposition temperatures

### 4.3 I-V-T Measurements

I-V-T measurements were performed to see the behavior of diode at various temperatures ranging from 25 ºC to 500 ºC. As temperature increases the linear part in I-V plot tends to decrease which results in an increased ideality factor and lowering of potential barrier height. At the temperature 500 ºC linear part of I-V plot completely disappeared and diode acts as ohmic, as show in Figure 38.



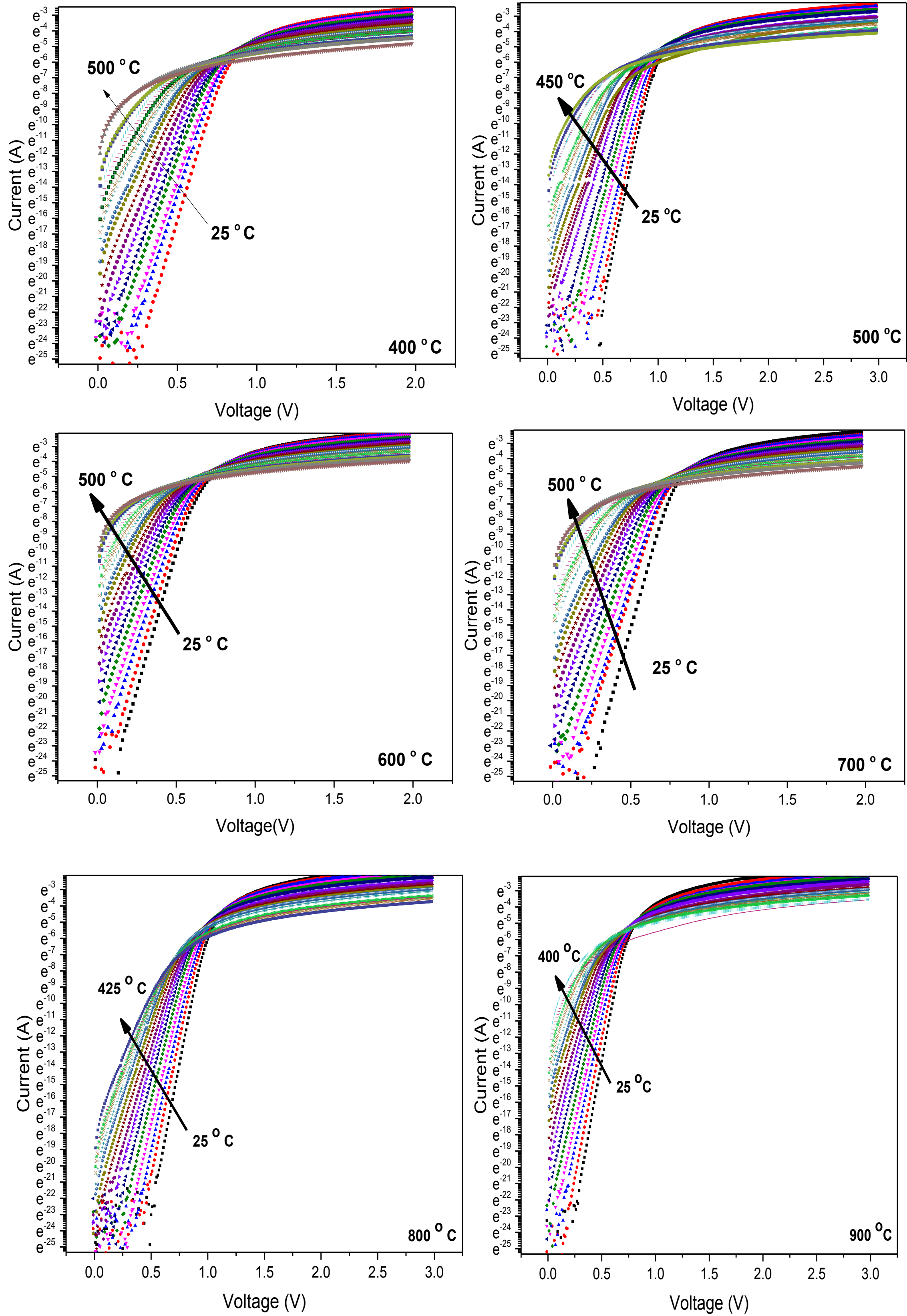



**Figure 38**. I-V-T plot of samples 26 - 900 °C

**Table 13:** Richardson Constant and Barrier height of different samples

| Temperature ($^oC$) | Barrier Height, $\varphi_B$ (eV) | Richardson Constant A**, (A/K-$cm^2$) |
|---|---|---|
| 26 | 1.00 | 0.36 |
| 100 | 0.66 | 1.93 |
| 200 | 1.02 | 0.51 |
| 300 | 1.34 | 0.26 |
| 400 | 1.12 | 3.06 |
| 500 | 1.32 | 3.74 |
| 600 | 1.29 | 3.63 |
| 700 | 0.96 | 2.61 |
| 800 | 1.03 | 2.88 |
| 900 | 0.87 | 0.606 |

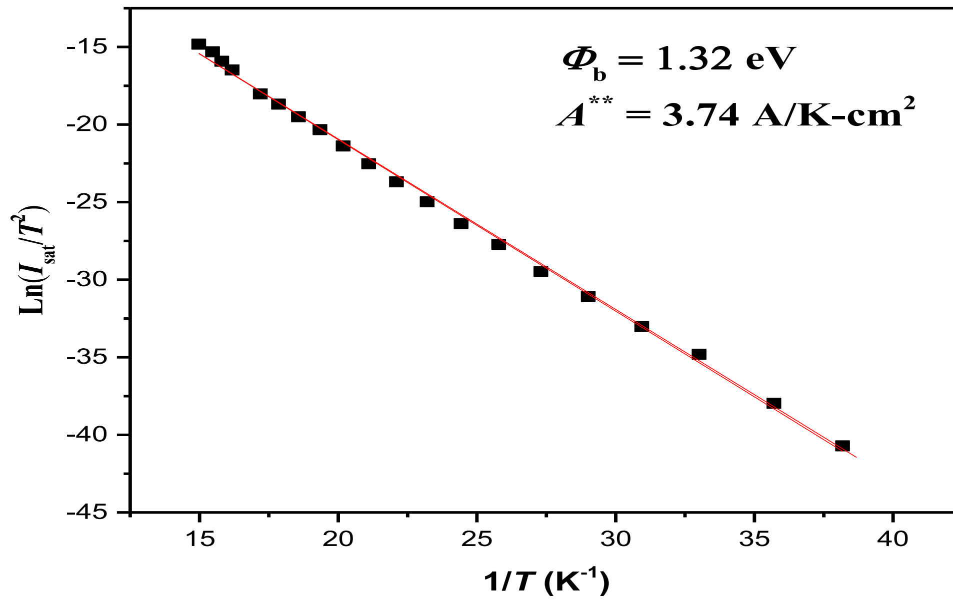



**Figure 39.** Richardson plot of sample deposited at 500 $^o$C.

Current voltage temperature measurements performed to characterize electrical properties of diodes at different temperatures, as labeled in Table 12 and Richardson plot gives an actual area of contact between metal and substrate. Contacts deposited at 500 $^{o}$C produced the optimum barrier height of 1.32 eV and an area of contact (A**) 3.74 A/K-cm$^2$ which is lower than actual value 146 A/K-cm$^2$**,** as shown in Figure 39**.**

**Table 14:** Ideality factor and barrier height of 500 $^{o}$C I-V-T sample.

| Temperature ($^{o}$C) | Ideality Factor, n | Barrier Height, $\varphi_B$ (eV) |
|---|---|---|
| 25 | 1.05 | 1.35 |
| 50 | 1.19 | 1.24 |
| 75 | 1.34 | 1.16 |
| 100 | 1.35 | 1.13 |
| 125 | 1.43 | 1.08 |
| 150 | 1.54 | 1.04 |
| 175 | 1.65 | 1.00 |
| 200 | 1.74 | 0.96 |
| 225 | 1.87 | 0.92 |
| 250 | 2.10 | 0.88 |
| 275 | 2.22 | 0.86 |
| 300 | 2.38 | 0.83 |
| 325 | 2.44 | 0.82 |
| 350 | 2.62 | 0.80 |
| 375 | 2.80 | 0.78 |
| 400 | 3.06 | 0.76 |
| 425 | 3.26 | 0.73 |
| 450 | 3.57 | 0.74 |
| 475 | 3.82 | 0.69 |

### 4.4 XRD Measurements

X-ray diffraction measurements were performed on Mo/4H-SiC Schottky barrier diodes deposited at different temperatures, 900 ºC, 800 ºC, 700 ºC, 600 ºC, 500 ºC, 400 ºC, 300 ºC, 200 ºC, 100 ºC, 26ºC to analyze structural properties and phase relationship between SiC substrate and molybdenum metal, as shown in Figure 40. From Figure 40 formation of silicides is not observed at elevated temperatures except at 600 ºC [40]. After annealing samples for 24 hours at 500 ºC in vacuum three silicide phases are observed with increased temperatures [41].

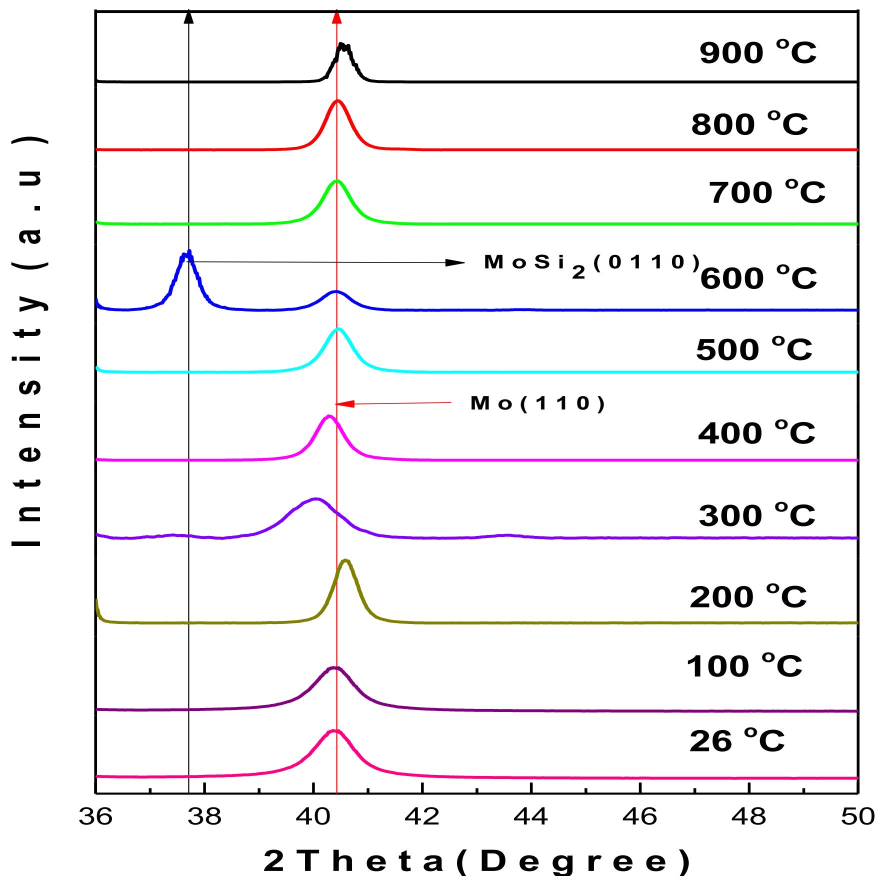



**Figure 40.** XRD pattern of samples deposited from 26 ºC to 900 ºC

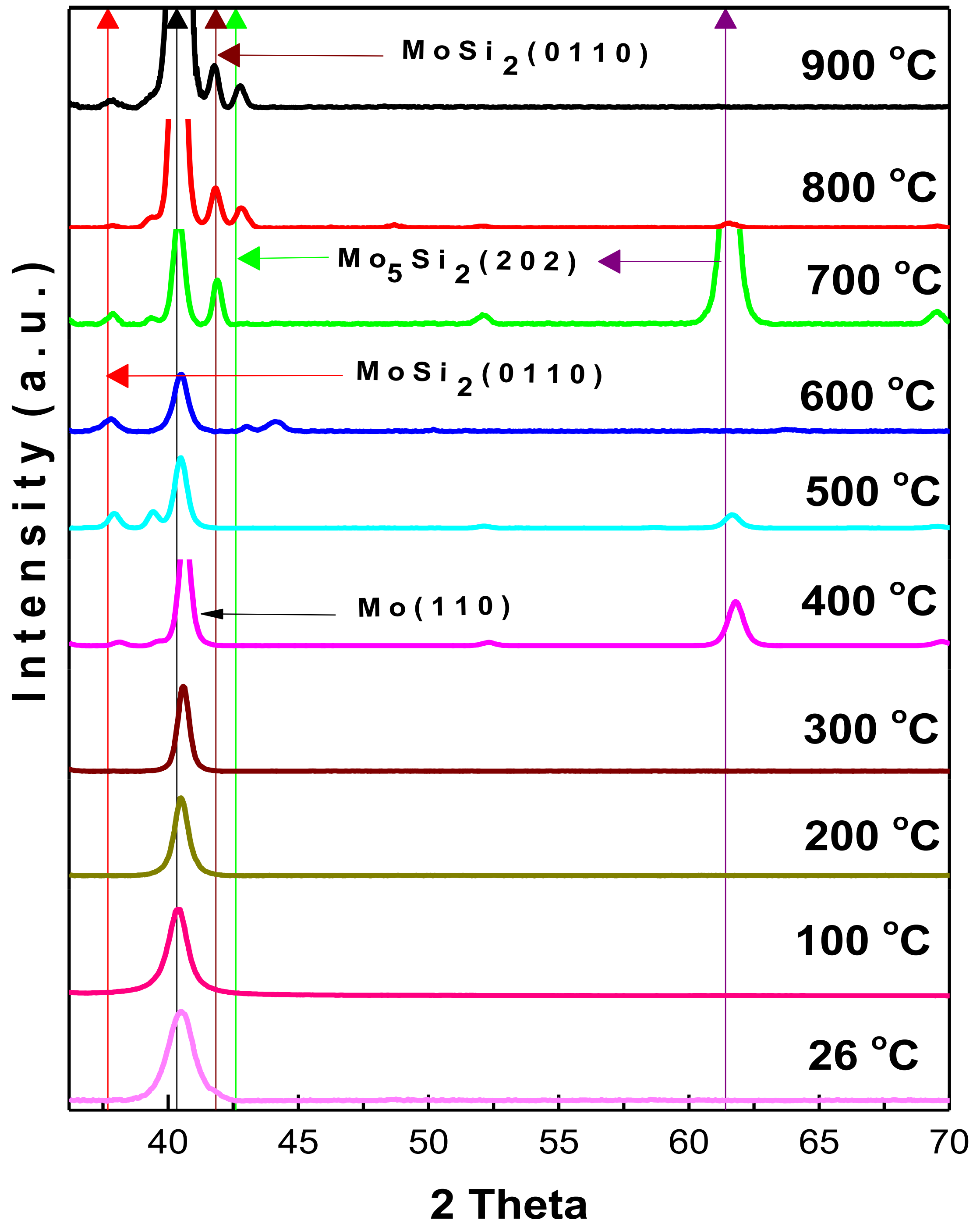



**Figure 41.** XRD pattern of samples deposited from 26 ºC to 900 ºC annealed at 500 ºC for 24 hours

## CHAPTER 5

### 5.1 Conclusion

In this investigation, molybdenum (Mo) metal is used as a Schottky contact material on 4H-SiC at different temperatures ranging from 26 to 900 $^{o}$C. Titanium (Ti) and nickel gallide ($Ni_{0.9}Ga_{0.1}$) are deposited on the back side of 4H-SiC as an ohmic contact. The electrical properties of the diodes are determined by current-voltage, capacitance voltage and current-voltage-temperature measurements. Thermal processing of samples were carried at 500 $^{o}$C for 24 hours to improve the quality of contact and structural properties of the diodes deposited at different temperatures are characterized using X-ray diffraction spectroscopy.

Schottky contacts deposited at 200, 500, 600 $^{o}$C, annealed for 24 hours showed a decent ideality factor of 1.05, 1.08, 1.07 and an optimum barrier height of 1.48, 1.30, 1.30 eV. Capacitance voltage characteristics showed a thermionic emission ($N_D < 10^{17}$ $cm^{-3}$). Contacts deposited at 500 $^{o}$C showed a Richardson constant of 3.74 A/K-$cm^2$ and a barrier height of 1.32 eV. X-ray diffraction results shows the formation $MoSi_2$, $Mo_5Si_2$ at the interfacial layer.

### 5.2 Future Work

Investigation of different cleaning processes on the substrate surface is required to improve the device performance. Diodes deposited at higher temperatures, subjected to thermal annealing shows a clear possibility of device operation at high temperatures, forward bias characteristics of samples exhibit a decent results and investigation of

reverse bias characteristics are required to evaluate breakdown voltage of diodes. As mentioned, deposition temperature shows an impact on interfacial layer of the diodes and accurate analysis of interfacial layer is required.

## References

[1] Kundeti, Krishna Chaitanya "The Properties of SiC Barrier Diodes Fabricated with Ti Schottky Contacts." M.Sc. Thesis, Youngstown State University, 2017. https://etd.ohiolink.edu/. Accessed 24 April 2019.

[2] K. V. Vassilevski, I. P. Nikitina, N. G. Wright, A. B. Horsfall, A. G. O'Neill, and C. M. Johnson, "Device processing and characterisation of high temperature silicon carbide Schottky diodes", *Microelectronic Engineering,* vol. 83, no. 1, pp. 150–154, Jan. 2006.

[3] A. Elasser and T. P. Chow, "Silicon carbide benefits and advantages for power electronics circuits and systems," *in Proceedings of the IEEE,* vol.90, no. 6, pp. 969-986, June 2002.

[4] W. Wesch, "Silicon carbide: synthesis and processing", *Nuclear Instruments and Methods in Physics Research Section B: Beam Interactions with Materials and Atoms,* Volume 116, Issues 1- 4, 1996.

[5] Casady, J.B. & Johnson, R. (1996). "Status of Silicon Carbide (SiC) as a Wide Bandgap Semiconductor for High-Temperature Applications, A Review". *Solid-State Electronics* 39(10):1409-1422, DOI: 10.1016/0038-1101(96)00045-7

[6] K. Jarrendahl and R. F. Davis, SiC Materials and Devices, pp. 1–20, Academic Press London, 1998. https://doi.org/10.1016/S0080-8784(08)62843-4. Accessed on 26 April 2019.

[7] "File: Wurtzite polyhedra.png - Wikimedia Commons", Commons.wikimedia.org, 2017. https://commons.wikimedia.org/wiki/File:Wurtzite_polyhedra.png. Accessed on 26 April 2019.

[8] C. Zetterling, Process technology for silicon carbide devices, 1st ed. London: Institution of Electrical Engineers, 2002. Accessed on 25 April 2019.

[9] T. Ayalew, "SiC Semiconductor Devices Technology, Modeling and Simulation", Ph.D, Vienna University of Technology, 2004. Accessed on 25 April 2019.

[10] H. Morkoç, S. Strite, G. B. Gao, M. E. Lin, B. Sverdlov, and M. Burns, "Large-band-gap SiC, III-V nitride, and II-VI ZnSe-based semiconductor device technologies", *Journal of Applied Physics*, vol. 76, no. 3, pp. 1363–1398, Aug. 1994.

[11] Dr. Alan Doolittle, “Ion Implantation”, GeorgiaTech. http://alan.ece.gatech.edu/ECE6450/Lectures/ECE6450L5-Ion%20Implantation.pdf. Accessed on 24 April 2019.

[12] M. A. Capano, S. Ryu, M. R. Melloch, J. A. Cooper, and M. R. Buss, “Dopant activation and surface morphology of ion implanted 4H- and 6H-silicon carbide,” *Journal of Electronic Materials*, vol. 27, no. 4, pp. 370–376, Apr. 1998.

[13] H. Oda, P. Wood, H. Ogiya, S. Miyoshi, and O. Tsuji, “Optimizing the SiC Plasma Etching Process for Manufacturing Power Devices,” *CS MANTECH Conference*, May 18th - 21st, 2015, Scottsdale, Arizona, USA, 2015.

[14] P. H. Yih, V. Saxena, and A. J. Steckl, “A Review of SiC Reactive Ion Etching in Fluorinated Plasmas,” *physica status solidi (b)*, vol. 202, no. 1, pp. 605–642, 16 November 2001.

[15] P. Yih, "Residue-Free Reactive Ion Etching of Silicon Carbide in Fluorinated Plasmas", *Journal of The Electrochemical Society*, vol. 142, no. 1, p. 312, 1995

[16] M. Wijesundara, Silicon Carbide Microsystems for Harsh Environments, 1st ed. New York, NY: *Springer Science+Business Media*, LLC, 2011.

[17] Hybrid SiC Schottky Rectifier/Si IGBT Modules from GeneSiC enables 175°C operation | GeneSiC Semiconductor, Inc. https://www.genesicsemi.com/hybrid-sic-schottky-rectifier-si-igbt-modules-from-genesic-enables-175c-operation/. Accessed on 24 April 2019.

[18] Wang, Fei & Zhang, Zheyu, Overview of Silicon Carbide Technology: Device, Converter, System, and Application. *CPSS Transactions on Power Electronics and Applications*. 1. 13-32. 10.24295/CPSSTPEA.2016.00003, Member, IEEE, 2016.

[19] David Rowe, Refractory metals, Ideal for use in high-temperature furnace applications, *Refractory metals ASM International*, December 2003. https://www.asminternational.org/documents/10192/1913972/htp00307p056.pdf/ad82c332-c622-4e51-b4ff-6f6805d2ea44. Accessed on 24 April 2019.

[20] J. A. Shields, “Applications of Molybdenum Metal and Its Alloys, second completely revised edition 2013, ISBN 978-1-907470-30-1.

[21] M. Ben Karoui, K. Shili, R. Gharbi, M. Fathallah, S. Ferrero, C. F. Pirri, Effect of Barrier Metal Based on Titanium or Molybdenum in Characteristics of 4H-SiC Schottky Diodes, *Sensors & Transducers journal*. vol. 27. 180-184, Nov 05 2018.

[22] L. Stöber et al., “Impact of sputter deposition parameters on molybdenum nitride thin film properties,” *J. Micromech. Micro engineering*. vol. 25, no. 7, p. 074001, May 2015.

[23] “Silicon Carbide Schottky Barrier Diodes Taking Efficiency to the Next Level for PFC and Other Applications”, *RHOM Semiconductors*, Innovations Embedded. https://www.rohm.com/documents/11308/12928/ROHM_SiC+Diodes_wp.pdf. Accessed on 24 April 2019.

[24] V. L. Rideout, “A review of the theory, technology and applications of metal-semiconductor rectifiers,” *Thin Solid Films*, vol. 48, no. 3, pp. 261–291, Feb. 1978.

[25] B. Sharma, “Metal semiconductor Schottky barrier junctions and their applications”, 2st ed. New York: Plenum Press, 1984.

[26] L. C. Han et al., “Annealing temperature influence on the degree of inhomogeneity of the Schottky barrier in Ti/4H—SiC contacts,” *Chinese Physics* B, vol. 23, no. 12, p. 127302, Dec. 2014.

[27] J. Zhao, K. Sheng and R. Lebron-Velilla, "Silicon Carbide Schottky Barrier Diode", Int. J. Hi. *Special Electronics Systems. National Aeronautics and Space Administration* 15, 821, 2005.

[28] T. N. Oder, K. C. Kundeti, N. Borucki, and S. B. Isukapati, “Effects of deposition temperature on the electrical properties of Ti/SiC Schottky barrier diodes,” *AIP Advances*, vol. 7, no. 12, p. 125311, Dec. 2017.

[29] R. Kumaari, "Improved SiC Schottky Barrier Diodes Using Refractory Metal Borides", M.Sc. Thesis, Youngstown State University, 2009.

[30] B. L. Sharma, “Metal semiconductor Schottky barrier junctions and their applications”, 1st ed. New York: Plenum Press, 1984.

[31] G. Richieri, "Molybdenum barrier metal for sic schottky diode and process of manufacture", US 20080237608A1, 02 October 2008.

[32] Karoui, M & Shili, K & Gharbi, Rached & Fathallah, Mohamed & Ferrero, Sergio & F. Pirri, C. "Effect of Barrier Metal Based on Titanium or Molybdenum in Characteristics of 4H-SiC Schottky Diodes". *Sensors & Transducers journal*. vol. 27. 180-184, May 2014.

[33] S. Lee, "Processing and Characterization of Silicon Carbide (6H- and 4H-SiC) Contacts for High Power and High Temperature Device Applications", Ph.D., KTH, Royal Institute of Technology, 2002.

[34] R. Gade, "Comparison of delta and uniform doped p-type and n-type ZnO films", M.Sc. Thesis, Youngstown State University, 2017

[35] S. B. Isukapati, “Gallium Oxide Thin Films for Optoelectronic Applications”, M.Sc. Thesis, Youngstown State University, 2018.

[36] M. Siad, C. Vargas, M. Nkosi, D. Saidi, N. Souami, N. Daas and A. Chami, "Characterization of Ni and Ni/Ti contact on n-type 4H-SiC", *Applied Surface Science*, vol. 256, no. 1, pp. 256-260, ISSN 0169-4332, August 2009.

[37] “Technology  Farotex.” [Online]. Available: http://farotex.com/technology.html. Accessed on 24 April 2019.

[38] “X-ray diffraction |Rigaku.” [Online]. Available: https://www.rigaku.com/en/techniques/xrd. Accessed on 24 April 2019.

[39] “X-ray Powder Diffraction (XRD).” [Online]. Available: https://serc.carleton.edu/research_education/geochemsheets/techniques/XRD.html. Accessed on 24 April 2019.

[40] Y. Ijdiyaou, M. Azizan, E.L. Ameziane, M. Brunel, T.A. Nguyen Tan, "On the formation of molybdenum silicides in Mo/Si multilayers: the effect of Mo thickness and annealing temperature", *Applied Surface Science*, Volume 55, Issues 2–3, ISSN 0169-4332, February 1992.

[41] S. Sen, S. Yilmaz, and U. Sen, “structural characterization of molybdenum silicides deposited on molybdenum by pack method,” Sakarya University, Engineering Faculty, *Department of Metallurgical and Materials Engineering*, Esentepe Campus, 54187 Sakarya, Turkey 15. - 17. 5. 2013, Brno, Czech Republic, EU, 2013.