A BJT MODEL WITH SELF HEATING FOR WATAND COMPUTER SIMULATION

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ABSTRACT

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A brief overview of bipolar junction transistor (BJT) modeling is presented. Two macromodels based on the Gummel-Poon model are designed to simulate npn and pnp BJT performance including self heating. The self-heating models calculate BJT junction temperature, account for temperature dependency in the modeling equations and give automatic adjustment to temperature-variant parameters including the saturation current (I_S) and the forward current gain (β).

Two external thermal equivalent circuit nodes make it possible to connect improved and more complete thermal equivalent models.

A 2N2222 model based on the npn macromodel is developed and used for testing. Common-emitter and mirror current circuits are used to test the models. Experimental results for the thermal steady-state and transient responses are compared with WATAND and PSPICE analyses using the self-heating and nonthermal models of the 2N2222 transistor. For the self-heating model, the error with respect to steady-state experimental data is less than 7%. For the nonthermal models, the error is up to 84%. As temperature increases, error also increases. The self-heating model tracks the thermal transient response correctly, while the nonthermal model shows no thermal transient response. The self-heating model is also used to test the temperature stability of the mirror current circuit fabricated on an IC chip.

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CHAPTER I

INTRODUCTION

WATAND (WATerloo ANalysis and Design) is an interactive computer simulation software package for analyzing and designing linear and nonlinear electric circuits. It was developed by the Electrical Engineering Department of the University of Waterloo in Canada [1]. Many analyses which are essential to circuit analysis and design are available in WATAND, such as dc operating point (DC), dc transfer characteristics (DT), frequency response (FR), transient response (TC) and steady state response (SS), to name a few. The package has a large selection of built-in linear and nonlinear elements, and it allows the user to define elements, analyses and macro procedures. WATAND is an interactive program and is very flexible and convenient to the user.

There are about two dozen bipolar junction transistor (BJT) models in the WATAND model library. All of these BJT models are based on Ebers-Moll and Gummel-Poon models. Some are simple, while others are well extended from the simple models. In all of these models, some model parameters, more or less, are assumed to be temperature variant and complicated equations are introduced for temperature adjustment. All these models assume that the transistor operating temperature, or more precisely, the junction temperature, T_J, does not change during the

analysis. This assumption is quite sufficient for many circuit analyses.

However, the temperature set by the user may not reflect the real situation of the transistor junction temperature because one effect, the self heating in the transistor, is not taken into account. The transistor itself dissipates power, and the power dissipation at the transistor junction causes self heating and increases the junction temperature, T_J. Many transistor parameters are temperature variant. The variation of T_J with respect to the power dissipation may result in the change of the transistor Q-point, thermal runaway and other problems. A large junction temperature due to self heating may cause a circuit design to fail.

The purpose of this thesis is to design a bipolar junction transistor model which includes self heating, reflects junction temperature variation of a working transistor, and tracks the transistor characteristics better than the existing models do. The model is developed starting with the WATAND BJT Gummel-Poon model. When the self-heating function is disabled, the model will turn out to be similar to the WATAND BJT Gummel-Poon models already in existence.

Chapter 2 discusses the Ebers-Moll and the Gummel-Poon models from which all the BJT models in WATAND are developed. In Chapter 3, thermal equivalent circuits and the two BJT models with self heating are developed.

Chapter 4 provides the WATAND macromodel programs and FORTRAN subroutine for the two self-heating macromodels which are contained in the NPNT and PNPT WBLOCK files. In Chapter 5, a self-heating model for the 2N2222 based on the NPNT macromodel is developed, and several laboratory experiments are performed to test the validity of the self-heating model. The experimental data is compared with the computer simulation results by using different models in WATAND and PSPICE.

The WATAND version used in this work is Version V.11-04 with YSU changes (V1.11-4a). Circuit simulations are run on an Amdahl 5868 mainframe computer under VM/SP CMS Release 5. The PSPICE version used is Version 3.08, July 1988.

Chapter II

AN OVERVIEW OF BJT MODELS

2.1 INTRODUCTION

The Ebers-Moll (EM) and Gummel-Poon (GP) models are two commonly used bipolar junction transistor models [2] used in circuit simulation packages such as WATAND [1,3] and PSPICE [4]. For the Ebers-Moll model, there are three different model levels. The first and the simplest is the EM_1 model which has only dc performance of a transistor. The second level EM_2 model improves the EM_1 dc model and adds junction and diffusion capacitance for ac performance. The EM_3 model is the highest level which has second-order improvement over the dc aspects of the EM_2 model, charge-storage modeling, and temperature performance.

The Gummel-Poon model uses a different mathematical approach to improve the EM_3 model. It is on the same level as the EM_3 model, but is slightly more accurate and complete, and is more often used. The following sections describe the EM_1, EM_2, EM_3 and GP models which are used in WATAND.

2.2 THE EM_1 MODEL

The first bipolar transistor model was described by J. J. Ebers and J. L. Moll in 1954 [5,2]. It is basically a simple, nonlinear dc model. There is no characterization

of charge storage in the device. The Ebers-Moll model is valid for all regions of operation: saturation, active and cutoff, for both inverse and normal connections.

There are two different versions of the EM_1 model: the injection version and transport version. The only difference is in the choice of the reference currents. In WATAND, the transport version is used.

Fig. 2-1 is the nonlinear hybrid-π version of the EM_1 model which is an alternative form of transport version. The reference currents, I_{CC} and I_{EC}, represent the currents that are collected or transported across the base.

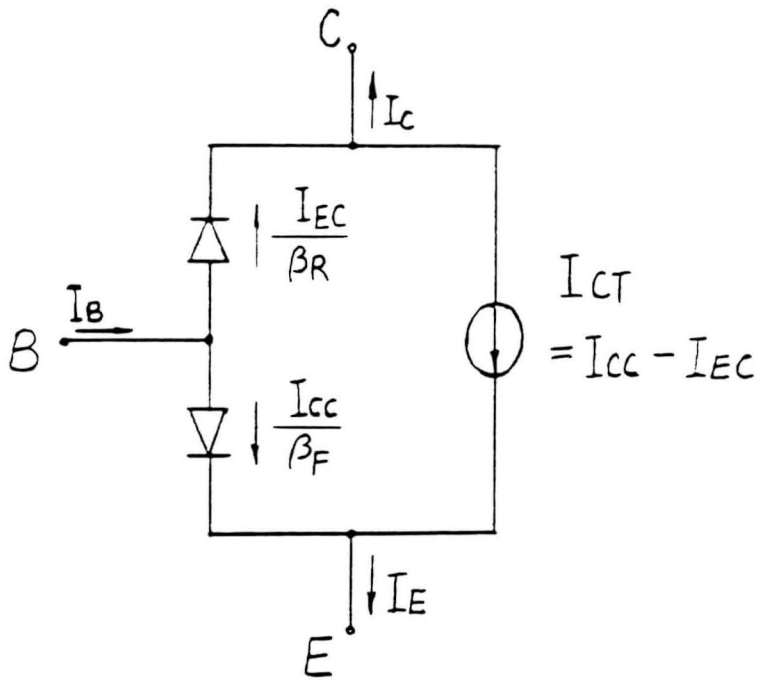

Figure 2-1. Hybrid-π Version of the EM_1 Model

The reference collector source current is

$$I_{CC} = I_S \cdot \left[\exp\left[\frac{qV_{BE}}{kT} \right] - 1 \right] \tag{2.1}$$

and the reference emitter current is

$$I_{EC} = I_S \cdot \left[\exp\left[\frac{qV_{BC}}{kT} \right] - 1 \right] \tag{2.2}$$

where I_S is transistor saturation current,

k is Boltzman constant, $k = 1.3826 \times 10^{-23}$ J/K,

q is electronic charge, $q = 1.6022 \times 10^{-19}$ C, and

T is the temperature in K.

From Fig. 2-1, the model terminal currents can be easily obtained:

$$I_C = I_{CT} - \frac{I_{EC}}{\beta_R} = (I_{CC} - I_{EC}) - \frac{I_{EC}}{\beta_R} \tag{2.3}$$

$$I_E = I_{CT} - \frac{I_{CC}}{\beta_F} = (I_{CC} - I_{EC}) - \frac{I_{CC}}{\beta_F} \tag{2.4}$$

$$I_B = \frac{I_{CC}}{\beta_F} + \frac{I_{EC}}{\beta_R} \tag{2.5}$$

β_F and β_R are the forward and reverse current gains of the transistor, respectively. Both are regarded as constants, independent of current, voltage and temperature at the EM_1 level.

In the EM_1 model, the transistor saturation current, I_S, is assumed to be temperature dependent in the form of

$$I_S(T) = I_S(T_{nom}) \cdot \left[\frac{T}{T_{nom}}\right]^3 \cdot \exp\left[\left[\frac{-E_g}{k}\right]\left[\frac{1}{T} - \frac{1}{T_{nom}}\right]\right] \quad (2.6)$$

where

T is operating temperature in K,

T_{nom} is the nominal temperature in K at which all the model parameters are obtained; in WATAND, it is set to "room" temperature at 27°C or 300 K, and

E_g is the effective gap energy of the semiconductor material in electron-volts.

Although the EM_1 model is quite simple and requires only a few model parameters (β_F, β_R, I_S, T and T_{nom}), it is accurate and useful only for dc characterization of the bipolar junction transistor; there is no transistor charge-storage (i.e., no diffusion or junction capacitances) and no ohmic resistances. These limitations are overcome in a first-order manner in the EM_2 model.

2.3 THE EM_2 MODEL

The EM_2 model shown in Fig. 2-2 improves the dc characterization of the EM_1 model by introducing three constant resistors. They are the collector resistor, r_c, the emitter resistor, r_e, and the base resistor, r_b. These resistors represent the transistor ohmic resistances from its active region to its collector, emitter and base terminals, respectively.

The charge-storage effects in the bipolar junction transistor are modeled by two nonlinear junction capacitors and two nonlinear diffusion capacitors.

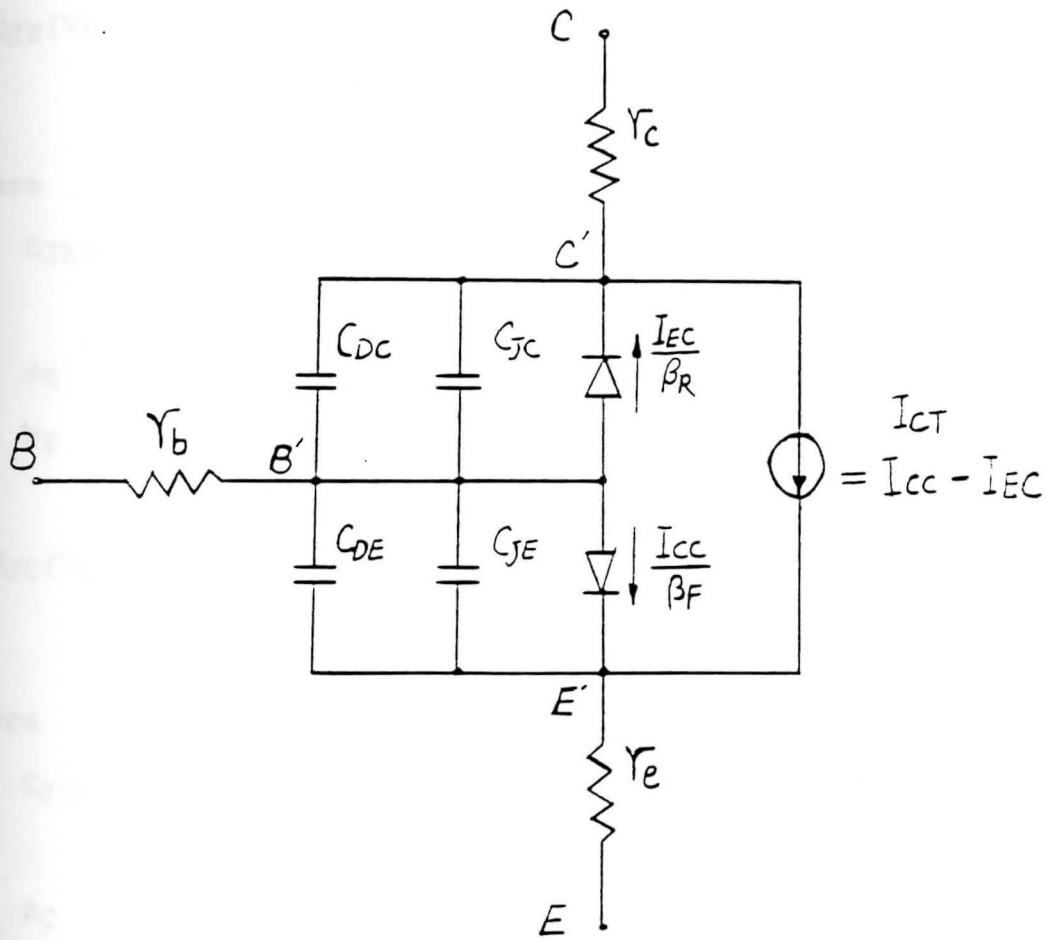

Figure 2-2. The EM_2 Model

2.3.1 JUNCTION CAPACITORS

The two junction capacitors C_{JE} and C_{JC} in Fig. 2-2 model the incremental fixed charges stored in the transistor space-charge layers for incremental changes in the associated junction voltage. The capacitors are denoted by C_{JE} for the base-emitter junction and C_{JC} for the base-collector junction. For an npn transistor

$$C_{JE}(V_{B'E'}) = \frac{C_{JE0}}{\left[1 - \frac{V_{B'E'}}{\phi_E}\right]^{m_E}} \tag{2.7}$$

where

C_{JE0} is the value of the emitter-base junction capacitance at $V_{B'E'} = 0$,

ϕ_E is the emitter-base barrier potential, and

m_E is the emitter-base capacitance gradient factor.

$$C_{JC}(V_{B'C'}) = \frac{C_{JC0}}{\left[1 - \frac{V_{B'C'}}{\phi_C}\right]^{m_C}} \tag{2.8}$$

where

C_{JC0} is the value of the collector-base junction capacitance at $V_{B'C'} = 0$,

ϕ_C is the collector-base barrier potential, and

m_C is the collector-base capacitance gradient factor.

The value of C_{JE} in equation (2.7) will be very large when $V_{B'E'}$ is close to ϕ_E, as is C_{JC} when $V_{B'C'}$ is close to ϕ_C. It has been shown [2,6] that under these situations

equations (2.7) and (2.8) do not hold. Several approximations have been tried. In WATAND, a linear extrapolation method is introduced [3]. It is used when

$$V_{B'E'} > \phi_E - 0.05 \quad \text{or} \quad V_{B'C'} > \phi_C - 0.05$$

otherwise, equation (2.7) and (2.8) still apply. Now the modified expressions for C_{JE} and C_{JC} are

$$C_{JE} = \frac{C_{JE0}}{\left[1 - \frac{V_{B'E'}}{\phi_E}\right]^{m_E}} \qquad V_{B'E'} \le \phi_E - .05 \qquad (2.9)$$

$$C_{JE} = K_1 \cdot V_{B'E'} + K_2 \qquad V_{B'E'} > \phi_E - .05 \qquad (2.10)$$

where

$$K_1 = \left.\frac{dC_{JE}}{dV_{B'E'}}\right|_{V_{B'E'} = \phi_E - .05} \qquad (2.11)$$

$$K_2 = -K_1 \cdot (\phi_E - .05) + C_{JE}\Big|_{V_{B'E'} = \phi_E - .05} \qquad (2.12)$$

$$C_{JC} = \frac{C_{JC0}}{\left[1 - \frac{V_{B'C'}}{\phi_C}\right]^{m_C}} \qquad V_{B'C'} \le \phi_C - .05 \qquad (2.13)$$

$$C_{JC} = K_1 \cdot V_{B'C'} + K_2 \qquad V_{B'C'} > \phi_C - .05 \qquad (2.14)$$

where

$$K_1 = \left.\frac{dC_{JC}}{dV_{B'C'}}\right|_{V_{B'C'} = \phi_C - .05} \qquad (2.15)$$

$$K_2 = -K_1 \cdot (\phi_C - .05) + C_{JC}\Big|_{V_{B'C'} = \phi_C - .05} \qquad (2.16)$$

2.3.2 DIFFUSION CAPACITORS

The two diffusion capacitors model the charge associated with mobile carriers in the transistor. The charges, Q_{DE} and Q_{DC}, are modeled by two nonlinear capacitors C_{DE} and C_{DC}, respectively, given by:

$$C_{DE} = \frac{Q_{DE}}{V_{B'E'}} = \frac{\tau_F \cdot I_{CC}}{V_{B'E'}} \tag{2.17}$$

$$C_{DC} = \frac{Q_{DC}}{V_{B'C'}} = \frac{\tau_R \cdot I_{EC}}{V_{B'C'}} \tag{2.18}$$

where

τ_F is the total forward transit time, and

τ_R is the total reverse transit time.

Both τ_F and τ_R are assumed to be constants in the EM_2 model.

In summary, the EM_2 model requires some extra resistors (r_b, r_e and r_c) and capacitors (C_{JE}, C_{JC}, C_{DE} and C_{DC}) to be added to the EM_1 model in order to improve the transistor dc performance and to provide ac characterization. The EM_2 model is adequate for most modeling, especially for analyzing digital circuits. However, there are still some limitations, including the absence of such dc effects as basewidth modulation and the variation of β with current level. These second-order effects are accounted for in the EM_3 and GP models.

2.4 THE EM_3 MODEL

The EM_3 model is the third level of bipolar junction transistor modeling. It is concerned with second-order improvements in the dc aspects of the EM_2 model, charge-storage modeling, and the temperature performance. The EM_3 model adds the following features:

a) basewidth modulation and variation of β with current and voltage at a given temperature,

b) the rise of τ_F at high current at a given temperature, and

c) variation of device parameters other than I_S with temperature.

These effects are incorporated by modifying existing equations, adding two diodes in the model and introducing extra model parameters. Fig. 2-3 shows the EM_3 model.

2.4.1 AN IMPROVED DC MODEL AT GIVEN TEMPERATURE

The dc characteristics of the EM_3 model are improved by including features of basewidth modulation and the variation of β with current and voltage. The Early voltage V_A is introduced into the EM_3 model. The "Early Effect", or basewidth modulation, describes the change in basewidth because of the change in the collector-base junction voltage. In the normal active region, the width of the space-charge layer of a p-n junction is a strong function

of the applied potential. Large variation in V_{BC} may vary the collector-base space-charge layer significantly. This, in turn, changes the normally thin basewidth.

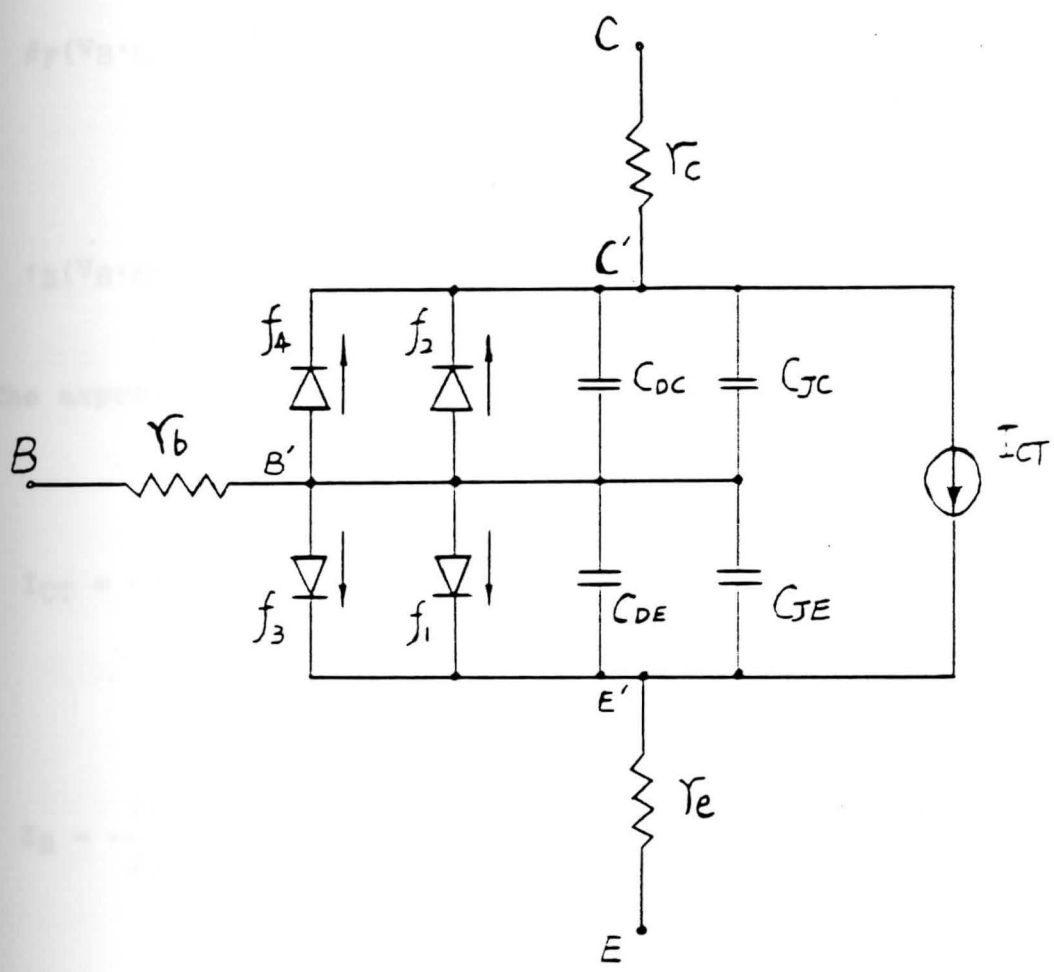

Figure 2-3. The EM_3 Model

Three model parameters, I_S, β_F and τ_F are affected by the Early Effect because they depend on the basewidth strongly. The modified I_S, β_F and τ_F equations are

$$I_S(V_{B'C'}) = \frac{I_S(0)}{1 + \frac{V_{B'C'}}{V_A}} \approx I_S(0) \cdot \left[1 - \frac{V_{B'C'}}{V_A}\right] \tag{2.19}$$

$$\beta_F(V_{B'C'}) = \frac{\beta_F(0)}{1 + \frac{V_{B'C'}}{V_A}} \approx \beta_F(0) \cdot \left[1 - \frac{V_{B'C'}}{V_A}\right] \tag{2.20}$$

$$\tau_B(V_{B'C'}) = \tau_B(0) \cdot \left[1 + \frac{V_{B'C'}}{V_A}\right]^2 \tag{2.21}$$

The expressions for I_{CT} and I_B then become

$$I_{CT} = \frac{I_S(0)}{1 + \frac{V_{B'C'}}{V_A}} \cdot \left[\left[\exp\left[\frac{qV_{B'E'}}{kT}\right] - 1\right] - \left[\exp\left[\frac{qV_{B'C'}}{kT}\right] - 1\right]\right] \tag{2.22}$$

$$I_B = \frac{I_S(0)}{\beta_F(0)} \cdot \left[\exp\left[\frac{qV_{B'E'}}{kT}\right] - 1\right] - \frac{I_S(0)}{\beta_R} \cdot \left[\exp\left[\frac{qV_{B'C'}}{kT}\right] - 1\right] \tag{2.23}$$

In general there are three regions of interest in the variation of β_{dc} with current. Region I is the low current region in which β_F increases with I_C. Region II is the

mid-current region in which β_F is constant. Region III is the high-current region in which β_F drops as current increases.

In region I, the low current region, two diode current sources are added to describe forward and reverse biased situation in the EM_3 model. The expression for I_B then is

$$I_B = \frac{I_S(0)}{\beta_{FM}} \cdot \left[\exp\left[\frac{qV_{B'E'}}{kT}\right] - 1\right] + C_2 I_S(0) \cdot \left[\exp\left[\frac{qV_{B'E'}}{n_{EL}kT}\right] - 1\right]$$

$$+ \frac{I_S(0)}{\beta_{RM}} \cdot \left[\exp\left[\frac{qV_{B'C'}}{kT}\right] - 1\right] + C_4 I_S(0) \cdot \left[\exp\left[\frac{qV_{B'C'}}{n_{CL}kT}\right] - 1\right] \qquad (2.24)$$

where

n_{EL} is the low-current, forward region emission coefficient, and

n_{CL} is the low-current, inverse region emission coefficient.

C_2, C_4 are two extra model parameters, where

$C_2 I_S(0)$ is the composite forward low saturation current, and

$C_4 I_S(0)$ is the composite reverse low saturation current.

In region II, the mid-current region, β_F is regarded as constant. It is now called β_{FM}. The EM_1 model holds. When $V_{B'C'} = 0$,

$$I_C = I_S(0) \cdot \left[\exp\left[\frac{qV_{B'E'}}{kT}\right] - 1\right] \qquad (2.25)$$

$$I_B = \frac{I_S(0)}{\beta_{FM}} \cdot \left[\exp\left[\frac{qV_{B'E'}}{kT} \right] - 1 \right] \qquad (2.26)$$

In region III, the high current region, the injection of minority carriers into the base region is significant compared to the majority carrier concentration. This results in an increase of the total majority carrier concentration. The effect of the excess majority carriers on the collector current is shown in the EM_3 model by modifying the collector current expression for $V_{B'C'} = 0$ as

$$I_C(0) = \frac{I_S(0)}{1 + \theta \cdot \exp\left[\frac{qV_{B'E'}}{2kT} \right]} \cdot \left[\exp\left[\frac{qV_{B'E'}}{kT} \right] - 1 \right] \qquad (2.27)$$

where θ is an additional model parameter for the high current level.

Considering these current regions, β_F can then be expressed as

$$\beta_F^{-1} = a_1 + a_2 \left[I_C^{-(1-1/n_{EL})} \right] + a_3 \cdot I_C \qquad (2.28)$$

where

$$a_1 = \beta_{FM}^{-1} \qquad (2.29)$$

$$a_2 = C_2 \cdot I_S^{(1-1/n_{EL})} \qquad (2.30)$$

$$a_3 = \frac{\theta^2}{\beta_{FM} \cdot I_S} \qquad (2.31)$$

2.4.2 AN IMPROVED CHARGE-STORAGE MODEL AT GIVEN TEMPERATURE

Another second-order improvement is made in the charge-storage model part. The τ_F varies with current as [7,2]

$$\tau_{Fac}(I_C) = \frac{dQ_{DE}}{dI_{CC}}$$

$$= \tau_F \cdot \left[1 + \frac{1}{4} \cdot \left[\frac{L_E}{W}\right]^2 \cdot \left[\frac{I_{CC}}{I_{CO}} - 1\right]^2\right] \qquad I_C > I_{CO} \qquad (2.32)$$

where

L_E is the smallest width of the emitter,

W is the basewidth, and

I_{CO} is the the current at which τ_F starts to increase.

Two additional model parameters are needed: I_{CO} and the ratio (L_E/W).

2.4.3 AN IMPROVED VARIATION WITH OPERATING TEMPERATURE

In the EM_1 and EM_2 models, only one model parameter, I_S, varies with temperature. An improved model is introduced in EM_3 assuming several other parameters are also temperature dependent [2]. In the WATAND EM_3 model, only the major effect, β_F, is taken into account. The β_F temperature variation is

$$\beta_F(T) = \beta_F(T_{nom}) \cdot [1 + BTC_1 \cdot (T-T_{nom}) + BTC_2 \cdot (T-T_{nom})^2] \qquad (2.33)$$

where

BTC_1 is the first-order temperature coefficient, and

BTC_2 is the second-order temperature coefficient.

2.5 THE GUMMEL-POON MODEL

The Gummel-Poon (GP) model is based on the model formulated by Gummel and Poon in 1970 [8,2]. It is almost entirely concerned with improvements in the dc characterization of the EM_3 model. These improvements, however, are normally minor in their effect. Thus, the GP model shown in Fig. 2-4 is basically equivalent to the EM_3 model.

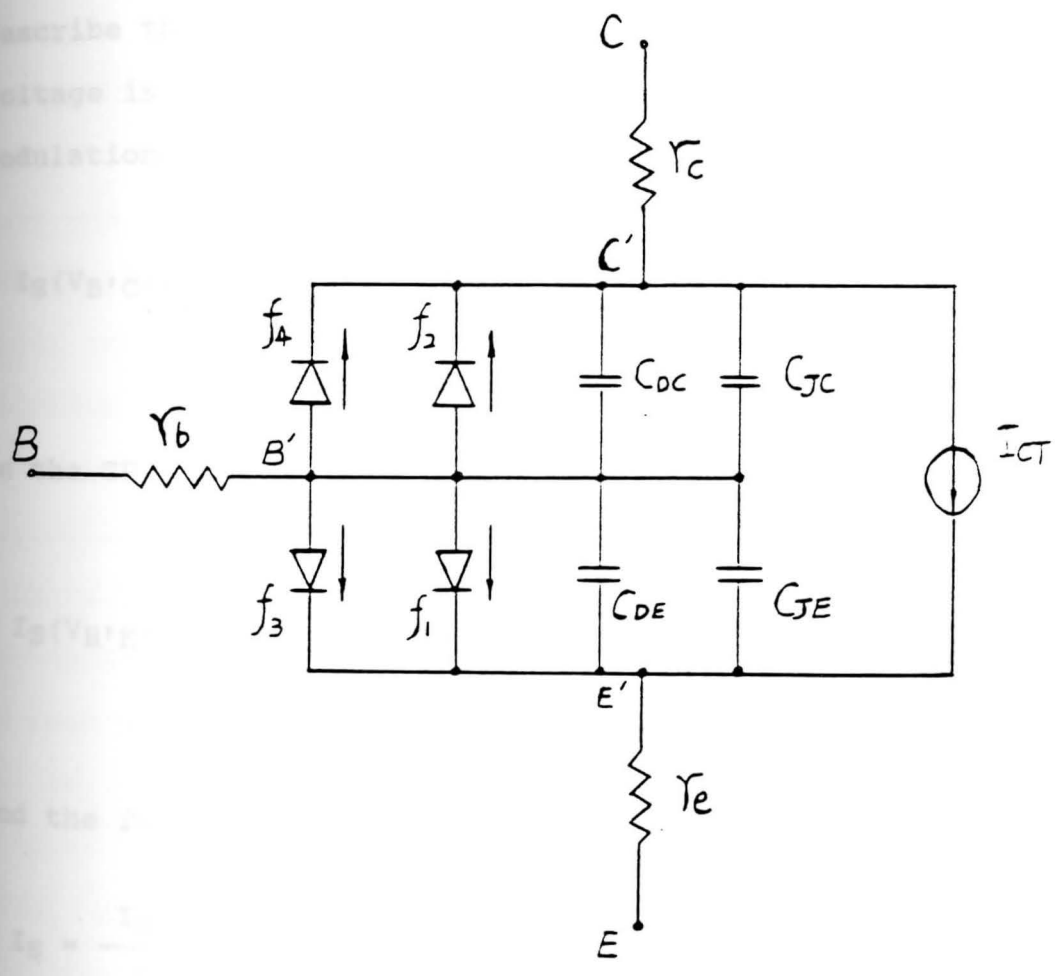

Figure 2-4. The GP Model

The GP model treats the three effects, basewidth modulation, high-injection effects and τ_F versus I_C, together, while the EM_3 model treats them separately. The unified treatment provides a slightly more accurate and complete model than is provided by the EM_3 model. However, the GP model uses a different approach to derive and modify all the formulas; its procedure is more mathematical and less intuitive.

In the GP model, a reverse Early voltage, V_B, is included along with the forward Early voltage, V_A, to describe the basewidth modulation. The reverse Early voltage is due to V_{BE}, not V_{BC}. So, for basewidth modulation only, instead of

$$I_S(V_{B'C'})_{EM_3 \text{ model}} = \frac{I_S(0)}{1 + \dfrac{V_{B'C'}}{V_A}} \tag{2.34}$$

in the GP model, a more complete treatment is given by

$$I_S(V_{B'E'}, V_{B'C'})_{GP \text{ model}} = \frac{I_S(0)}{1 + \dfrac{V_{B'C'}}{V_A} + \dfrac{V_{B'E'}}{V_B}} \tag{2.35}$$

and the full definition for I_S in the GP model is [2]

$$I_S = \frac{I_S(0)}{q_b} \tag{2.36}$$

$$q_b = \frac{q_1}{2} + \left[\left[\frac{q_1}{2}\right]^2 + q_2\right]^{\frac{1}{2}} \tag{2.37}$$

$$q_1 = 1 + \frac{V_{B'C'}}{V_A} + \frac{V_{B'E'}}{V_B} \tag{2.38}$$

$$q_2 = \frac{I_S(0)}{I_K}\left[\exp\left[\frac{qV_{B'E'}}{kT}\right] - 1\right] + \frac{I_S(0)}{I_{KR}}\left[\exp\left[\frac{qV_{B'E'}}{n_{EL}kT}\right] - 1\right] \tag{2.39}$$

where

$I_S(0)$ is the saturation current at $V_{B'C'} = 0$,

I_K is the knee current,

I_{KR} is the reverse knee current.

The ac characterization equations in the GP model are long and complicated, but the results are about the same as for the EM_3 model. The EM_3 and GP models are of the same model complexity in the nonlinear modeling of the bipolar junction transistor. The GP model mainly improves dc performance of the EM_3 model and provides a slightly more accurate and complete result. On the other hand, EM_3 has simpler ac modeling equations than GP does. So in the WATAND GP model, a set of Gummel-Poon dc modeling equations is used for dc performance, while for ac characteristics, the EM_3 ac modeling equations are used. This leads to a simpler model than a complete GP dc and ac treatment would give. At the same time, it saves WATAND computing time and also keeps the accuracy and completeness of the GP model.

Chapter III

DEVELOPING THE BJT MODEL

3.1 INTRODUCTION

In this chapter, several approaches to describe the thermal characteristics of a bipolar junction transistor are discussed. A thermal equivalent circuit for a transistor and the BJT model which deals with temperature variation due to transistor (and/or circuit) operation are developed.

3.2 THERMAL EQUIVALENT CIRCUIT OF A TRANSISTOR

It is evident that the junction temperature variation within a transistor is related in some way to the power applied to the transistor and how the transistor material dissipates heat energy. Because the heat may leave the transistor by radiation, thermal conduction and by convection or forced air cooling, the relationship between the junction temperature and the power dissipation within a transistor is quite complicated.

One approach to this problem is to solve the boundary-value problem posed by the partial-differential equations for heat flow [9]. There are difficulties in using this method. First, to formulate the problem requires a great deal of knowledge about the internal geometry of the transistor; second, certain physical constants, such as the heat conductivity, diffusibility and heat-transfer

coefficient must be available for every material in the device; and last, the solutions for certain equations which are often needed can be obtained only by numerical analysis methods.

Another approach is to introduce Newton's law of cooling. The heat generated within a transistor is transferred to a large body such as a heat sink or a room that remains at an essentially fixed ambient temperature, T_A. The transfer is a combination of radiation, thermal conduction, convection and/or forced air cooling. Most everyday problems of heat transfer can be adequately expressed by Newton's law of cooling [10]

$$T_J - T_A = \theta \cdot P \qquad (3.1)$$

where

T_J is the junction temperature in K,

T_A is the ambient temperature in K,

θ is the thermal resistance in K/W, and

P is the dissipated power in W.

Newton's law states that the temperature difference in K between two equitemperature surfaces is proportional to both the rate at which heat, P, in watts is transferred from one surface to the other and to the thermal resistance, θ, between the two surfaces in K/watt.

According to Newton's law of cooling, the junction temperature of a transistor can be determined as

$$T_J = T_A + \theta \cdot P_T \qquad (3.2)$$

if the ambient temperature, T_A, the thermal resistance

between the junction and the ambient, θ, and the power dissipated in a transistor, P_T, can be measured or calculated. A disadvantage of using this law is that the transient heat flow in a transistor cannot be analyzed.

A third approach, which is commonly used, is to propose a thermal equivalent circuit for the transistor [9,10,11]. The circuit representation of a thermal system is permitted by an analogy between electrical and thermal quantities as shown in Table 3-1.

Table 3-1. Thermal and Electrical Analogies

Electrical	Thermal
V voltage (volts)	T temperature (K)
I current (amperes)	P power dissipation (watts)
R electrical resistance (ohms)	θ thermal resistance (K/watt)
C electrical capacitance (farads)	C_θ thermal capacitance (joule/K)

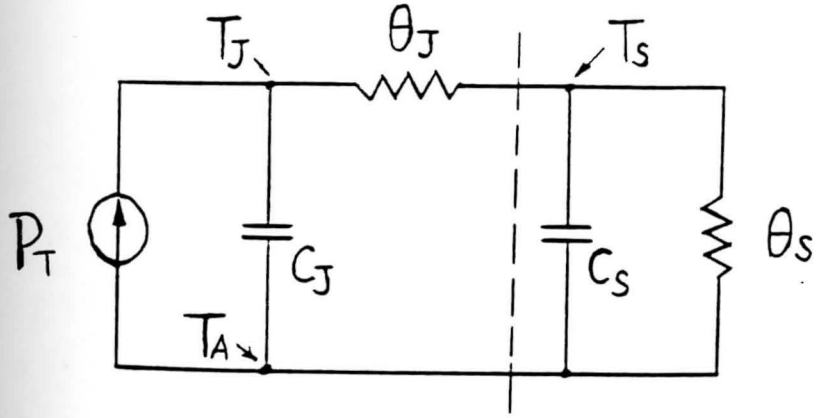

Figure 3-1. The Thermal Equivalent Circuit of a Transistor

Fig. 3-1 shows a thermal equivalent circuit of a bipolar junction transistor [10,11]. The transistor has a thermal resistance, θ_J, and a thermal capacitance, C_J, in the junction; θ_S and C_S, in the heat sink. P_T is the total power dissipation in the transistor. If a transistor is working in a steady state, or say, dissipating constant power, the temperature difference between junction and ambient is

$$T_J - T_A = (\theta_J + \theta_S) \cdot P_T \qquad (3.3)$$

which yields Newton's law of cooling.

For a small transistor without a heat sink in free air, the thermal circuit in Fig. 3-1 could be simplified as in Fig. 3-2. The thermal circuit in Fig. 3-2 is also a reasonable simplification if the total thermal resistance and capacitance of a certain transistor can be determined [11].

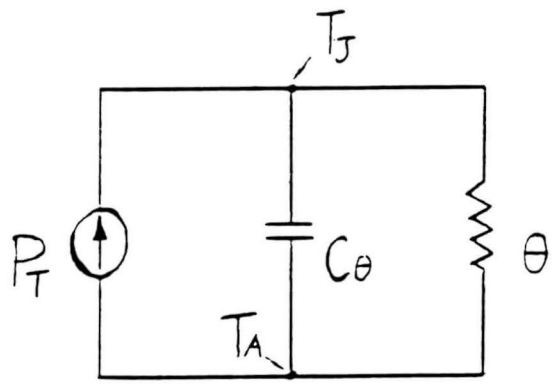

Figure 3-2. A Simplified Thermal Equivalent Circuit

3.3 BJT MODEL WITH SELF HEATING

A BJT model which includes self heating is obtained by combining the electrical and the thermal-equivalent circuits of a transistor. The proposed npn BJT model with self-heating characteristics for this thesis is shown in Fig. 3-3.

The model in Fig. 3-3 has five external terminals. Nodes 1, 2 and 3 are the transistor base, emitter and collector, respectively. Nodes 4 and 5 are two terminals of the thermal equivalent circuit. The voltage at node 4 with respect to node 5 corresponds to the difference between junction and ambient temperature, T_J-T_A.

For the electrical circuit part, the GP model which is discussed in Chapter 2 is used. In the thermal circuit part, the simplified thermal equivalent circuit as shown in Fig. 3-2 is used. The thermal resistance, θ, and the thermal capacitance, C_θ, can be regarded as the total thermal resistance and capacitance from the transistor junction to ambient environment. If a more detailed thermal circuit is needed, one could simply set θ to be large (infinite), and then connect the detailed thermal circuit to the two external nodes, nodes 4 and 5. If the actual junction temperature is desired at node 4, node 5 could be connected to a voltage source equal to the ambient temperature. This simplified thermal circuit provides user flexibility for thermal modeling.

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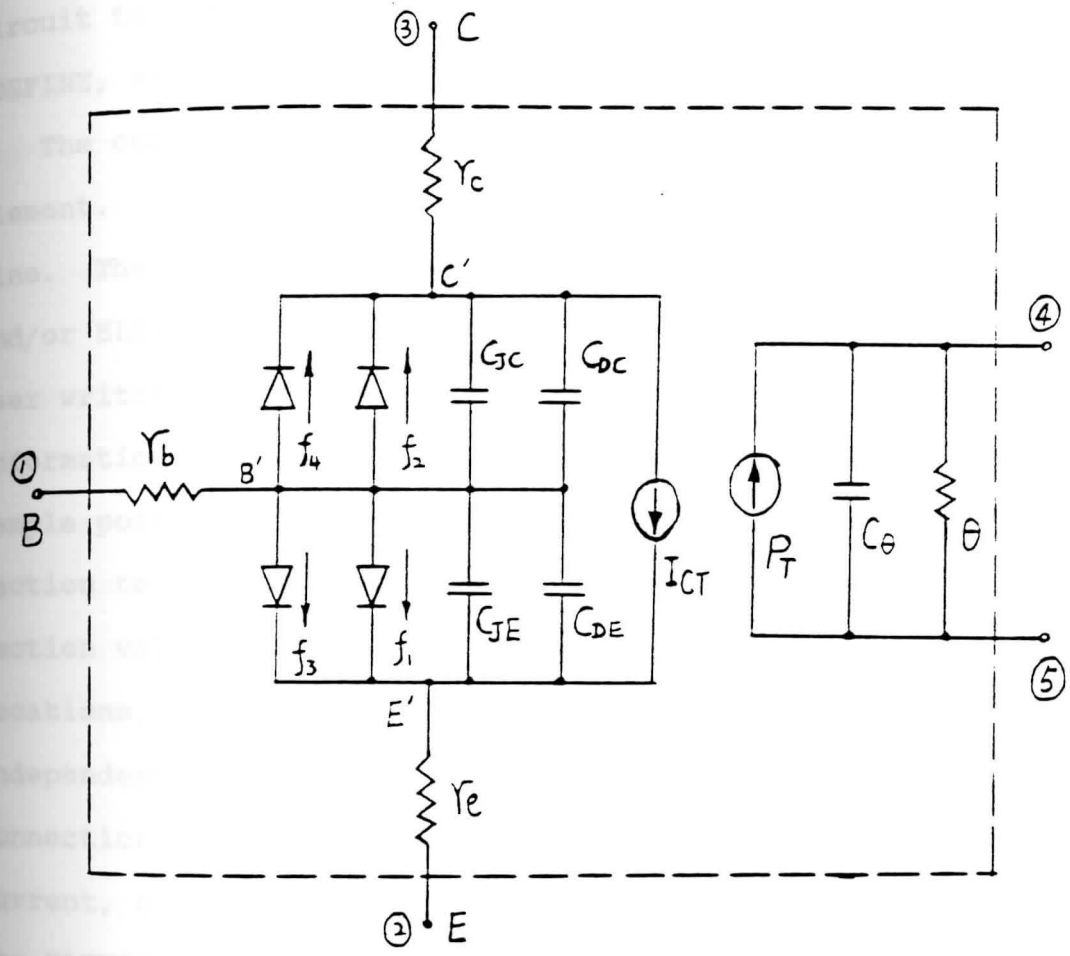

Figure 3-3. The NPN Type BJT Model with Self Heating

CHAPTER IV

WATAND NPNT AND PNPT MACROS

4.1 INTRODUCTION

WATAND macros provide for the creation of models and circuit topology descriptions. Control words such as #DEFINE, #MODEL and #DATA can be used in such a macro [3].

The control word #DEFINE is for creating a user-defined element. The element name follows the #DEFINE on the same line. The #DEFINE sections include MODEL, DATA, FUNCTION and/or ELEMENTS. The MODEL section defines the name of the user written subroutine to be used, storage location information, parameter names and their default values, and sample point names and their default values. The DATA section tells the information about the number of #DATA section values, the number of extra element-level storage locations, the number of external nodes, and a list of independent variables. The FUNCTION section allows the connection of four kinds of functions, J, Q, V, and F for current, charge, voltage, and flux sources, respectively. The ELEMENTS section allows the connection of built-in linear elements available in WATAND. It specifies the locations and values of the elements.

The WATAND #MODEL control word introduces the environment in which a model is defined. All models must be defined before the model is used in the circuit as an element in the #DATA section. The #DATA control word

describes the topology of a circuit and linear element values.

In Section 4.2, models for the npn and pnp bipolar junction transistors with self-heating characteristics are presented. Their numerical modeling equations are also given. In Section 4.3, the NPNT and PNPT WBLOCK files are presented. The #DEFINE and #MODEL sections are included in these WBLOCK files. A FORTRAN subroutine (GUPONT) which evaluates function values of the #DEFINE NPNT and PNPT elements is presented in Section 4.4.

4.2 NUMERICAL MODELING OF THE NPNT AND PNPT MODELS

Fig. 4-1 shows an npn type GP BJT model with the self-heating thermal equivalent circuit. It is a modification of the model in Fig. 3-3, mainly for WATAND computing and programming. Two short circuits are added for sampling collector and emitter currents during WATAND iteration. Two current sources J_C and J_E are used to replace five currents, f_1, f_2, f_3, f_4 and I_{CT}, presented in the model electrical circuit part of Fig. 3-3. Two charge sources Q_C and Q_E also replace the four capacitors in Fig. 3-3, Q_C for C_{JC} and C_{DC}, Q_E for C_{JE} and C_{DE}.

A similar model shown in Fig. 4-2 is established for the pnp type transistor model. Notice since the bias directions in the pnp type transistor are opposite to the npn type transistor, the directions of bias voltage,

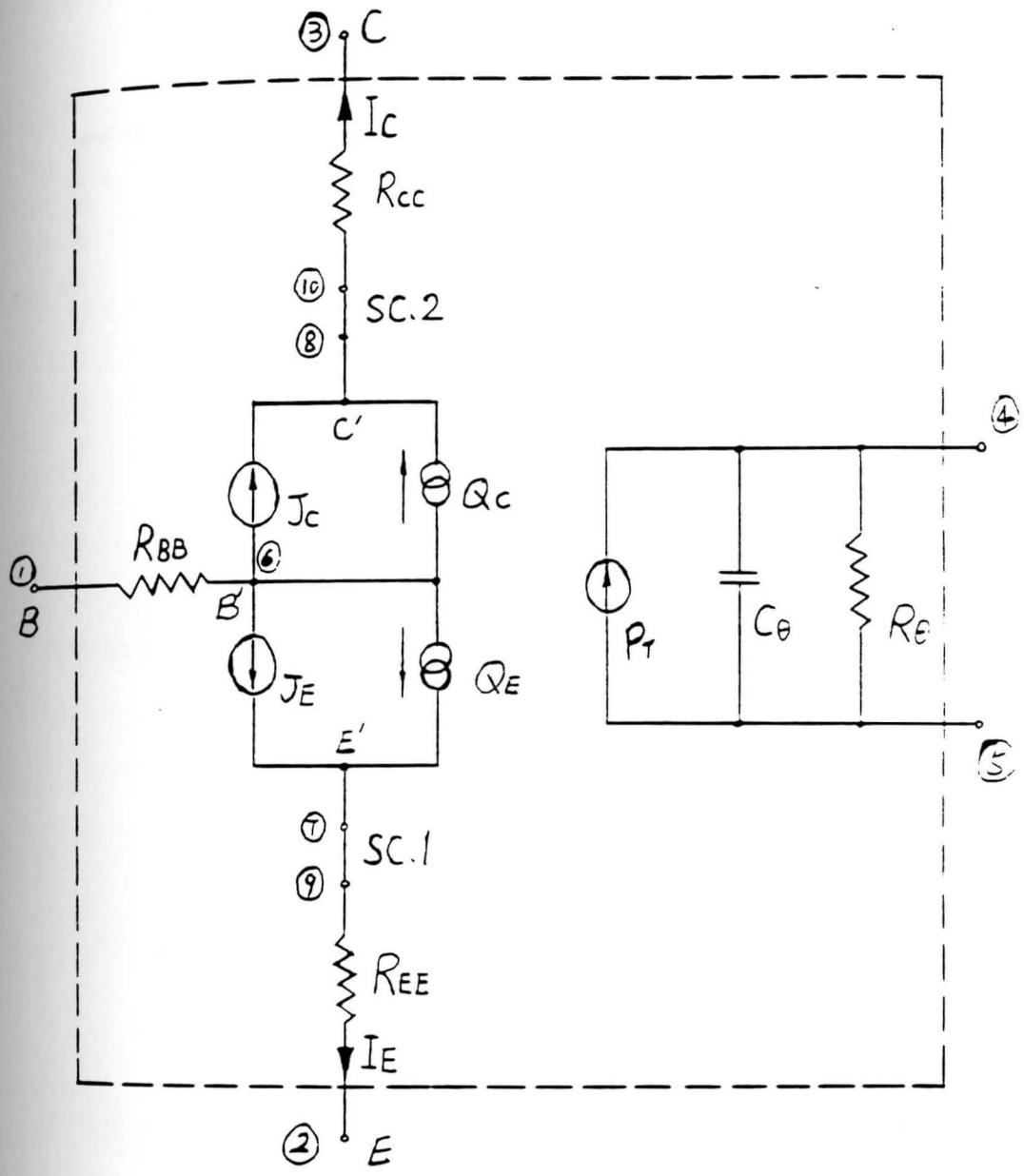

Figure 4-1. A Modified NPN BJT Model with Self Heating

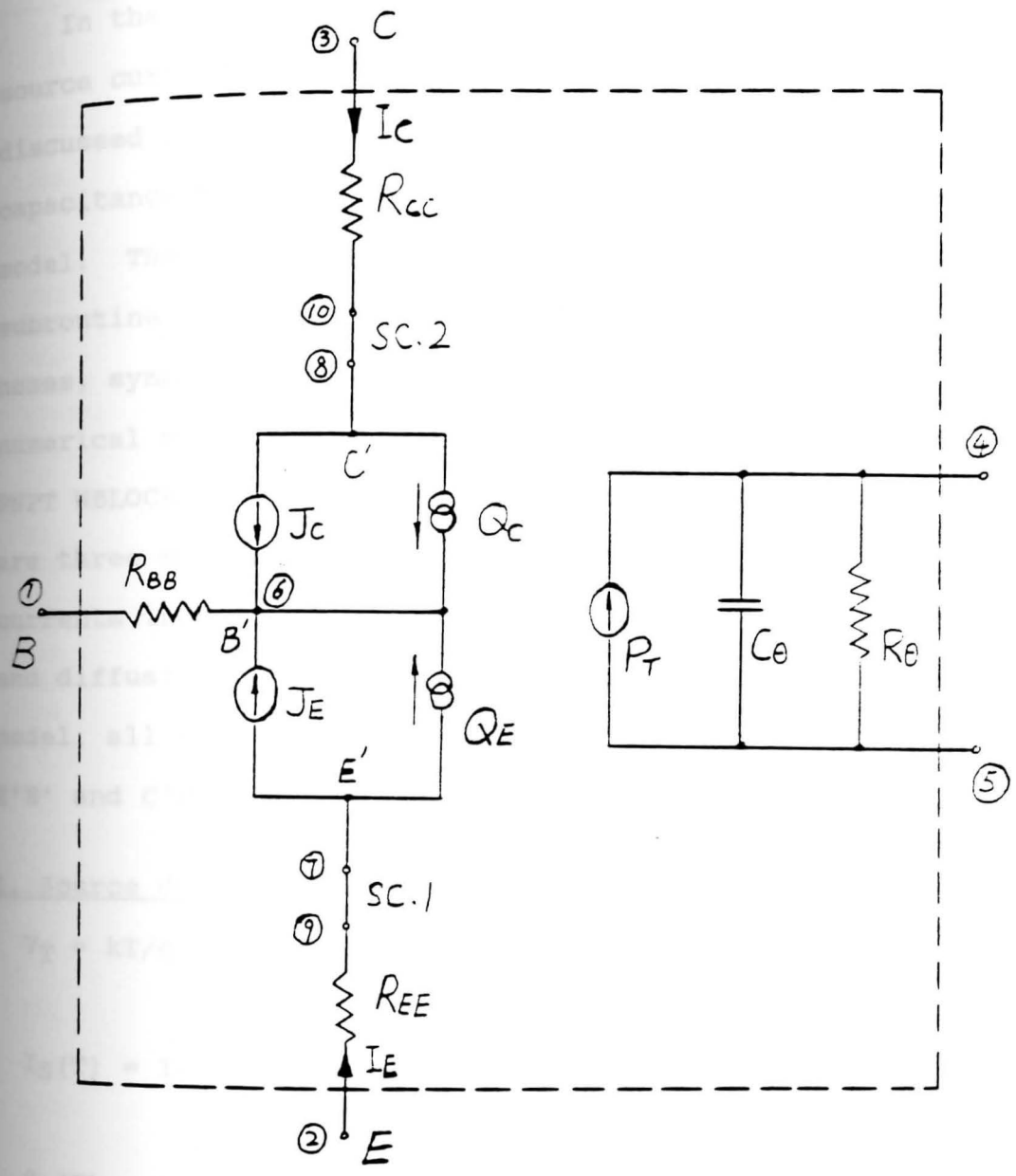

Figure 4-2. A Modified PNP BJT Model with Self Heating

current and charge sources (except for P_T and T_{JA}) are merely switched.

In the following numerical modeling equations, the source current equations are based on the GP model discussed in Chapter II, while the junction and diffusion capacitance relationships are mainly based on the EM_3 model. These equations are used by the GUPONT FORTRAN subroutine. Table 4-1 contains all the model parameter names, symbols and descriptions which are included in the numerical modeling equations as well as in the NPNT and PNPT WBLOCK files and GUPONT FORTRAN subroutine. Following are three groups of equations for modeling the source currents including dissipated power, junction capacitances, and diffusion capacitances in the NPNT model. For the PNPT model, all subscripts B'E' and B'C' are to be replaced by E'B' and C'B', respectively.

1. Source Currents

$$V_T = kT/q \qquad (k/q = 8.6164X10^{-5}) \tag{4.1}$$

$$I_S(T) = I_S \cdot \left[\frac{T}{T_0}\right]^3 \cdot \exp\left[\left[\frac{-E_g}{k}\right]\left[\frac{1}{T} - \frac{1}{T_0}\right]\right] \tag{4.2}$$

$$\beta_F(T) = \beta_F \cdot [1 + BTC1 \cdot (T-T_0) + BTC2 \cdot (T-T_0)^2] \tag{4.3}$$

$$I_{CC} = \frac{I_S(T)}{\beta_F(T)}\left[\exp\left[\frac{V_{B'E'}}{V_T}\right] - 1\right] = f_1 \tag{4.4}$$

$$I_{EC} = \frac{I_S(T)}{\beta_R}\left[\exp\left[\frac{V_{B'C'}}{V_T}\right] - 1\right] = f_2 \tag{4.5}$$

Table 4-1. Macromodel Parameters

Parameter Name	Symbol	Default Value	Unit	Descriptions
IS	I_S	1.6×10^{-14}	A	Saturation current
ISS	I_{SS}	0	A	Composite forward low saturation current I_S
MSS	M_{SS}	1	-	Forward low current emission coefficient
ISR	I_{SR}	0	A	Composite inverse low saturation coefficient
MSR	M_{SR}	1	-	Inverse low current emission coefficient
RBB	r_b	15	Ohms	Base resistance
REE	r_e	0.1	Ohms	Emitter resistance
RCC	r_c	1	Ohms	Collector resistance
THETA	Θ	0	K/W	Thermal resistance
CTHETA	C_Θ	0	Joule/K	Thermal capacitance
TE	T	0	K	Ambient Temperature
TJ	T_J	0	K	Junction temperature
BF	β_F	100	-	Forward current gain
BR	β_R	1	-	Reverse current gain
BTC	BTC1	0	-	1st order BF temperature coeff.
	BTC2	0	-	2nd order BF temperature coeff.
IKF	I_{KF}	1E40	A	Forward knee current
IKR	I_{KR}	1E40	A	Inverse knee current
VAF	V_A	1E40	V	Forward Early voltage
VAR	V_B	1E40	V	Inverse Early voltage
CE	C_{JE}	0	F	B-E junction capacitance at V_{JE}
	V_{JE}	0	V	V_{BE} for C_{JE}
	ϕ_E	0.8	V	B-E barrier potential
	m_E	0.33333	-	Exponent in B-E capacitance voltage law
TF	τ_F	0	s	Low current forward transit time
	F_{LEW}	0	-	Ratio of emitter length to base width
	$I_{K\tau F}$	I_K	A	Knee current for τ_F modification
CC	C_{JC}	0	F	B-C junction capacitance at V_{JC}
	V_{JC}	0	V	V_{BC} for C_{JC}
	ϕ_C	0.5	V	B-C barrier potential
	m_C	0.5	-	Exponent in B-C capacitance voltage law
TR	τ_R	0	s	Low current inverse transit time
	F_{LCW}	0	-	Ratio of collector length to base width
	$I_{K\tau R}$	I_{KR}	A	Knee current for τ_R modification

$$I_{E1} = I_{SS} \cdot \left[\exp\left[\frac{V_{B'E'}}{V_T . M_{SS}} \right] - 1 \right] = f_3 \qquad (4.6)$$

$$I_{C1} = I_{SS} \cdot \left[\exp\left[\frac{V_{B'C'}}{V_T . M_{SR}} \right] - 1 \right] = f_4 \qquad (4.7)$$

$$I_{CT} = \frac{1 - \frac{V_{B'C'}}{V_A} - \frac{V_{B'E'}}{V_B}}{\frac{1}{2} + \left[\frac{1}{4} + \frac{I_{CC}}{I_K} + \frac{I_{EC}}{I_{KR}} \right]^{\frac{1}{2}}} \cdot (I_{CC} - I_{EC}) \qquad (4.8)$$

$$J_C = f_2 + f_4 - I_{CT} \qquad (4.9)$$

$$J_E = f_1 + f_3 + I_{CT} \qquad (4.10)$$

$$P_T = I_C \cdot V_{C'B'} + I_E \cdot V_{B'E'} + I_B \cdot RBB^2 + I_C \cdot RCC^2 + I_E \cdot REE^2 \qquad (4.11)$$

2. Junction Capacitances

$$C_{JE} = \frac{C_{JE0}}{\left[1 - \frac{V_{B'E'}}{\phi_E} \right]^{m_E}} \qquad V_{B'E'} \leq \phi_E - .05 \qquad (4.12)$$

$$C_{JE} = K_1 \cdot V_{B'E'} + K_2 \qquad V_{B'E'} > \phi_E - .05 \qquad (4.13)$$

where

$$K_1 = \left. \frac{dC_{JE}}{dV_{B'E'}} \right|_{V_{B'E'} = \phi_E - .05} \qquad (4.14)$$

$$K_2 = -K_1 \cdot (\phi_E - .05) + C_{JE} \Big|_{V_{B'E'} = \phi_E - .05} \qquad (4.15)$$

$$C_{JC} = \frac{C_{JC0}}{\left[1 - \frac{V_{B'C'}}{\phi_C}\right]^{m_C}} \qquad V_{B'C'} \leq \phi_C - .05 \qquad (4.16)$$

$$C_{JC} = K_1 \cdot V_{B'C'} + K_2 \qquad V_{B'C'} > \phi_C - .05 \qquad (4.17)$$

where

$$K_1 = \left.\frac{dC_{JC}}{dV_{B'C'}}\right|_{V_{B'C'} = \phi_C - .05} \qquad (4.18)$$

$$K_2 = -K_1 \cdot (\phi_C - .05) + C_{JC}\Big|_{V_{B'C'} = \phi_C - .05} \qquad (4.19)$$

3. Diffusion Capacitances

$$C_{DE} = \tau_{Fac} \cdot \frac{dI_{CC}}{dV_{B'E'}} \qquad V_{B'E'} > 0 \qquad (4.20)$$

$$C_{DE} = 0 \qquad V_{B'E'} \leq 0 \qquad (4.21)$$

where

$$\tau_{Fac} = \tau_F \qquad I_{CC} \leq I_{K\tau F} \qquad (4.22)$$

$$\tau_{Fac} = \tau_F \cdot \left[1 + \frac{1}{4} \cdot (F_{LEW})^2 \cdot \left[\frac{I_{CT}}{I_{K\tau_F}} - 1\right]^2\right]$$

$$I_{CC} > I_{K\tau F} \qquad (4.23)$$

$$C_{DC} = \tau_{Rac} \cdot \frac{dI_{EC}}{dV_{B'C'}} \qquad V_{B'C'} > 0 \qquad (4.24)$$

$$C_{DC} = 0 \qquad V_{B'C'} \leq 0 \qquad (4.25)$$

where

$$\tau_{Rac} = \tau_R \qquad I_{EC} \leq I_{K\tau R} \qquad (4.26)$$

$$\tau_{Rac} = \tau_R \cdot \left[1 + \frac{1}{4} \cdot (F_{LCW})^2 \cdot \left[\frac{-I_{CT}}{I_{K\tau R}} - 1 \right]^2 \right]$$

$$I_{EC} > I_{K\tau R} \qquad (4.27)$$

4.3 THE NPNT AND PNPT WBLOCK FILES

The circuit of the npn type bipolar junction transistor model has been shown in Fig. 4-1. Following are explanations of the NPNT WBLOCK file shown in Table 4-2.

The #DE line defines the element type as NPNT. In the MODEL section, GUPONT is the FORTRAN subroutine name, followed by the number of model storage locations (14) used by the subroutine and then 23 parameter names, each with one or more values for a total of 34 parameter values. Next are five sample-point parameter names for the independent variables V_{BE}, V_{BC}, I_C, I_E and T_{JA} and their default values. The users can change these parameter and sample-point values interactively and/or in the WATAND file. Only three sample-point values are given for each independent variable which will make the model perform poorly; it is expected that a user will define reasonable sample points to work for a given transistor or use a previously written macro which does this. For example, in the next chapter the TH2N2222 WBLOCK file, a model for the 2N2222 transistor is presented and all five sample points are defined properly for computer simulations.

Table 4-2. The NPNT WBLOCK File

```
#*********************************************************************
#* This Gummel-Poon BJT model includes self heating due to dissipated
#* power.  It is based on the GPN model.  In the #Data section, enter
#*
#*  NPNT.mname.name  Bnode  Enode  Cnode  Tnode+  Tnode-
#*
#*  (V Tnode+ Tnode-) = junction minus ambient temperature
#*
#*  Created 23-May-90  F.Q. Ye  MS Thesis   YSU EE Dept.
#*********************************************************************
&MODEL
#DE NPNT
MODEL GUPONT 14 IS 1.6D-14  ISS 0  MSS 1  ISR 0  MSR 1
*               RBB 15  REE .1  RCC 1  THETA 0  CTHETA 0
*               TE 0  TJ 0  BF 100  BR 1  BTC 0 0
*               IKF 1D40  IKR 1D40  VAF 1D40  VAR 1D40
*               CE 0 0 .8 .33333  TF 0 0 1D40
*               CC 0 0 .5 .5  TR 0 0 1D40
*               VBE -1 0 1  VBC -1 0 1  IE -1 0 1  IC -1 0 1
*               TJA -1 0 1
DATA 0 0  5  6 7  6 8  A 1  A 2  4 5
FUNCTIONS
J  6  7
J  6  8
Q  6  7
Q  6  8
J  5  4
ELEMENTS
R  1  6  RBB
R  2  9  REE
SC 7  9
R  3 10  RCC
SC 8 10
R  4  5  14 MS
C  4  5  CTHETA
#M
NPNT.&MNAME &POSITION
#*********************************************************************
&DATA
&ERROR MISSING OR INVALID #MODEL DEFINITION FOR ELEMENT NPNT.&NAME
```

The DATA line tells that the element requires no #DATA section values, no extra storage locations, five external nodes, and three independent voltages and two auxiliary currents which make up the five independent variables. The directions of the three independent voltages are also specified. The FUNCTION lines give connections for each of the dependent current and charge sources.

The ELEMENTS section specifies the connections and values of linear elements. The values are taken from either the MODEL lines or from the model storage. The directions of the two auxiliary currents "A 1" and "A 2" are specified by two short circuits, "SC 7 9" and "SC 8 10", respectively. The value of resistor "R 4 5", which is the thermal resistance, θ, is obtained from the fourteenth model storage position in the subroutine GUPONT. This will be explained later in Section 4.3.

The PNPT WBLOCK file in Table 4-3 defines the pnp type BJT model shown in Fig. 4-2. The WBLOCK file is identical to the NPNT file except for the difference in directions of all independent voltages and current and charge sources (except P_T and T_{JA}). These are switched due to the difference in npn and pnp biasing.

The NPNT and PNPT WBLOCK files are macro or general models for the npn and pnp BJT models. For a specific type of bipolar junction transistor, the user only needs to specify model parameter values and sample-point values for the specific transistor.

Table 4-3. The PNPT WBLOCK File

```
#*********************************************************************
#* This Gummel-Poon BJT model includes self heating due to dissipated
#* power.  It is based on the GPP model.  In the #Data section, enter
#*
#*  PNPT.mname.name  Bnode  Enode  Cnode  Tnode+  Tnode-
#*
#*  (V Tnode+ Tnode-) = junction minus ambient temperature
#*
#*  Created 23-May-90  F.Q. Ye  MS Thesis   YSU EE Dept.
#*********************************************************************
&MODEL
#DE PNPT
MODEL GUPONT 14 IS 1.6D-14  ISS 0  MSS 1  ISR 0  MSR 1
*               RBB 15  REE .1  RCC 1  THETA 0  CTHETA 0
*               TE 0  TJ 0  BF 100  BR 1  BTC 0 0
*               IKF 1D40  IKR 1D40  VAF 1D40  VAR 1D40
*               CE 0 0 .8 .33333  TF 0 0 1D40
*               CC 0 0 .5 .5  TR 0 0 1D40
*               VEB -1 0 1  VCB -1 0 1  IE -1 0 1  IC -1 0 1
*               TJA -1 0 1
DATA 0 0  5  7 6  8 6  A 1  A 2  4 5
FUNCTIONS
J  7  6
J  8  6
Q  7  6
Q  8  6
J  5  4
ELEMENTS
R  1  6  RBB
R  2  9  REE
SC 9  7
R  3 10  RCC
SC 10 8
R  4  5  14 MS
C  4  5  CTHETA
#M
PNPT.&MNAME &POSITION
#*********************************************************************
&DATA
&ERROR MISSING OR INVALID #MODEL DEFINITION FOR ELEMENT PNPT.&NAME
```

4.4 THE GUPONT FORTRAN SUBROUTINE

The FORTRAN subroutine GUPONT is shown in Table 4-4. Since appropriate reversals for the directions of sample voltages, auxiliary sample currents, current and charge sources are made in the PNPT WBLOCK file, the subroutine is suitable for both NPNT and PNPT WBLOCK files.

The subroutine calculates values for the current and charge sources (P_T, J_E, J_C, Q_E and Q_C) at a certain junction temperature. It takes WATAND a certain number of iterations to reach a solution for a circuit, and the subroutine is called during each iteration. The subroutine is called in type 0, type 1, and type 2 situations, and each call sets the ICODE value to 0, 1, and 2, respectively [3].

The ICODE=1 call occurs from the #DATA section of the WATAND file during WInput and when #AModel or #Alter is used to set or alter any value of the element. Since neither case affects the NPNT or PNPT elements, no calculations occur, and the subroutine goes directly to RETURN.

ICODE=0 call happens at the #MODEL section of the WATAND file during WInput and when #AModel is used to set or alter any parameter and sample-point values for the model. Pre-calculation is needed for the model at this time. First, model input parameters TJ, the junction temperature, and TE, the ambient temperature, are checked, and either TJ or TE is selected for pre-calculating the

Table 4-4. The GUPONT FORTRAN File

```
C*********************************************************************
      SUBROUTINE GUPONT(ICODE,MPVAL,MSTOR,INDVAR,FUNVAL,DVAL,
     *                  DSTOR,MIDA,DERIV)
C*********************************************************************
C
C     ROUTINE CALCULATES VALUES FOR GUMMEL-POON NPNT AND PNPT MODELS.
C     THESE MODELS INCLUDE SELF HEATING, I.E., JUNCTION TEMPERATURE
C     CAN VARY WITH POWER DISSIPATED.
C
C
C     IN ADDITION TO STANDARD GPN/GPP PARAMETERS, THE FOLLOWING ARE
C     USED:
C
C     RBB      BASE SERIES RESISTANCE
C     REE      EMITTER SERIES RESISTANCE
C     RCC      COLLECTOR SERIES RESISTANCE
C     THETA    THERMAL RESISTANCE
C     CTHETA   THERMAL CAPACITANCE
C     TE       AMBIENT TEMPERATURE
C                WHEN TE <= 0, GLOBAL VALUE (#O TEMP) IS USED
C     TJ       JUNCTION TEMPERATURE
C                WHEN TJ <=0, THEN
C                  IF THETA <= 0, AMBIENT TEMPERATURE IS USED
C                  IF THETA > 0, SELF HEATING IS IN EFFECT
C     BTC1     FIRST ORDER BETA TEMPERATURE COEFFICIENT
C     BTC2     SECOND ORDER BETA TEMPERATURE COEFFICIENT
C
C     CREATED 23-MAY-90  F.Q. YE  MS THESIS  YSU EE DEPT.
C
C+++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++
      REAL*8 MPVAL(1),MSTOR(1),INDVAR(5),FUNVAL(5),DVAL(1),DSTOR(1),
     *         DERIV(1,1),
     *       TEMPO,TEMOLD,TEMPX,
     *       MP(34),MS(14),
     *       IS,ISS,MSS,ISR,MSR,RBB,REE,RCC,THETA,CTHETA,
     *         TE,TJ,BF,BR,BTC1,BTC2,IKF,IKR,VAF,VAR,
     *         CJE,VJE,PHIE,GAMMAE,TAUF,LEOWF,IKTF,
     *         CJC,VJC,PHIC,GAMMAC,TAUR,LEOWR,IKTR,
     *       VT,TEMP,ISTEMO,CE0,XTRE,KE1,KE2,VIKTF,
     *         CC0,XTRC,KC1,KC2,VIKTR,RTHETA,
     *       VBE,VBC,IE,IC,TJA,
     *       TEMPRT,IB,PT,VBEVT,VBCVT,JE,JC,JEC,QE,TT1,QC,
     *       VTMSS,VTMSR,DTEMP,BETAF
      INTEGER ICODE,MIDA(1),I
C
      EQUIVALENCE
     *(MP( 1),IS    ), (MP( 2),ISS   ), (MP( 3),MSS   ),
     *(MP( 4),ISR   ), (MP( 5),MSR   ), (MP( 6),RBB   ),
     *(MP( 7),REE   ), (MP( 8),RCC   ), (MP( 9),THETA ),
     *(MP(10),CTHETA), (MP(11),TE    ), (MP(12),TJ    ),
     *(MP(13),BF    ), (MP(14),BR    ), (MP(15),BTC1  ),
     *(MP(16),BTC2  ), (MP(17),IKF   ), (MP(18),IKR   ),
     *(MP(19),VAF   ), (MP(20),VAR   ), (MP(21),CJE   ),
```

```
     *(MP(22),VJE   ), (MP(23),PHIE  ), (MP(24),GAMMAE),
     *(MP(25),TAUF  ), (MP(26),LEOWF ), (MP(27),IKTF  ),
     *(MP(28),CJC   ), (MP(29),VJC   ), (MP(30),PHIC  ),
     *(MP(31),GAMMAC), (MP(32),TAUR  ), (MP(33),LEOWR ),
     *(MP(34),IKTR  )
      EQUIVALENCE
     *(MS( 1),VT    ), (MS( 2),TEMP  ), (MS( 3),ISTEMO),
     *(MS( 4),CE0   ), (MS( 5),XTRE  ), (MS( 6),KE1   ),
     *(MS( 7),KE2   ), (MS( 8),VIKTF ), (MS( 9),CC0   ),
     *(MS(10),XTRC  ), (MS(11),KC1   ), (MS(12),KC2   ),
     *(MS(13),VIKTR ), (MS(14),RTHETA)
C
      COMMON /TEMPBL/ TEMPO,TEMOLD,TEMPX
C+++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++
      DO 10 I=1,34
10    MP(I)=MPVAL(I)
      DO 15 I=1,14
15    MS(I)=MSTOR(I)
C
      IF(ICODE.EQ.1) GOTO 999
      IF(ICODE.EQ.2) GOTO 50
C+++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++
C...ICODE=0
C
      IF(TJ.GT.0D0) GOTO 20
      TEMPRT=TE
      IF(TE.LE.0D0) TEMPRT=TEMPO
      GOTO 30
20    TEMPRT=TJ
C
C...PREPARE VALUES
30    VT=TEMPRT*8.6164D-5
      TEMP=12882D0*(1D0/300D0-1D0/TEMPRT)
      IF(TEMP.GT.174D0) TEMP=174D0
      ISTEMO=IS*(TEMPRT/300D0)**3*DEXP(TEMP)
      VIKTF=IKTF
      IF(IKTF.GT..9D30) VIKTF=IKF
      VIKTR=IKTR
      IF(IKTR.GT..9D30) VIKTR=IKR
      XTRE=.05D0
      XTRC=.05D0
      CALL JNCNP(CJE,VJE,PHIE,GAMMAE,XTRE,CE0,KE1,KE2)
      CALL JNCNP(CJC,VJC,PHIC,GAMMAC,XTRC,CC0,KC1,KC2)
      RTHETA=1D0
      IF(THETA.GT.0D0) RTHETA=THETA
      DO 40 I=1,14
40    MSTOR(I)=MS(I)
      GOTO 999
C+++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++
C...ICODE=2
C
50    FUNVAL(5)=0D0
      VBE=INDVAR(1)
      VBC=INDVAR(2)
```

```
      IF(TJ.GT.0D0.OR.THETA.LE.0D0) GOTO 100
C
C...SELF HEATING--FIND POWER
      TEMPRT=TE
      IF(TE.LE.0D0) TEMPRT=TEMPO
      TJA=INDVAR(5)
      TEMPRT=TEMPRT+TJA
      VT=TEMPRT*8.6164D-5
      TEMP=12882D0*(1D0/300D0-1D0/TEMPRT)
      IF(TEMP.GT.174D0) TEMP=174D0
      ISTEMO=IS*(TEMPRT/300D0)**3*DEXP(TEMP)
      DO 60 I=1,3
60    MSTOR(I)=MS(I)
      IE=INDVAR(3)
      IC=INDVAR(4)
      IB=IE+IC
      PT=VBC*IC+VBE*IE+IE*IE*REE+IC*IC*RCC+IB*IB*RBB
      FUNVAL(5)=PT
C
C...EVALUATE FUNCTIONS
C
C...CURRENTS
100   VBEVT=VBE/VT
      IF(VBEVT.GT.174D0) VBEVT=174D0
      VBCVT=VBC/VT
      IF(VBCVT.GT.174D0) VBCVT=174D0
      JE=ISTEMO*(DEXP(VBEVT)-1D0)
      JC=ISTEMO*(DEXP(VBCVT)-1D0)
      JEC=1D0-VBC/VAF-VBE/VAR
      JEC=JEC/(.5D0+DSQRT(.25D0+JE/IKF+JC/IKR))
      JEC=JEC*(JE-JC)
C
C...CHARGES
      CALL JNCNQ(CE0,PHIE,GAMMAE,XTRE,KE1,KE2,VBE,QE)
      IF(VBE.LE.0D0) GOTO 110
      TT1=TAUF
      IF(JEC.GT.VIKTF)
     *   TT1=TAUF*(1D0+.25D0*LEOWF*LEOWF*(JEC/VIKTF-1D0)**2)
      IF(JEC.GT.0D0) QE=QE+TT1*JEC
C
110   CALL JNCNQ(CC0,PHIC,GAMMAC,XTRC,KC1,KC2,VBC,QC)
      IF(VBC.LE.0D0) GOTO 120
      TT1=TAUR
      IF(-JEC.GT.VIKTR)
     *   TT1=TAUR*(1D0+.25D0*LEOWR*LEOWR*(-JEC/VIKTR-1D0)**2)
      IF(JEC.LT.0D0) QC=QC-TT1*JEC
C
C...FINISH CURRENTS
120   VTMSS=VT*MSS
      VTMSR=VT*MSR
      VBEVT=VBE/(VTMSS)
      IF(VBEVT.GT.174D0) VBEVT=174D0
      VBCVT=VBC/(VTMSR)
      IF(VBCVT.GT.174D0) VBCVT=174D0
```

```
      DTEMP=TEMPRT-300D0
      BETAF=BF*(1+(BTC1+BTC2*DTEMP)*DTEMP)
      JE=JE/BETAF+ISS*(DEXP(VBEVT)-1D0)
      JC=JC/BR+ISR*(DEXP(VBCVT)-1D0)

C
C...USE ONLY TWO EQUIVALENT CURRENT SOURCES
      JE=JE+JEC
      JC=JC-JEC

C
C...AND PASS THEM BACK
      FUNVAL(1)=JE
      FUNVAL(2)=JC
      FUNVAL(3)=QE
      FUNVAL(4)=QC
999   RETURN
      END
```

temperature-variant saturation current, I_S. TJ will be selected if it is a nonzero positive value, otherwise, TE is selected. If TE is zero or negative, the WATAND #Option global temperature value is chosen [3]. The subroutine also calculates the initial values of C_{JC0} and C_{JE0} by calling a built-in WATAND subroutine JNCNP.

WATAND does not allow a resistance value of zero. So when θ is less or equal to zero which means that there is no self heating, the subroutine arbitrarily sets R_θ, which stands for the thermal resistance, θ, in the model circuit, to 1. The subroutine puts all fourteen pre-calculated values to model storage, which is from MS(1) to MS(14). The fourteenth model storage, or MS(14), stores either the actual nonzero thermal resistance value or the value 1.0 which has been set. In the ELEMENTS section of the NPNT or PNPT WBLOCK file, the value of "R 4 5", which is for θ, is

specified by 14 MS, the value in the model storage location 14.

A type-2 call (ICODE=2) occurs when the model or element is being entered into the circuit description by an analysis and when function values are required during an analysis. ICODE is equal to 2 during WATAND iterations. Under either of two circumstances there will be no self heating effect in the model, and the self-heating model will act like other nonthermal WATAND Gummel-Poon models (GP or GN). First, when TJ is greater than zero, the transistor junction temperature, T_J, is fixed at that value. This allows the user to specify TJ separately from the ambient temperature, TE. Second, when TJ is set to zero, and THETA is zero, there will be no self-heating effect. In this case, T_J is equal to T_A, i.e., the junction temperature is the same as the ambient temperature. For either of these two situations, the subroutine will skip the self-heating section which calculates the temperature variation. The operating temperature for computing the model function is then the value TEMPRT set in the ICODE=0 section.

If TJ is zero and THETA is greater than zero, there will be self heating in the model. In the "self-heating" section, the subroutine takes the five independent variable values, determines the junction temperature of the transistor, recalculates the temperature variant saturation

current (I_S), and evaluates the power dissipation within the transistor as the value of the current source P_T.

From the subroutine GUPONT line-label 100, the subroutine does all the calculation by using the equations presented in Section 4.2. The operating temperature value it uses is either the temperature set in the ICODE=0 section if there is no self heating or the calculated junction temperature if there is self heating. At the end, it provides current and charge source values (P_T, J_E, J_C, Q_E and Q_C) for WATAND iteration to analyze and solve the circuit.

CHAPTER V

MODEL PERFORMANCE

To demonstrate the self-heating model performance, several experiments are performed by using the 2N2222 transistor, and the laboratory experimental data is compared with WATAND and PSPICE computer simulation results. The 2N2222 is a common general purpose npn bipolar junction transistor, and there are several computer simulation models available for the transistor, such as T2N2222 in WATAND [13] and Q2N2222 and Q2N2222A in PSPICE [4]. The T2N2222 macro is a WATAND GP model. It is based on the GN1 macro which uses the GUPO1 FORTRAN subroutine. The PSPICE P2N2222 model used in this chapter is also a GP model.

In this chapter, a TH2N2222 WBLOCK file based on the NPNT macro to simulate the 2N2222 transistor is discussed in Section 5.1. It is also used in the examples in this chapter. In Section 5.2, the thermal steady state of a common-emitter circuit is tested experimentally and compared with WATAND and PSPICE simulations. The thermal transient response is also tested experimentally and its results are compared with WATAND simulations. In Section 5.3, a mirror current circuit in discrete components is tested experimentally and simulated in WATAND, and the results are compared. The same mirror current circuit on

an IC chip is analyzed in WATAND using the TH2N2222 model to verify the temperature stability of the circuit.

WATAND handles nonlinear elements by using piecewise-linear approximation. Sample points are set for each independent variable. The function values between sample points are interpolated linearly. Using more sample points gives a more accurate solution, but it increases the computing time generally. WATAND allows the user to change the sample-point density by using the control word "#Option DEnsity". For the WATAND analyses in this chapter, "#Option DENsity 5" for the sample points is used. This means that there are four more sample points between each sample-point interval as they are defined in the TH2N2222 or T2N2222 WBLOCK files.

5.1 THE TH2N2222 SELF-HEATING MODEL

The TH2N2222 WBLOCK file is based on the NPNT macro which uses the GUPONT subroutine to simulate 2N2222 transistor characteristics including self heating. The TH2N2222 model has the same circuit topology as the NPNT macromodel in Fig. 4-1. But in the TH2N2222 WBLOCK, parameter values and the five independent variables' sample points are different from those in the NPNT WBLOCK. The parameter values in the TH2N2222 WBLOCK are from the 2N2222 transistor. The five groups of sample points for independent variables (V_{BE}, V_{BC}, I_E, I_C and T_{JA}) are also set properly so that "rough" but reasonably precise results

can be obtained. In this chapter, the global density of sample points is increased to 5 so that "smoother" and more accurate results can be obtained.

Table 5-1 is the TH2N2222 WBLOCK file. The &PARAM lines define the macro variable names for 23 input parameters and five independent variables. These names are the same as those in the NPNT WBLOCK file. The &DEFAULT lines give default values for the input parameters and for sample points of the independent variables. The #M section specifies the NPNT macromodel with these default values or user specified values for the 2N2222 transistor.

In the following sections, both laboratory experimental data and computer simulation results are presented. Three different models are used to simulate the 2N2222 transistor. These models are WATAND self-heating TH2N2222, WATAND T2N2222, and PSPICE P2N2222. In order to compare the results, seven common input parameters in the three models are set to the same values. The seven input parameters are I_S, V_{AF}, V_{AR}, B_F, B_R, R_B, R_E, and R_C. Three critical parameter values, the saturation current, I_S, the forward Early voltage, V_{AF}, and the forward current gain, β, are measured at room temperature for the transistor(s) used in the laboratory experiments by means of a Tektronix 577 curve tracer [2]. The rest of the input parameters in the three models are kept at their default values.

Table 5-1. The TH2N2222 WBLOCK File

```
#*********************************************************************
#*  This 2N2222 model uses the self-heating NPNT BJT model.
#*  In the #Data section, enter
#*
#*  TH2N2222.mname.name  Bnode  Enode  Cnode  Tnode+  Tnode-
#*
#*  Created on 23-May-90  F.Q. Ye  MS Thesis   YSU EE Dept.
#*********************************************************************
&MODEL
&PARAM IS ISS MSS ISR MSR RBB REE RCC THETA CTHETA TE TJ
*      BF BR BTC IKF IKR VAF VAR CE TF CC TR VBE VBC IE IC TJA
&DEFAULT IS 3.0D-14 ISS 0 MSS 1 ISR 0 MSR 1
*        RBB 15 REE .1 RCC 1 THETA 160 CTHETA 9.375D-2
*        TE 0D0 TJ 0D0 BF 110 BR 4 BTC 6.67D-3 -3.6D-6
*        IKF 1D40 IKR 1D40 VAF 370 VAR 25
*        CE 17P -1 .6 .33333 TF 0 0 1D40
*        CC 10P -1 .8 .5 TR 0 0 1D40
*        VBE -1 0 IN .2 .6 IN .02 .76 LE 1 HE .05
*        VBC -40 IN 5 -1 IN .1 1 LE 5 HE .1
*        IE  -1M 0 IN 5M 100M LE 10M HE 10M
*        IC  -100M IN 5M 0 1M LE 10M HE 10M
*        TJA -10 0 IN 5 150 LE 10 HE 10
#M
NPNT.&MNAME &POSITION IS &IS ISS &ISS MSS &MSS ISR &ISR MSR &MSR
*           RBB &RBB REE &REE RCC &RCC THETA &THETA CTHETA &CTHETA
*           TE &TE TJ &TJ BF &BF BR &BR BTC &BTC IKF &IKF
*           IKR &IKR VAF &VAF VAR &VAR CE &CE TF &TF CC &CC TR &TR
*           VBE &VBE VBC &VBC IE &IE IC &IC TJA &TJA
#*********************************************************************
&DATA
NPNT.&MNAME.&NAME &POSITION
```

5.2 A COMMON-EMITTER CIRCUIT

Fig. 5-1 is a simple common emitter circuit which is used for steady-state and transient response experiments, and for WATAND and PSPICE analyses using the TH2N2222, T2N2222 and P2N2222 models. It is drawn to show all the circuitry and nodes necessary for all the tests carried out with this circuit. But the two external nodes of the transistor, nodes 0 and 900, are for the self-heating model

TH2N2222 only. Table 5-2 is the PSPICE file using the P2N2222 model; tables 5-3 and 5-4 are WATAND files using the T2N2222 and the TH2N2222 models, respectively.

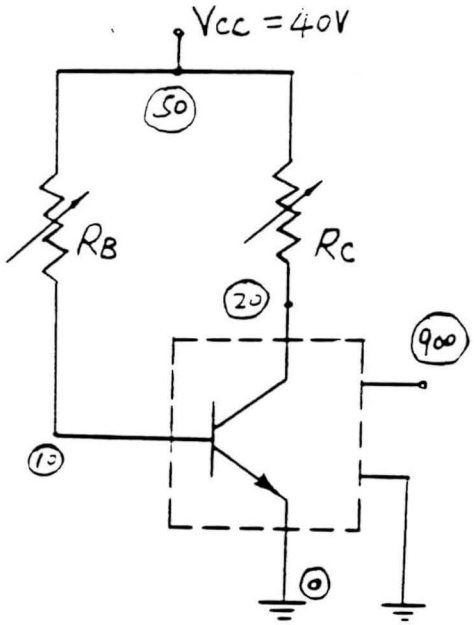

Figure 5-1. A Common-Emitter Circuit

Table 5-2. The EXP1.CIR File

```
Pspice Analysis of a Common-Emitter Circuit
Vcc   50   0   40
Rb    50  10   581k
Rc    50  20   1k
Q1    20   10   0   P2N2222
.model P2N2222 NPN(Is=3e-14 Vaf=370 Bf=110 Var=25 Br=4 Rc=1
+                    Re=0.1 Rb=15)
.op
.end
```

Table 5-3. The EXP1N2 WATAND File

```
#* FILE: EXP1N2 WATAND
#T SIMPLE COMMON-EMITTER CIRCUIT USING STANDARD BJT MODEL T2N2222
#T THE CIRCUIT IS USED FOR THERMAL STEADY-STATE AND TRANSIENT ANALYSES
#M
 T2N2222.M IS 3D-14 BF 110 BR 4 QB 1D40 1D40 370 25
#D
 V.CC  50    0   DC 40
 R.B   50   10   581K
 R.C   50   20   1K
 T2N2222.M.1 10   0   20
#E
 #G RB R.B
 #G RC R.C
 #G VCC V 50
 #G VBE V 10
 #G VCE V 20
 #GI IB I R.B
 #GI IC I R.C
 #G BETA G IC / G IB
 #G PT G IC * G VCE + G IB * G VBE
 DC OU G RB G RC G IC G VBE G BETA G PT PR IT 1000
 TC IP ZERO EN 100 DE .1 NO OU G IC G VBE G VCE G PT KE OU ON D IT 1000
 DI OU G IC G VCE IB .0074 .0080 VB 29.5 33.0 XB -1 100 US TC ON D PL
#S
```

Table 5-4. The EXP1N2T WATAND File

```
#* FILE: EXPN2T WATAND
#T SIMPLE COMMON-EMITTER CIRCUIT USING SELF-HEATING MODEL TH2N2222
#T THE CIRCUIT IS USED FOR THERMAL STEADY-STATE AND TRANSIENT ANALYSIS
#M
 TH2N2222.M
#D
 V.CC  50   0  DC 40
 R.B   50  10  581K
 R.C   50  20  1K
 TH2N2222.M.1 10  0  20  900 0
#E
 #G RB R.B
 #G RC R.C
 #G VCC V 50
 #G VBE V 10
 #G VCE V 20
 #GI IC I R.C
 #GI IB I R.B
 #G BETA G IC / G IB
 #GI PT G IC * G VCE + G IB * G VBE
 #G TEMP V 900 + 300
 DC OU G RB G RC G IC G VBE G BETA G PT PR IT 1000
 TC IP ZERO EN 100 DE .1 NO OU G IC G VBE G VCE G PT G TEMP
*   KE OU ON D IT 1000
 DI OU G IC G VCE US TC ON D IB .0075 .011 VB 29.5 32.5 XB -1 100 PL
#S
```

5.2.1 THERMAL STEADY STATE ANALYSIS

The common-emitter circuit in Fig. 5-1 with no emitter resistance and a large base resistance has poor temperature stability, and self heating has a significant effect on the Q-point [14]. The experiment measured transistor performance at different power dissipations which vary the junction temperature. During the experiment, the collector current was kept at 10.0 mA for different load resistances, R_C. This was fulfilled by altering base resistance, R_B. Decade-box resistors were used to vary R_B and R_C. Since

the collector current is kept constant, the variation of load resistance changes the transistor power dissipation, and therefore the junction temperature, base-emitter voltage, current gain and other characteristics. As the temperature has significant effect on the Q-point, it took time to adjust R_B in order to get the collector current established at 10.0 mA for a certain R_C. That is, time was required for the circuit to reach its thermal steady state for each change of R_B. A minimum of 10 minutes was needed after the last adjustment of R_B before experimental data was taken. By measuring V_{BE} and V_{RC} for each setting of R_B and R_C in the experiment, the collector current, I_C, the current gain, β, and the power dissipation, P_T, can be calculated as

$$I_C = \frac{V_{RC}}{R_C} \tag{5.1}$$

$$\beta = \frac{I_C}{I_B} = \frac{\dfrac{V_{RC}}{R_C}}{\dfrac{V_{CC} - V_{BE}}{R_B}} = \frac{V_{RC} \cdot R_B}{R_C \cdot (V_{CC} - V_{BE})} \tag{5.2}$$

$$P_T = I_C \cdot V_{CE} + I_B \cdot V_{BE} \tag{5.3}$$

In Tables 5-5 to 5-8, the analysis results for P_T, I_C, V_{BE}, and β are compared with experimental results. In the

Table 5-5. Comparison of Power Dissipation P_T

R_B (Ω)	R_C (Ω)	P_T (mW) Exp.	P_T (mW) TH2N2222	Error (%)	P_T (mW) T2N2222	Error (%)	P_T (mW) P2N2222	Error (%)
620k	600	340	343	0.9	265	-22.1	264	-22.4
599k	800	320	326	1.9	260	-18.8	260	-18.8
581k	1.0k	300	307	2.3	253	-15.7	253	-15.7
550k	1.5k	250	253	1.2	227	- 9.2	227	-9.2
522k	2.0k	200	200	0.0	196	-2.0	196	-2.0
492k	2.5k	150	147	-2.0	158	5.3	158	5.3
474k	3.0k	100	99	-1.0	115	15.0	115	15.0
450k	3.5k	50	51	2.0	64	28.0	64	28.0

Table 5-6. Comparison of Collector Current I_C

R_B (Ω)	R_C (Ω)	I_C (mA) Exp.	I_C (mA) TH2N2222	Error (%)	I_C (mA) T2N2222	Error (%)	I_C (mA) P2N2222	Error (%)
620k	600	10.0	10.10	1.0	7.44	-25.6	7.44	-25.6
599k	800	10.0	10.27	2.7	7.67	-23.3	7.67	-23.3
581k	1.0k	10.0	10.38	3.8	7.87	-21.3	7.87	-21.3
550k	1.5k	10.0	10.36	3.6	8.22	-17.8	8.22	-17.8
522k	2.0k	10.0	10.29	2.9	8.56	-14.4	8.56	-14.4
492k	2.5k	10.0	10.27	2.7	8.95	-10.5	8.95	-10.5
474k	3.0k	10.0	10.07	0.7	9.17	-8.3	9.17	-8.3
450k	3.5k	10.0	9.98	-0.2	9.50	-5.0	9.50	-5.0

Table 5-7. Comparison of Base-Emitter Voltage V_{BE}

R_B (Ω)	R_C (Ω)	V_{BE} (V) Exp.	V_{BE} (V) TH2N2222	Error (%)	V_{BE} (V) T2N2222	Error (%)	V_{BE} (V) P2N2222	Error (%)
620k	600	0.589	0.588	-0.2	0.678	15.1	0.679	15.3
599k	800	0.593	0.596	0.5	0.679	14.5	0.680	14.7
581k	1.0k	0.599	0.604	0.8	0.680	13.5	0.680	13.5
550k	1.5k	0.614	0.619	0.8	0.682	11.1	0.682	11.1
522k	2.0k	0.629	0.634	0.8	0.683	8.6	0.683	8.6
492k	2.5k	0.646	0.649	0.5	0.685	6.0	0.685	6.0
474k	3.0k	0.660	0.662	0.3	0.686	3.9	0.686	3.9
450k	3.5k	0.677	0.675	-0.3	0.687	1.5	0.687	1.5

Table 5-8. Comparison of Forward Current Gain β

R_B (Ω)	R_C (Ω)	β Exp.	β TH2N2222	Error (%)	β T2N2222	Error (%)	β P2N2222	Error (%)
620k	600	157	159	1.3	117	-25.5	117	-25.5
599k	800	152	156	2.6	117	-23.0	117	-23.0
581k	1.0k	147	153	4.1	116	-21.1	116	-21.1
550k	1.5k	140	145	3.6	115	-17.9	115	-17.9
522k	2.0k	132	136	3.0	114	-13.6	114	-13.6
492k	2.5k	125	128	2.4	112	-10.4	112	-10.4
474k	3.0k	120	121	0.8	111	-7.5	111	-7.5
450k	3.5k	114	114	0.0	109	-4.4	109	-4.4

experiment, the power dissipation, P_T, varies from 50mW to 340 mW. For thermal steady-state analysis, the equation

$$T_J - T_A = \Theta \cdot P_T \qquad (5.4)$$

can be applied. When the ambient temperature, T_A, is 300 K (27°C), and the thermal resistance, Θ, is 160 K/W, the transistor junction temperature, T_J, varies from 308 K (33°C) to 354.4 K (81.4°C).

From the four tables, it can be concluded that the TH2N2222 self-heating model tracks the experimental circuit variations well with respect to junction temperature variations. The maximum error is less than 5%. For V_{BE}, it is less than 1%.

The analysis results of I_C, V_{BE} and β using the nonthermal T2N2222 and P2N2222 models vary significantly from the experimental data. As the transistor temperature increases, the error also increases. Neither the T2N2222 nor the P2N2222 models track the transistor and circuit well. Notice that the results from the T2N2222 and

P2N2222 models are almost identical. This is not surprising since these (nonthermal) models are based on the Gummel-Poon model and they are quite similar.

5.2.2 THERMAL TRANSIENT ANALYSIS

The second experiment used the same circuit in Fig. 5-1 to measure the turn-on transient response of the circuit due to thermal effects. When the transistor is not dissipating power, its junction temperature is equal to the ambient environment temperature. After the power supply is turned on, the transistor junction temperature begins to rise. It takes a period of time for the transistor to reach its steady-state temperature because of the thermal capacitance in the transistor. Normally, the thermal time constant is in seconds. During that period of time, the transistor Q-point will also vary due to temperature variation.

In this experiment, only one set of values for R_B and R_C was used. Their values were set to 581k and 1k, respectively. An X-Y plotter was used to graph the thermal transient responses of V_{BE} and V_{CE} during the first 100 seconds of circuit operation.

WATAND transient analyses (TC) were also run using both the T2N2222 and TH2N2222 models. In TC analysis, the default value for time step "DElta" is

$$\text{DELTA} = \frac{\text{Time Period}}{50} \qquad (5.5)$$

For a 100 second period, the default would be 2.0 seconds, but it was set to 0.1 second to improve the smoothness and accuracy of the thermal transient response. In the WATAND display post-processor (DI), the time axis was set to begin before zero. This made a clear display of the transient response starting from 0 seconds. The vertical voltage bounds (VB) and current bounds (IB) were also set properly so that the varying part of transient responses would be displayed in detail. Tables 5-3 and 5-4 show these settings.

Figs. 5-2 and 5-3 are experimental graphs of V_{BE} and V_{CE} obtained with an X-Y plotter. From the graphs, the measured thermal time constant is about 15 seconds. Since the thermal resistance is 160 K/W, the thermal capacitance is therefore set to 0.09375 Joule/K in the TH2N2222 WBLOCK file. Figs. 5-4 to 5-6 show the self-heating TH2N2222 model results of I_C, V_{BE}, V_{BC} and temperature responses. As the relationship between I_C and V_{CE} is simple,

$$I_C = \frac{V_{CC} - V_{CE}}{R_C} \qquad (5.6)$$

it can be calculated that the experimental value of I_C is also close to the computer simulation result. Fig. 5-6 shows the way the junction temperature rises. The junction temperature of the transistor was not measured because it could not be easily done.

Figs. 5-7 to 5-8 are the T2N2222 results of I_C, V_{BE}

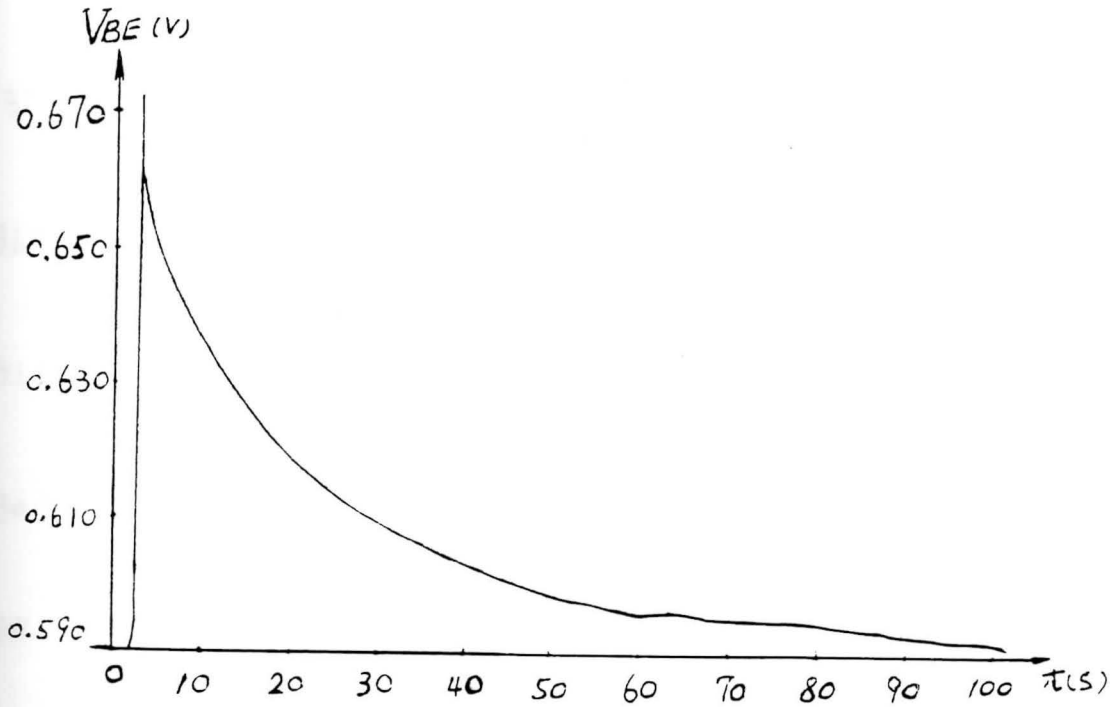

Figure 5-2. Experimental Result of Thermal Transient Response of V_{BE}

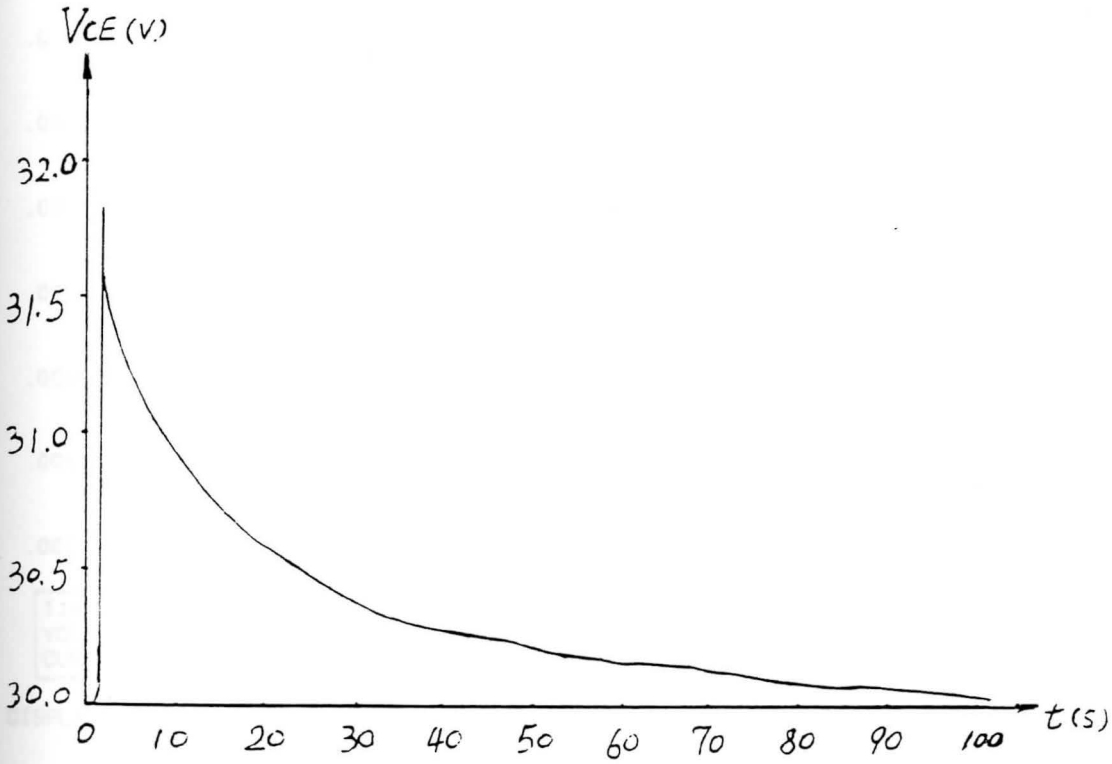

Figure 5-3. Experimental Result of Thermal Transient Response of V_{CE}

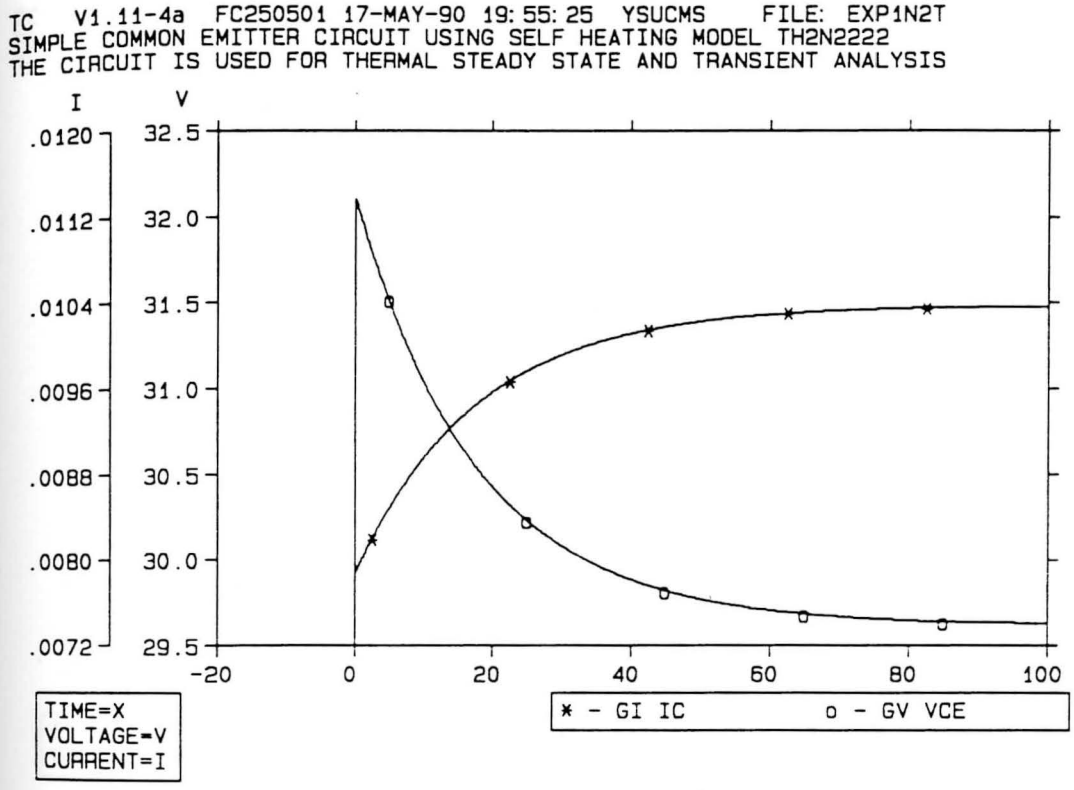

Figure 5-4. Thermal Transient Response of I_C and V_{CE} Using the Self-heating TH2N2222 Model

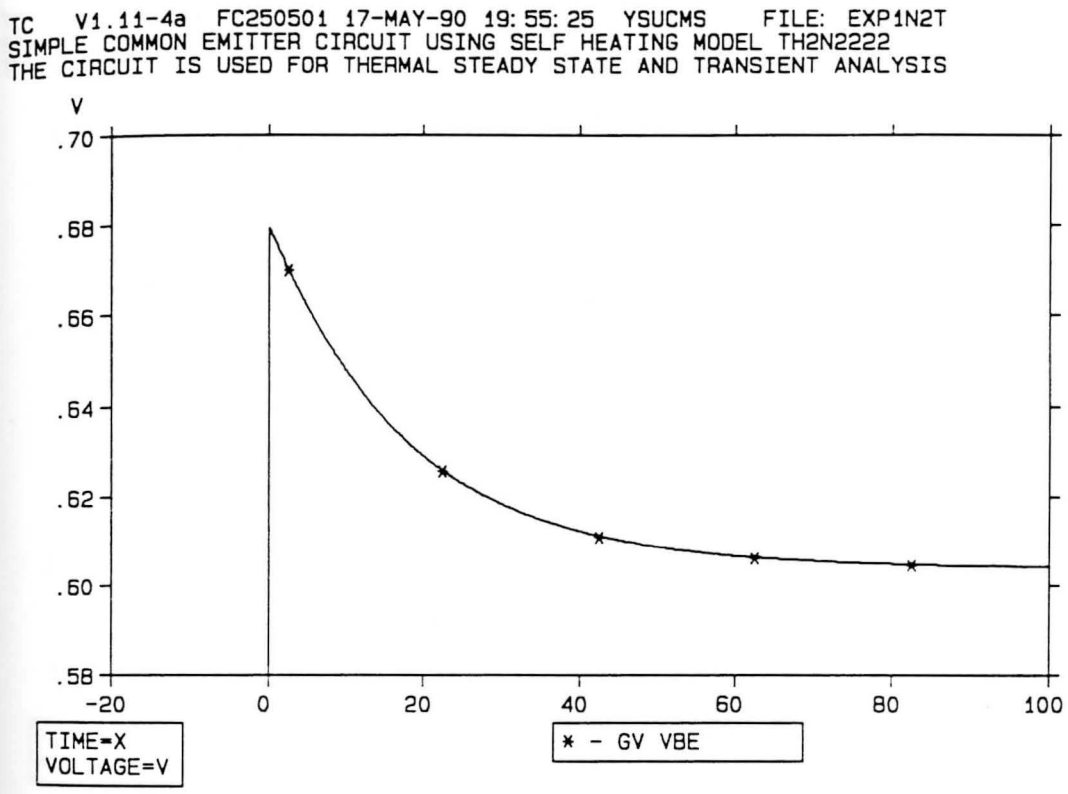

Figure 5-5. Thermal Transient Response of V_{BE} Using the Self-heating TH2N2222 Model

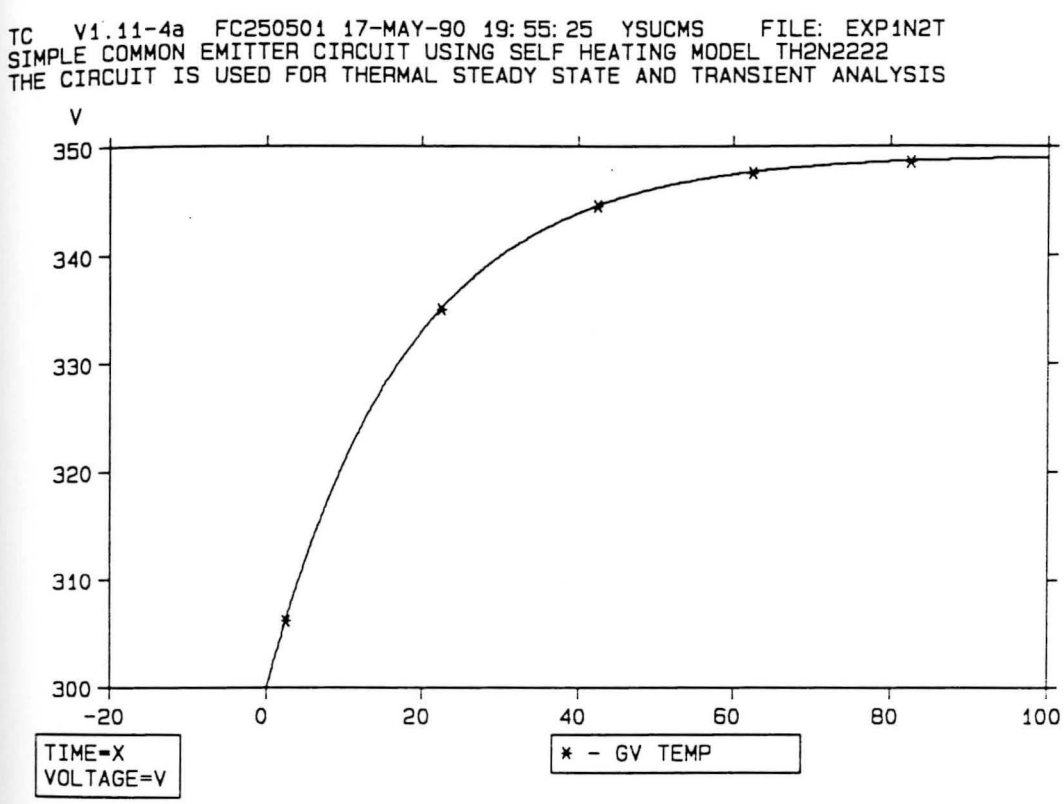

Figure 5-6. Thermal Transient Response of Temperature Using the Self-heating TH2N2222 Model

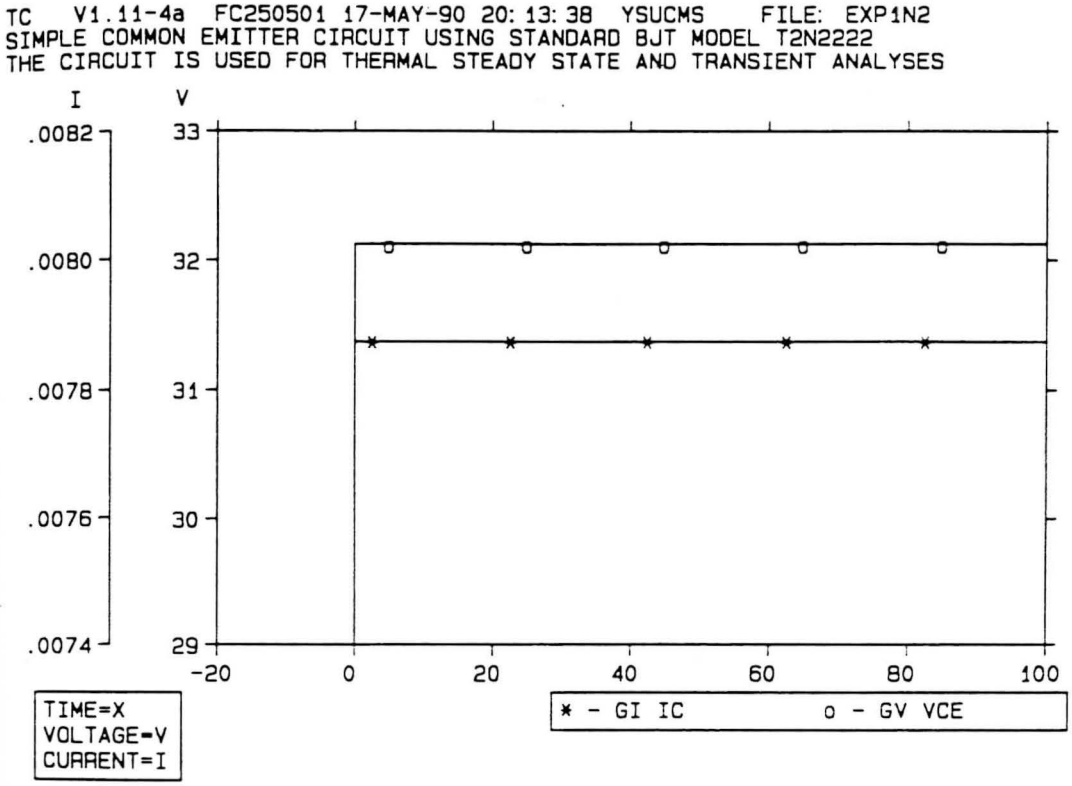

Figure 5-7. Thermal Transient Response of I_C and V_{CE} Using the Nonthermal T2N2222 Model

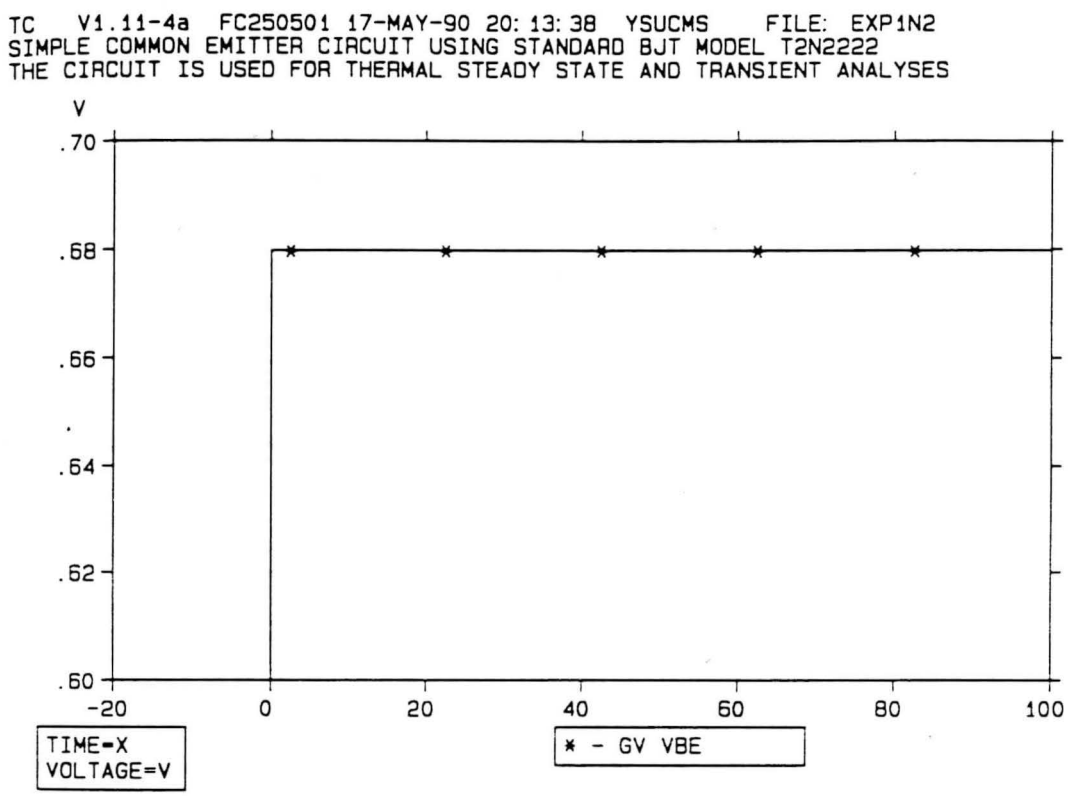

Figure 5-8. Thermal Transient Response of V_{BE} Using the Nonthermal T2N2222 Model

and V_{CE}. There is of course no thermal transient response because there is no thermal modeling in this case.

5.3 MIRROR CURRENT CIRCUIT

The next example is to test the mirror current circuit shown in Fig. 5-9. The TH2N2222 and T2N2222 models are used for WATAND analyses of the circuit. Their WATAND files are shown in Tables 5-9 and 5-10, respectively. The mirror current circuit is commonly used in integrated circuit (IC) design as a current source. The two transistor bases and emitters would be fabricated on the same chip so they would have the same model parameters and base-emitter voltage, and therefore, the same collector current. That is, the output current, I_{out}, is about the same value as the reference current, I_{ref}. Theoretically, the circuit on an IC chip has good temperature stability [15].

The first purpose of the example is to test the thermal characteristics of the circuit when it is built with discrete components instead of on an IC chip; The second purpose is to run the circuit in WATAND in order to verify the temperature stability of the circuit on an IC chip by using the self-heating model TH2N2222.

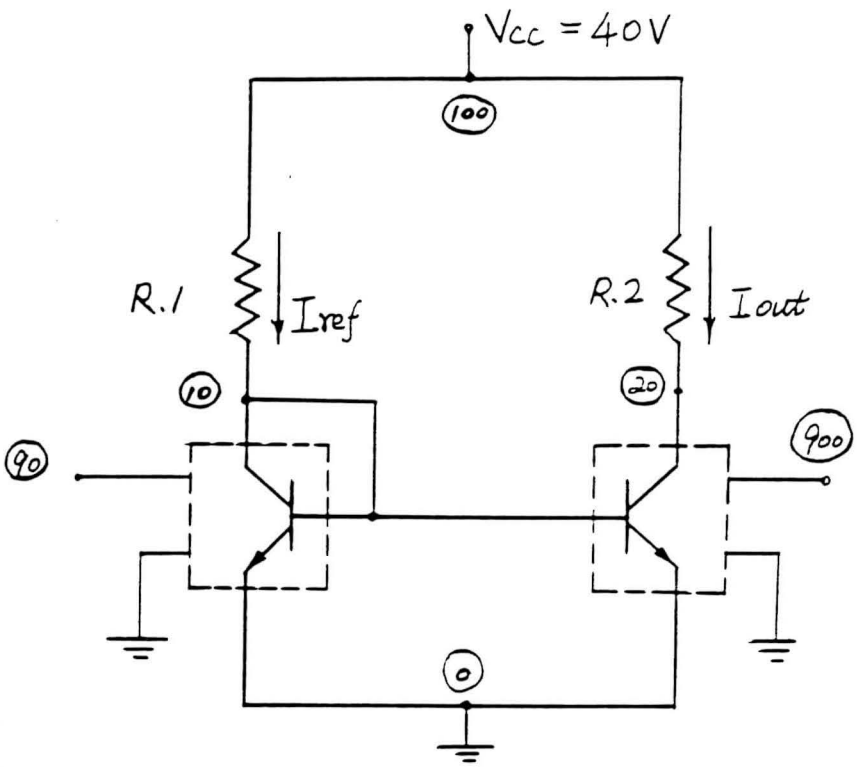

Figure 5-9. The Mirror Current Circuit

Table 5-9. The EXP3 WATAND File

```
#* FILE: EXP3 WATAND
#T MIRROR CURRENT CIRCUIT USING STANDARD BJT MODEL T2N2222
#M
 T2N2222.M  IS 3D-14 BF 110 BR 4 QB 1D40 1D40 370 25
#D
 V.CC  100   0  DC 40
 R.1   100  10   2K
 R.2   100  20   2K
 T2N2222.M.1  10  0  10
 T2N2222.M.2  10  0  20
#E
 #GI IREF I R.1
 #GI IOUT I R.2
 #G  R.1  R.1
 #G  R.2  R.2
 DC OU G R.1 G IREF G IOUT PR IT 1000
#S
```

Table 5-10. The EXP3T WATAND File

```
#* FILE: EXP3T WATAND
#T MIRROR CURRENT CIRCUIT USING SELF-HEATING MODEL TH2N2222
#M
 TH2N2222.M
#D
 V.CC  100   0  DC 40
 R.1   100  10   2K
 R.2   100  20   2K
 TH2N2222.M.1  10  0  10  90   0
 TH2N2222.M.2  10  0  20  900  0
#E
 #GI IREF I R.1
 #GI IOUT I R.2
 #G  R.1  R.1
 #G  R.2  R.2
 DC OU G R.1 G IREF G IOUT PR IT 1000
#S
```

5.3.1 MIRROR CURRENT CIRCUIT WITH DISCRETE COMPONENTS

To test the circuit with discrete components, V_{BE} and V_{R2} were measured. The reference current, I_{ref}, and output current, I_{out}, can be calculated as

$$I_{ref} = \frac{V_{CC} - V_{BE}}{R1} \tag{5.7}$$

$$I_{out} = \frac{V_{R2}}{R2} \tag{5.8}$$

Table 5-11 includes three different groups of reference and output currents obtained from the laboratory experiment and from WATAND analyses using the T2N2222 and TH2N2222 models.

Table 5-11. Reference and Output Current Results for the Mirror Current Circuit

R.1 (Ω)	Experiment		TH2N2222			T2N2222		
	I_{ref}(mA)	I_{out}(mA)	I_{ref}(mA)	I_{out}(mA)	Error (%)	I_{ref}(mA)	I_{out}(mA)	Error (%)
2.0k	19.6	19.4	19.6	19.6	1.0	19.6	19.3	-0.5
2.7k	14.7	18.8	14.6	18.9	0.5	14.6	14.7	-21.8
4.0k	9.8	17.9	9.8	17.9	0.0	9.8	10.1	-40.2
8.0k	4.9	16.1	4.9	15.9	-1.2	4.9	5.2	-67.7
16.0k	2.4	13.8	2.5	13.4	-2.9	2.5	2.6	-81.9
20.0k	2.0	13.1	2.0	12.3	-6.1	2.0	2.1	-84.0

From Table 5-11, it is easy to get the conclusion as in the previous examples that the TH2N2222 model follows the experimental circuit situation well. The error of I_{out} in the TH2N2222 model results vary from +1.0% to -6.1%. But in the T2N2222 model results, the error can be as high as 84.0%. The T2N2222 model is not able to track the experimental circuit using discrete transistors.

5.3.2 MIRROR CURRENT CIRCUIT ON AN IC CHIP

To verify the temperature stability of the circuit when it is fabricated on an IC chip, the two transistors must have the same temperature. This can be easily modeled by connecting the thermal equivalent circuits in the two TH2N2222 models together. Therefore, the dissipated powers are added and the junction temperatures of the two transistors are the same. Figure 5-10 shows the circuit that the two transistors' thermal equivalent circuits have two common nodes, nodes 900 and 0. Table 5-12 is the WATAND file of the circuit. Because the two thermal equivalent circuits are in parallel, the thermal resistance value is changed to 320 K/W in each model so that the total thermal resistance remains at 160 K/W. Although the thermal resistance on an IC chip would probably not be 160 K/W, for the convenience of comparing with the results in the previous sub-section, the total thermal resistance value is kept at 160 K/W. Table 5-13 gives analysis

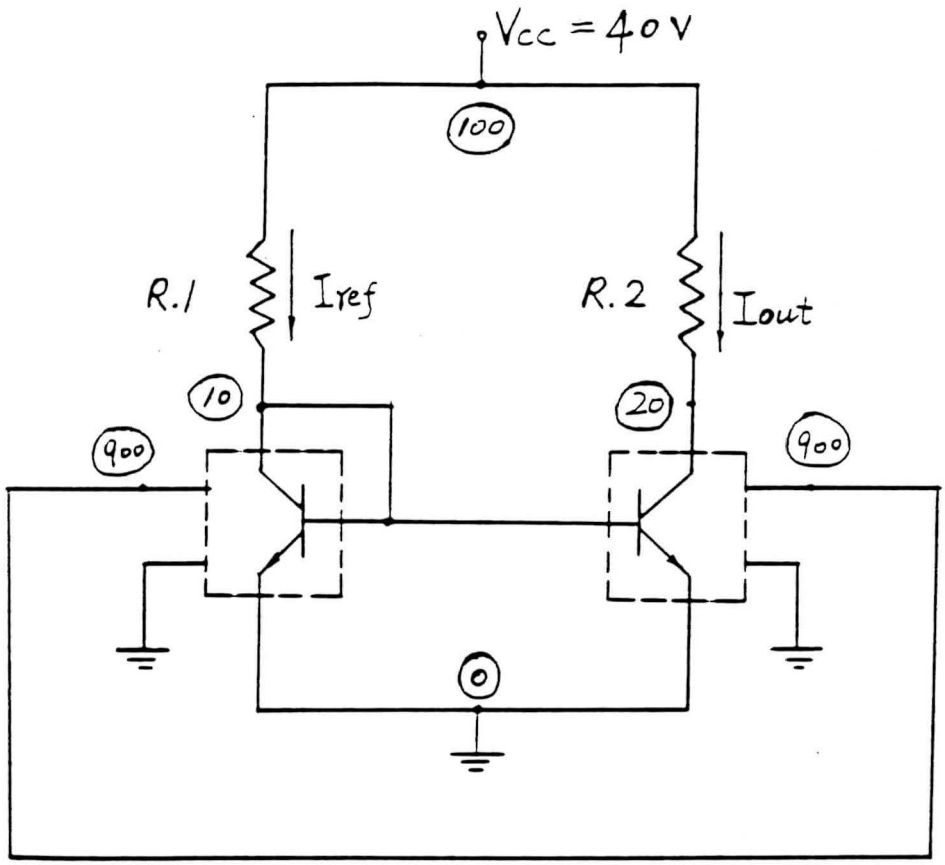

Figure 5-10. A Mirror Current Circuit on an IC Chip

Table 5-12. The EXP4T WATAND File

```
#* FILE: EXP4T WATAND
#T MIRROR CURRENT CIRCUIT USING TH2N2222 MODEL AND CONNECTING TWO
#T THERMAL CIRCUIT TOGETHER TO CHECK THE TEMPERATURE STABILITY
#M
 TH2N2222.M THETA 320
#D
 V.CC  100   0  DC 40
 R.1   100  10   2K
 R.2   100  20   2K
 TH2N2222.M.1  10  0  10  900  0
 TH2N2222.M.2  10  0  20  900  0
#E
 #GI IREF I R.1
 #GI IOUT I R.2
 #G  VBE V 10
 #G  VCE1 V 10
 #G  VCE2 V 20
 #G  PT G IREF * G VCE1 + G IOUT * G VCE2
 #G  TEMP V 900 + 300
 #G  R.1 R.1
 #G  R.2 R.2
 DC OU G R.1 G IREF G IOUT G VBE G PT G TEMP PR IT 1000
#S
```

Table 5-13. WATAND Results of the Mirror Current Circuit on an IC Chip Using the TH2N2222 Model

R.1	I_{ref} (mA)	I_{out} (mA)	V_{BE} (V)	P_T (mW)	Temp. (K)
2.0k	19.65	19.34	0.698	39.4	306
2.7k	14.57	14.71	0.655	165.0	326
4.0k	9.84	10.19	0.632	206.2	333
8.0k	4.92	5.23	0.625	157.5	325
16.0k	2.46	2.65	0.623	93.4	315
20.0k	1.97	2.12	0.622	77.1	312

results for reference current, I_{ref}, output current, I_C, base-emitter voltage, V_{BE}, two transistors' power dissipation, P_T, and junction temperature, Temp., at different R.1 values. The value of R.2 was kept at 2 kΩ.

Table 5-13 shows that despite the variation of power dissipation and temperature, the output current follows the reference current well. The results of using the TH2N2222 self-heating model are about the same as the analysis results using the nonthermal T2N2222 model. This verifies that the mirror current circuit fabricated on an IC chip has good temperature stability. When analyzing circuits with good temperature stabilities, it may be more economical to use a T2N2222 model because a model without self heating is simpler and consumes less computing time. However, the self-heating model can be very useful for verification in these kinds of situations.

CHAPTER VI

CONCLUSION

The bipolar junction transistor thermal characteristics and its thermal equivalent circuit have been discussed. Two macromodels, the NPNT and PNPT WBLOCK files, have been designed to simulate BJT performance including self heating. The self-heating models are able to calculate BJT junction temperature during the circuit operation, account for temperature dependency in the modeling equations and give automatic temperature adjustment to transistor parameters including saturation current, I_S, and forward current gain, β.

The TH2N2222 WBLOCK file, which is based on the NPNT macromodel and has specific parameter data for the 2N2222, has been developed, and comparison has been made with experimental data from two circuits using 2N2222 transistors. Common-emitter and mirror current circuits were used in several experiments to get experimental data for the 2N2222 transistor thermal steady-state and transient responses. The experimental results were compared with WATAND and PSPICE analyses results using different models for the 2N2222 transistor. The TH2N2222 self-heating model was also used to test the temperature stability of the mirror current circuit fabricated on an IC chip.

Comparing the thermal steady-state results, the error with respect to experimental data is less than 7% for the self-heating model. But for the nonthermal models, it can be up to 84%. As temperature increases, error also increases. The self-heating model can also track the thermal transient response correctly, while there is no thermal transient response shown in the results using the nonthermal models.

Further study and work could be done to improve the self-heating model by including base-collector breakdown, and making more components such as the three junction resistors (r_b, r_e and r_c), the junction capacitors (C_{JE} and C_{JC}) and the forward transit time (τ_F) sensitive to junction temperature. Further testing of the self-heating model could also be carried out with other circuits, e.g., power amplifiers and digital circuits.

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