RESONANT POWER MOSFET DRIVERS FOR LED LIGHTING

by

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Abstract

LED lighting has a promising future in consumer markets. Many researchers have conducted researches to improve the LED driver efficiencies. In this thesis, a computer model of a high efficiency resonant power LED driver is developed. The LED driver circuit is constructed and simulated at 20 kHz to 35 kHz of switching frequencies of the MOSFET. The OrCAD 16.2 is used as simulation software. The computer simulations show that the efficiency of the resonant power LED driver is considerably higher compare to that of conventional LED resistive drivers. The MOSFET used in the LED driver circuit has three different models: MOSFET SPICE level 1, level 3 and commercial MOSFET SPICE model (IRF6668). The output power of the LED driver is controlled by the switching frequencies of the MOSFETs and the simulation results suggest that the power resonant LED driver with commercial MOSFET can achieve up to 90% overall system efficiency.

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Chapter 1 Introduction

Today, the lighting industry is trying to increase the efficiency of lighting systems with better lighting quality and reduction of environmental pollution. Currently, the main lighting market is dominated by incandescent lamps, compact fluorescent lamps (CFLs), and light emitting diodes (LEDs). Although almost 90% of residential light in the United States still uses incandescent bulbs, they are being replaced gradually by other high efficient lighting devices, which are creating opportunity for the next generation of lighting technology such as CFLs and LEDs. CFLs have a faster growing market compared to LEDs despite the high efficiency of LEDs in terms of their power consumption and light quality. The disadvantage of LEDs is the high acquisition cost. But if long term cost is considered, LEDs are in fact significantly cheaper. Thus, the LED-based lighting technology has a promising future as it has long life and high energy efficiency [1].

The first known LED was made in 1907 in Marconi Lab by British experimenter H.J Round. In the early 1960s, the first commercially available light-emitting diode was developed. In 1962, the first practical visible-spectrum (red) LED was developed by Nick Holonyak, Jr., while working at General Electric Company [2].

There are numerous drivers developed for LED lighting. Among the different power driver topologies and control schemes, resonant power LED drivers are considered to be the best driver topology with minimum EMI contributions and switching losses [3, 4]. The driver in this thesis is a resonant power MOSFET driver. The driver has been designed in such a way that the output power is controlled by the switching frequency of

the MOSFET. In this topology, power losses within a circuit are minimized to attain high efficiency compared to other drivers where current is set by a series variable resistor. The simulation is done using software called OrCAD 16.2. The driver consists of the power MOSFET H-bridge, of which switching frequency of a MOSFET can be controlled by a gate control circuit. The resonance frequency of the LED load circuit is determined by the values of series inductor (Ls) and capacitor (Cs). The resonant frequency of the LED load circuit can be characterized by the following equation,

$$F_{res} = \frac{1}{2\pi\sqrt{LsCs}} \quad (1)$$

Where,

Ls = Series inductor

Cs = Series capacitor

To set the resonant frequency at 20 kHz, the values for series inductance and capacitance were calculated to be 30 µH and 2.11µF [5]. The diodes are considered to be in parallel to each other with a current regulator to overcome the cumulative voltage drop [6, 7]. The H-bridge alternately generates positive and negative pulses with a peak-peak value of 40 V. Pulse width varies according to the switching frequency of MOSFETs**.** By varying the switching frequency, the circuit can behave as a resistive, capacitive or inductive load.

In this thesis, the MOSFET driver only drives an inductive load. The computer PSpice simulation with ideal circuit components reveals that the operating frequency range is between 20 kHz and 35 kHz. In this frequency range, the output power can be controlled from 28 W to 754 W.

Figure 1 (a) shows the schematics for a classic resistive LED driver where current is set by using variable series resistance. As the variable resistor changes value, the current through the LED changes, therefore, the output power level changes. However, the I^2R losses on the variable resistor increase extremely with the current. The basic concept of the resonant power MOSFET driver design is shown by Figure 1(b). Voltage sources V pulse1 and V pulse2 represent the power MOSFET H-bridge which is controlled by the switching frequency. Both the inductor and the capacitor are energy storage devices, therefore, the only power consumers are the LEDs. From the comparison of the classic LED drivers and the power resonant LED drivers, Figure 1 (b) will have higher efficiency than Figure 1 (a), even if the switching losses and other stray resistances are considered.

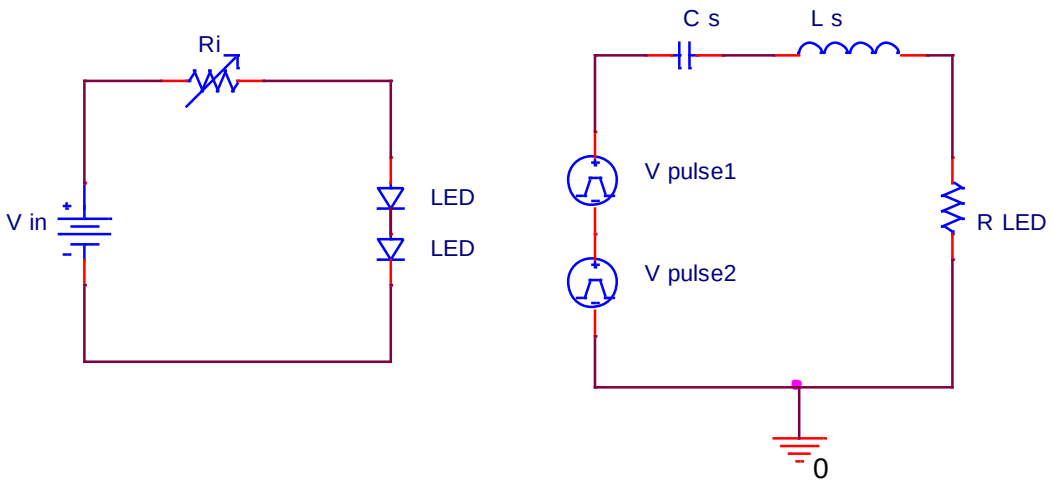

Figure 1. (a) Schematic for LED resistive driver, in which the current is set by a series variable resistor, (b) Schematic for basic resonant MOSFET driver

In ideal case, the LED driver control pulses are generated by using two ideal pulse voltage generators with a period of T (=1/switching frequency) but delay of T/2 in one of the generators.

This thesis explains the concept behind the frequency-driven resonant MOSFET driver. Once the driver is designed, the efficiency is calculated using first and second generation MOSFETs. As a first generation MOSFET, MOSFETs with MOS level 1 and MOS level 3 SPICE model are used. Likewise, as a second generation MOSFET, a commercial MOSFET (IRF6668) is used. Finally, the efficiency of drivers with various MOSFETs and the conventional driver is explained.

In short, Chapter 1 gives the brief introduction about the thesis and its content. Chapter 2 gives the brief introduction of MOSFET, SPICE and different MOSFET SPICE models. In chapter 3, we discuss about the basic driver design and simulation which explain the concept of power resonant MOSFET driver. Also the power resonant MOSFET driver circuit design along with its various components and its operation are discussed in chapter 3. In chapter 4, we discuss the computer simulation results of power resonant MOSFET drivers using the MOSFETs with various MOSFET SPICE models such as MOS level 1, MOS level 3 and the commercial MOSFET model. Chapter 6 gives the conclusion with the possible future work based on this research.

Chapter 2 Power MOSFET Modeling

2.1 MOSFET

MOSFET stands for Metal-Oxide Semiconductor Field-Effect Transistor, which is a special type of field effect transistor. The MOSFET was first proposed and patented by Lilienfeld and Heil in 1930. It was successfully demonstrated in the 1960s, 30 years after its invention. During the 1960s and 1970s, the designers were highly focused in integrated circuit design. NMOS was the dominant technology used for highly complex digital circuits. In the 1980s, CMOS transistors became popular because of their low static power consumption, simple laws of scalability and stability of operations. CMOS technology is also very useful for analog and RF circuits. Today most integrated circuits depend on MOS technology. Another application for the MOSFET is amplification or switching electronic signals in power applications [8]. Figure 2 shows the basic MOSFET structure with a gate, drain, source, substrate and metal oxide.

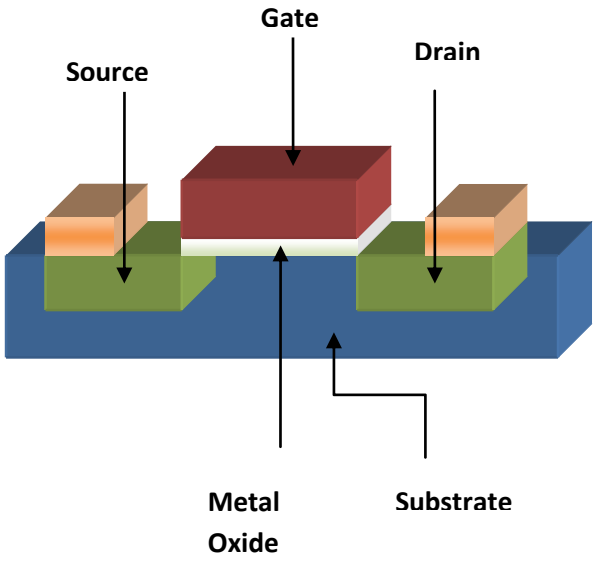

Figure 2. MOSFET structure

A MOSFET is controlled by varying the width of channel along with the charge carriers' flow. Charge carriers may be holes or electrons. The wider the channel is, the better the device conduction will be. For an NMOS MOSFET, the charge carriers enter the channel at the source and exit through the drain. The width of the channel is controlled by the voltage on an electrode which is called the gate and is connected between the source and drain. The gate is insulated from the channel by a very thin layer of metal oxide.

A typical MOSFET operates in two different modes, the depletion mode and the enhancement mode. In the depletion mode, when there zero voltage at the gate, the channel shows maximum conductance. As the voltage on the gate increases, the channel's conductivity decreases. In the enhancement mode, if there is no voltage on the gate, there will be no conduction. When the gate-to-source voltage greater than threshold voltage is applied to the gate, the channel will start conducting. The reverse can be observed in the depletion mode: as the voltage on the gate increases, the channel conductivity also increases. MOSFETs can be used as very fast and efficient switches for switching power purposes.

Between the two different modes of operation, the enhancement mode is the most common. Figure 3 shows the plot for drain current (I_{ds}) vs. drain-to-source voltage (V_{ds}) for several values of gate-to-source voltage ($V_{GS} - V_t$). V_t represents threshold voltage [9].

From the plot in Figure 3, the cutoff, linear and saturated regions can easily be identified. In the cutoff region where $V_{gs} \leq V_t$, there is no conduction other than very low

leakage current. The linear region where $V_{ds} < V_{gs} - V_t$, shows ohmic behavior and the saturation region where $V_{ds} \geq V_{gs} - V_t$, shows that the current is approximately constant.

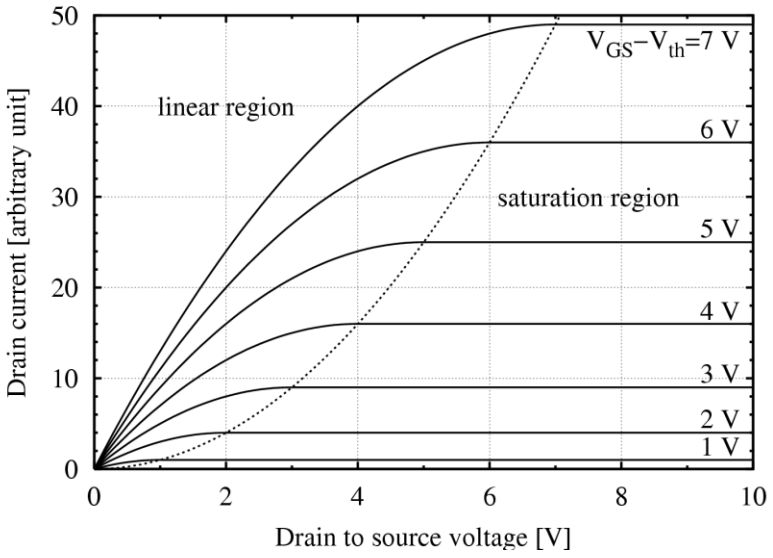

Figure 3. Drain current vs. drain-to-source voltage for several values of $V_{GS} - V_{th}$

2.2 SPICE

SPICE stands for the Simulation Program with Integrated Circuit Emphasis which is a standard computer program for electrical and electronic circuit simulations. When the circuit is not very large and complex, it can be built on a bread board for circuit tests and evaluations. Today, SPICE is a very important tool for modeling devices accurately, especially in integrated circuit designs. It has become a powerful tool that provides accurate simulation results in a reasonable amount of computation time. Today most designers rely on SPICE before they build the actual prototype.

In SPICE, a circuit is described as a collection of various elements connected at various nodes. Most electrical software simulation utilizes mathematical models to

replicate the behavior of an actual electronic device or circuit. A basic model provides a mathematical description of the element's behavior in circuits. Various simulation tools are commercially available in the market. OrCAD PSpice was used for the purpose of designing and evaluating the simulation of power MOSFET driver circuit for LED lighting.

2.3 MOSFET SPICE Models

For a specific component, there are a set of SPICE parameters which allow a simulator to predict its behavior. This set of SPICE parameter values for a specific component is known as a SPICE model. Many SPICE parameters are based on the physical characteristics of the component.

Different MOSFET SPICE models have been developed, and some of the commonly used MOSFET models are level 1, level 2, level 3, BSIM, HSPICE level 28, and BSIM 2, among others. Each model has its own process and electrical parameters. Each parameter contributes to the behavior of the circuit or component.

There are three historical generations of MOSFET models: first-generation, second-generation, and third-generation [10]. The first-generation model is a simple model compared to second and third generations. It merely describes a set of very simple, physically related parameters. This generation of model consists of level 1, level 2 and level 3 models. The second-generation model brings in a large number of electrical parameters. It focuses more on extensive mathematical conditioning to improve the robustness and convergence behaviors of the model when used in circuit simulation. This

generation of model consists of BSIM, HSPICE level 28 and BSIM2. The third-generation model is still under development.

Figure 4 shows the schematic of a typical MOSFET model.

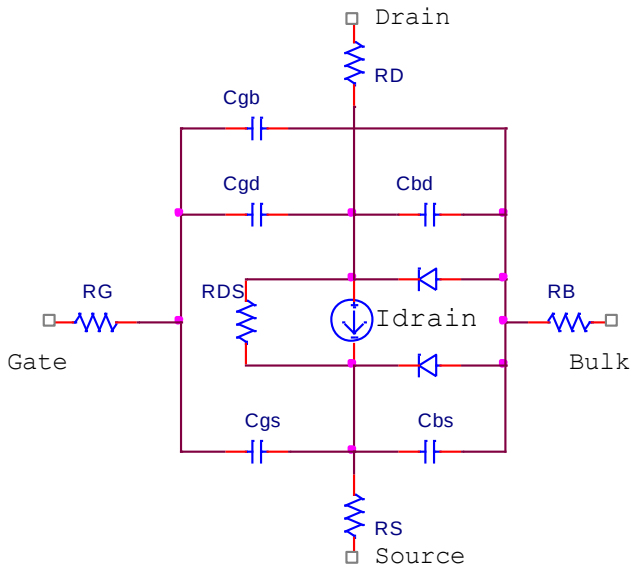

Figure 4. A MOSFET model

The MOSFET is modeled as intrinsic ohmic resistances in series with the drain, source, gate and substrate represented by RD, RS, RG and RB respectively. RDS represents the shunt resistance paralleled with the drain and source. Cgb, Cgd, Cbd, Cbs and Cgs represent the capacitance between gate-bulk, gate-drain, bulk-drain, bulk-source and gate-source respectively [11].

The level 1 model is the simplest MOSFET model for the SPICE circuit simulator. This model can explain the dependence of current on gate voltages greater than the threshold voltage. This level 1 model is used when accuracy is less important than simulation time. Table 1 shows the list of the level 1 model parameters [10]. This level 1

model represents the Shichman-Hodges model and is based on the gradual channel approximation and square law for the saturated drain current model.

Table 1: SPICE level 1 model parameter

Parameter	**Units**	**Description**
Process Parameter		
TPG	m	Type of gate material
TOX	m	Gate oxide thickness
NSUB	cm^2	Substrate doping concentration
XJ	m	Source/Drain junction depth
Electrical Parameter		
UO	$cm^2/V.s$	Zero bias low field mobility
VTO	V	Threshold voltage, long wide device, zero substrate bias
LAMBDA	V^{-1}	Channel length modulation/ output conductance parameter
CGSO	F/m	Zero bias gate-source capacitance
CGDO	F/m	Zero bias gate-drain capacitance
CGBO	F/m	Zero bias gate-bulk capacitance

The equation below gives the drain current model of MOSFET.

At cutoff region, $V_{gs} \leq V_t$

$$I_{ds} = 0 \tag{2}$$

In linear region, $V_{ds} < V_{gs} - V_t$

$$I_{ds,lin} = \frac{\mu W_{eff} C_{ox}}{L_{eff}} \left[(V_{gs} - V_t) V_{ds} - \frac{{V_{ds}}^2}{2} \right] (1 + LAMBDA \,.\, V_{ds}) \tag{3}$$

Where,

C_{ox} = Capacitance of the capacitor form between gate and substrate per unit area

μ = The mobility constant

W_{eff} = Effective channel width

L_{eff} = Effective channel length

V_{gs} = The gate to source voltage

V_t = The threshold voltage

V_{ds} =The drain to source voltage

$LAMBDA$ = The channel length modulation

It can be seen that the drain current is dependent upon the effective length and width of the channel. The quantity $\frac{\mu W_{eff} C_{ox}}{L_{eff}}$ is also considered to be the gain factor. This gain factor is proportional to $\frac{W_{eff}}{L_{eff}}$. The additional factor $(1 + LAMBDA\,.V_{ds})$ involves LAMBDA which models current dependence on drain voltage due to channel length modulation. A typical value for LAMBDA is much smaller than 0.1 V^{-1}.

In Saturation Region, $V_{ds} \geq V_{gs}$ - V_t

In the saturation region, V_{ds} will get saturated. i.e, $V_{ds} = V_{dsat} = V_{gs} - V_t$.

Therefore at saturation region the expression for $I_{ds,sat}$ will be as follows.

$$I_{ds,sat} = \frac{\mu W_{eff} C_{ox}}{2L_{eff}} \left(V_{gs} - V_t\right)^2 (1 + LAMBDA\,.V_{ds}) \quad (4)$$

The level 2 Model is simpler but has more equations and parameters to reflect the small geometry effects. This model was developed as the correction to the base model (level 1 model). This model describes the effect of channel length modulation, carrier velocity saturation and mobility degradation. Compared to the level 3 model, the level 2 model is less accurate and has convergence problems. Table 2 gives the list of the level 2 model parameters [10].

Table 2: SPICE level 2 model parameter

Parameter	Units	Description
Process Parameter		
TPG	m	Type of gate material
TOX	m	Gate oxide thickness
LD	m	Channel length reduction from drawn value
WD	m	Channel width reduction from drawn value
Electrical Parameter		
VTO	V	Threshold voltage, long, wide device, zero substrate bias
UO	$cm^2/V.s$	Zero bias low field mobility
UCRIT	V	Critical, vertical field for mobility reduction
UEXP		Exponent in the mobility model
RS	ohm	Source series resistance
RD	ohm	Drain series resistance
DELTA		Narrow channel effect on the threshold voltage
NSUB	cm^2	Substrate Sensitivity parameter (Effective substrate doping)
XJ	m	Short channel correction to the substrate sensitivity
VMAX		Maximum carrier velocity
NEFF		Fraction depletion charge Reduction due to channel length modulation
NFS	cm^{-2}	Sub threshold region fitting parameter
CGSO	F/m	Zero bias gate-source capacitance
CGDO	F/m	Zero bias gate-drain capacitance
CGBO	F/m	Zero bias gate-bulk capacitance
XQC		Charge partitioning parameter
Additional Mobility Parameter		
UTRA	V^{-1}	Charge partitioning parameter

The expressions for level 2 drain current is given by

$$I_{ds} = \frac{\mu W_{eff} C_{ox}}{L_{eff}} \left\{ \left(V_{gs} - \left(V_{fb} + 2\emptyset_f \right) \right) V_{ds} - \frac{{V_{ds}}^2}{2} - \frac{2}{3} f_s . \gamma . \left[\left(V_{ds} + 2\emptyset_f - V_{bs} \right)^{\frac{3}{2}} - \left(2\emptyset_f - V_{bs} \right)^{\frac{3}{2}} \right] - f_n . \left[\frac{{V_{ds}}^2}{2} + \left(2\emptyset_f - V_{bs} \right) \right] \right\} \quad (5)$$

Where,

$\emptyset_f$ = Fermi potential

V_{fb} = The flat band voltage.

V_{bs} = The bulk to source voltage.

γ = The constant = $\frac{(2\, s_i \epsilon\, N_A q)^{\frac{1}{2}}}{C_{ox}}$

f_s = The constant = $\frac{DELTA \in_s}{4\, C_{ox} W_{eff}}$

f_n = fractional reduction term

The level 3 model was developed to correct flaws such as short channel effect seen in level 1 and level 2 models. It runs faster than level 2 and convergence problems rarely occur. The problem with the level 3 model is that it fails to model the sub-threshold current and the output conductance. Table 3 gives list of the level 3 model parameters [10].

Table 3: SPICE level 3 model parameter

Parameter	Units	Description
Process Parameter		
TPG	m	Type of gate material
TOX	m	Gate oxide thickness
LD	M	Channel length reduction from drawn value
WD	m	Channel width reduction from drawn value
Electrical Parameter		
UO	$cm^2/V.s$	Zero bias low field mobility
VTO	V	Threshold voltage, long, wide device, zero substrate bias
THETA	V^{-1}	Gate field induced mobility reduction parameter
RS	Ohm	Source series resistance
RD	ohm	Drain series resistance
DELTA		Narrow channel effect on the threshold voltage
NSUB	cm^{-3}	Substrate sensitivity parameter (Effective substrate doping)
XJ	m	Short channel correction to the substrate sensitivity
ETA		DIBL coefficient
KAPPA	V^{-1}	Channel length modulation effect on the drain current
NFS	cm^{-2}	Subthreshold region fitting parameter
CGSO	F/m	Zero bias gate-source capacitance
CGDO	F/m	Zero bias gate-drain capacitance
CGBO	F/m	Zero bias gate-bulk capacitance
XQC		Charge partitioning parameter
Additional Mobility Parameter		
BEX	V^{-1}	Temperature effect on the low field mobility

The expressions for level 3 drain current is given by

$$I_{ds} = \frac{\mu_{eff} W_{eff} C_{ox}}{L_{eff}} \left\{ \left[V_{gs} - \left(V_{fb} + 2\emptyset_f \right) - f_s . \gamma . \left(2\emptyset_f - V_{bs} \right)^{\frac{1}{2}} - f_n . \left(2\emptyset_f - V_{bs} \right) \right] V_{ds} - \frac{{V_{ds}}^2}{2} \left[1 + \frac{f_s . \gamma}{2\left(2\emptyset_f - V_{bs} \right)^{\frac{1}{2}}} + f_n \right] \right\} \quad (6)$$

A commercial power MOSFET, DirectFET®, manufactured by International Rectifier Corporation is used in the simulation for the MOSFET driver design. The manufacture part number of the DirectFET® is IRF6668. The properties of IRF6668 according to its data sheet are as follows,

- Low profile, the device is less than 0.7mm with ultra low inductance
- Allows dual sided cooling to maximize thermal transfer in power systems
- Optimized for high frequency switching
- Ideal for high performance isolated converter primary switch socket
- Optimized for synchronous rectification
- Low conduction losses
- Compatible with existing surface mounted technique.

Every component has its own unique syntax to define its model. In the syntax of the SPICE model, there are numerous parameters that define the component characteristic. The syntax for the SPICE Model of MOSFET is represented by the following general form [11].

General Form of MOSFET:

M<name> <drain node> <gate node> <source node>
+ < bulk/substrade node> <model name>
+[L=<value>][W=<value>] [AD=<value>]
+ [AS=<value>] [PD=<value>][PS=<value>]
+ [NRD=<value>][NRS=<value>] [NRG=<value>]
+ [NRB=<value>] [M=<value>]

Examples:

M1 14 2 13 0 PNOM L=25u W=12u
M13 15 3 0 0 PSTRONG
M16 17 3 0 0 PSTRONG M=2
M28 0 2 100 100 NWEAK L=33u W=12u
+ AD=288p AS=288p PD=60u PS=60u NRD=14 NRS=24 NRG=10
Model Form
.MODEL <model name> NMOS [model parameter]
.MODEL <model name> PMOS [model parameter]

In the above syntax and general form, L and W represent the channel length and width respectively. These parameters can be specified in the model with the appropriate values. The default value for L and W are 100 μm. AD and AS are the drain and source diffusion areas where as PD and PS are the drain and source diffusion perimeters. The default value for PD and PS is 0. RHS stands for drain and source diffusion sheet resistance. It has a unit of ohms per square meter. The quantities NRD, NRS, NRG and NRB are multipliers that can be multiplied by RSH to yield the parasitic ohmic resistance RD, RS, RG and RB respectively. The default value for NRD and NRS is 1 and the default value for NRG and NRB is 0. M value represents the multiplier which simulates the effect of multiple devices in parallel. The default value for M is 1. The SPICE models for the MOSFETs used for the simulation are as follows:

Level 1 MOSFET SPICE model

```
.MODEL MM NMOS LEVEL=1 IS=1e-0
+VTO=5.6528 LAMBDA=0.0156185 KP=68.8096
+CGSO=1.22309e-05 CGDO=4.675e-07
```

Level 3 MOSFET SPICE model

```
.model IRF034  NMOS (Level=3 Gamma=0 Delta=0 Eta=0 Theta=0 Kappa=0.2 Vmax=0 Xj=0
+                   Tox=100n Uo=600 Phi=.6 Rs=31.69m Kp=21.5u W=1.3 L=2u Vto=3.441
+                   Rd=1.139m Rds=266.7K Cbd=2.857n Pb=.8 Mj=.5 Fc=.5 Cgso=579p
+                   Cgdo=456.3p Rg=8.548 Is=184.5f N=1 Tt=365n)
*                   Int'l Rectifier     pid=IRFC034    case=TO3
*                   88-08-25 bam    creation
```

The SPICE model for a commercial MOSFET was developed by the manufacturer and the SPICE parameters were derived from the actual experiments. Since the SPICE parameters vary with temperature, most commercial MOSFET SPICE models include a thermal model to compensate for the temperature effects. Thus, the commercial SPICE model is more complex than the level 3 model. A commercial SPICE model for the IRF6668 is shown in Appendix 1.

Chapter 3 Power Resonant MOSFET Driver Design and Simulations

3.1 Basic Driver Design

The design starts with the simulation of a simple circuit for a resonant MOSFET driver. The output of the MOSFET H-bridge is simulated by keeping two pulse generators in series as shown in Figure 5. Series capacitance and inductance are added in order to have a resonant condition at 20 kHz. With the help of the basic circuit of the resonant MOSFET driver in Figure 5, basic operation of the resonant MOSFET driver can be examined.

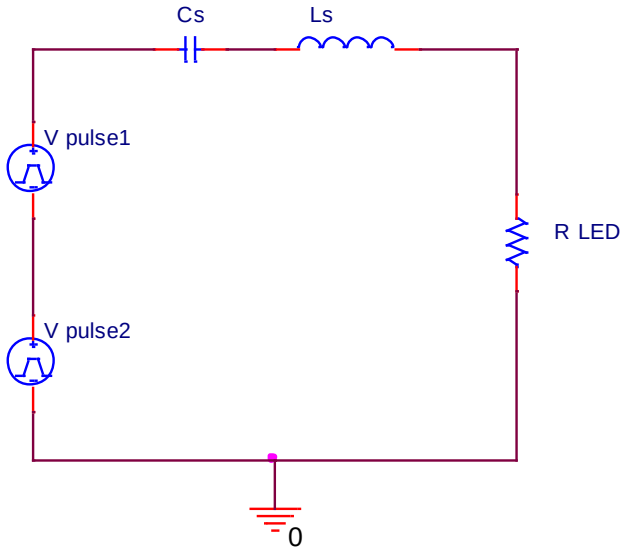

Figure 5. Basic circuit explaining resonant MOSFET driver

Pulse generators V pulse1 and V2 generate positive and negative pulses with a fixed pulse width PW and period PER. The PW and PER are given by the following expression:

$$PW = \frac{0.9 * 0.5}{FRQ} \tag{7}$$

$$PER = \frac{1}{FRQ} \tag{8}$$

Where,

FRQ = Frequency of the pulse generated by pulse generator

PW is inversely proportional to the switching frequency FRQ. Hence, the driver circuit can be controlled by varying the switching frequency. Frequency is varied in steps of 1 kHz and the values are measured for power output and current. Then the corresponding power factor is calculated from the measured values. Table 4 was obtained from the simulation result of the circuit shown in Figure 6. Various graphs were traced on the basis of Table 4.

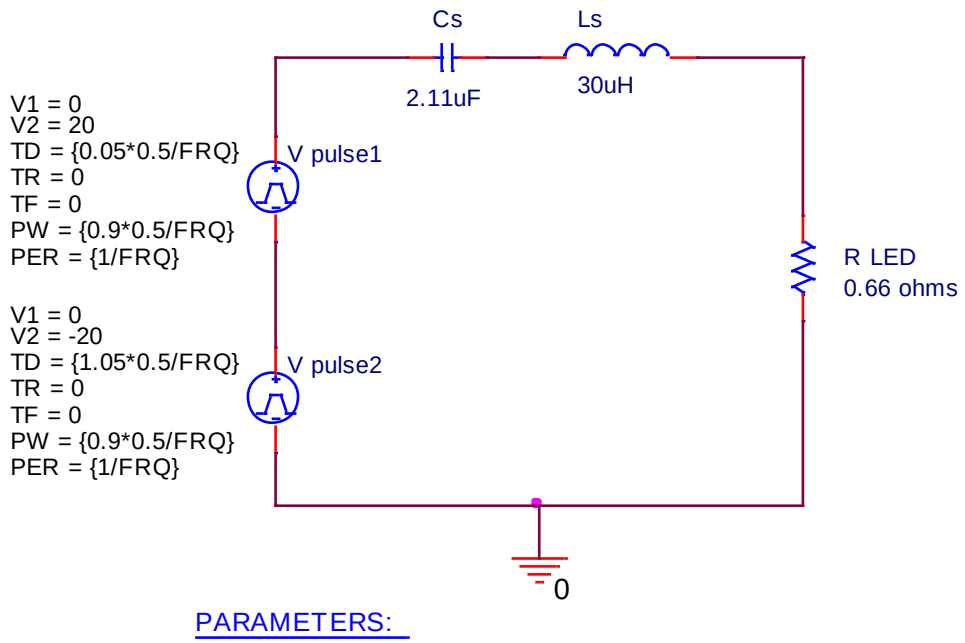

Figure 6. Simulation circuit for basic resonant MOSFET driver

Table 4: Simulation results for the basic resonant MOSFET driver

	Measured From Simulation				Calculated	
Frequency (KHz)	del T (u sec)	Current I peak (Amps)	Phase Difference	Power (Watt)	Difference Phase phi (degree)	Power Factor cos phi
20	0.00	33.81	0.00	754	0.00	1.00
21	3.39	30.47	0.07	613	25.63	0.90
22	6.56	24.25	0.14	388	51.95	0.62
23	6.46	19.54	0.15	235	53.45	0.60
24	6.18	16.33	0.15	176	53.39	0.60
25	7.16	14.10	0.18	131	64.42	0.43
26	7.22	12.50	0.19	103	67.60	0.38
27	7.25	11.29	0.20	84	70.45	0.34
28	7.14	10.30	0.20	70	72.02	0.31
29	7.07	9.48	0.21	59	73.82	0.28
30	6.90	8.79	0.21	51	74.51	0.27
31	6.80	8.20	0.21	44	75.94	0.24
32	6.65	7.69	0.21	39	76.57	0.23
33	6.47	7.25	0.21	35	76.90	0.23
34	6.38	6.86	0.22	31	78.12	0.21
35	6.20	6.52	0.22	28	78.17	0.21
34	6.38	6.86	0.22	31	78.12	0.21
35	6.20	6.52	0.22	28	78.17	0.21

In Figure 7, green, red and blue waveforms show the voltage waveform at 20 kHz, 22.5kHz, and 25 kHz respectively. This shows how the pulse width (PW) along with period (PER) can be varied by varying the FRQ. In this figure, the pulse width at 20 kHz, 22.5 kHz and 25 kHz are measured to be 22.5 µs, 20 µs and 18 µs respectively and period as 45 µs, 20 µs and 36 µs respectively. It can be noted that as frequency increases, the pulse width along with period decreases. This proves that the PW and PER are inversely proportional to FRQ.

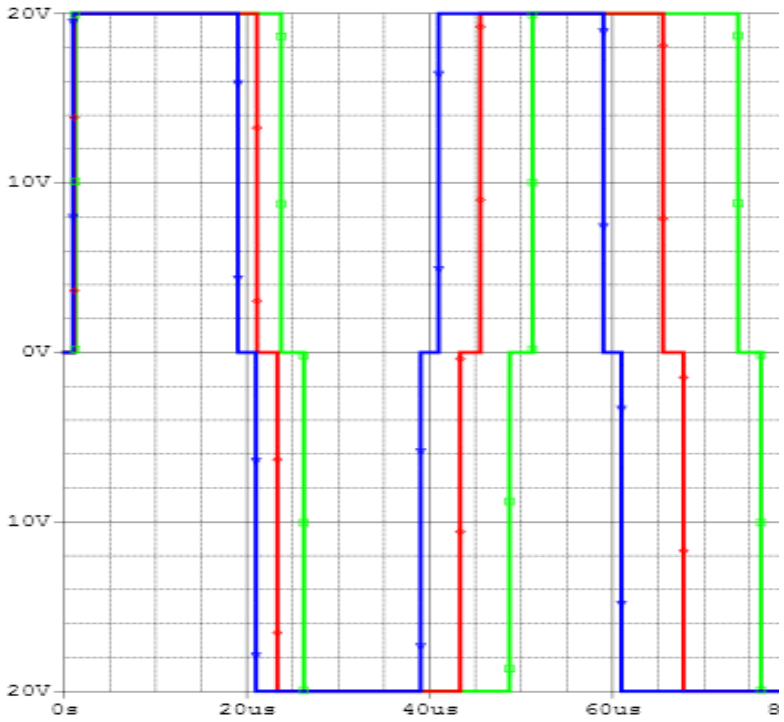

Figure 7. Voltage waveforms at 20 kHz (green), 22.5 kHz (red) and 25 kHz (blue)

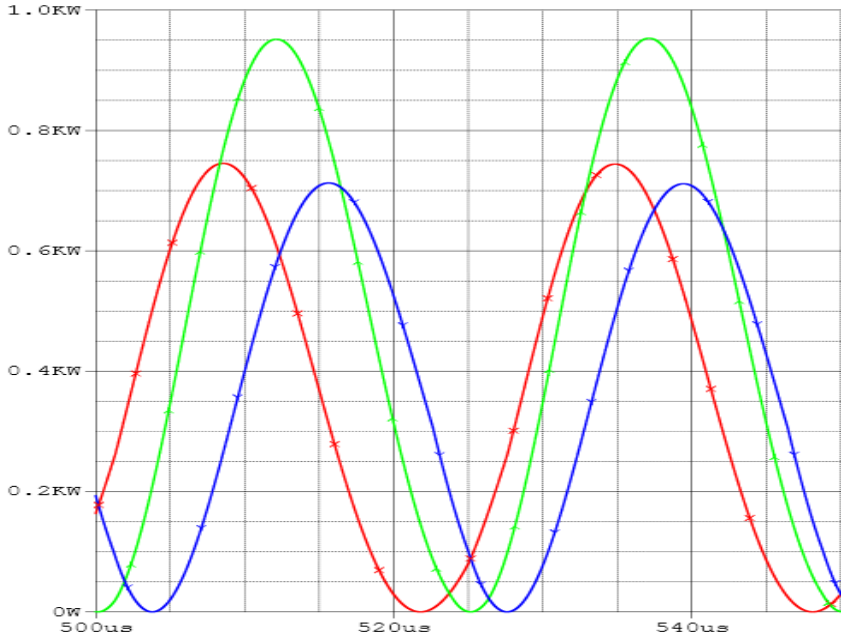

Figure 8. Power waveforms at 19 kHz (blue), 20 kHz (green) and 21 kHz (red)

Figure 8 shows that the power is at the maximum at resonant condition. At resonant condition, the switching frequency is 20 kHz. At 19 kHz and 21 kHz the power is lower compared to the power at resonant frequency. In Figure 8, green waveforms represent the power at resonant frequency. Red and Blue waveforms represent the power at 19 kHz and 21 kHz respectively. Thus, the output power can be adjusted from 754 W to 28 W by changing the switching frequency from 20 kHz to 35 kHz.

Figure 9 demonstrates that current and voltage are in phase with each other at resonant condition. At 19 kHz and 21 kHz, there are some phase diffferences which are demonstrated in Figures 10 and 11 respectively. In Figure 10, the voltage leads current, which indicats that the load circuit is inductive.

In Figure 11, the current leads voltage indicating that the circuit is capacitive. At 19 kHz, X_L is 3.5814 ohms and X_C is 3.9715 ohms and at 21 kHz, X_L is 3.9584 ohms and X_C is 3.5932 ohms.

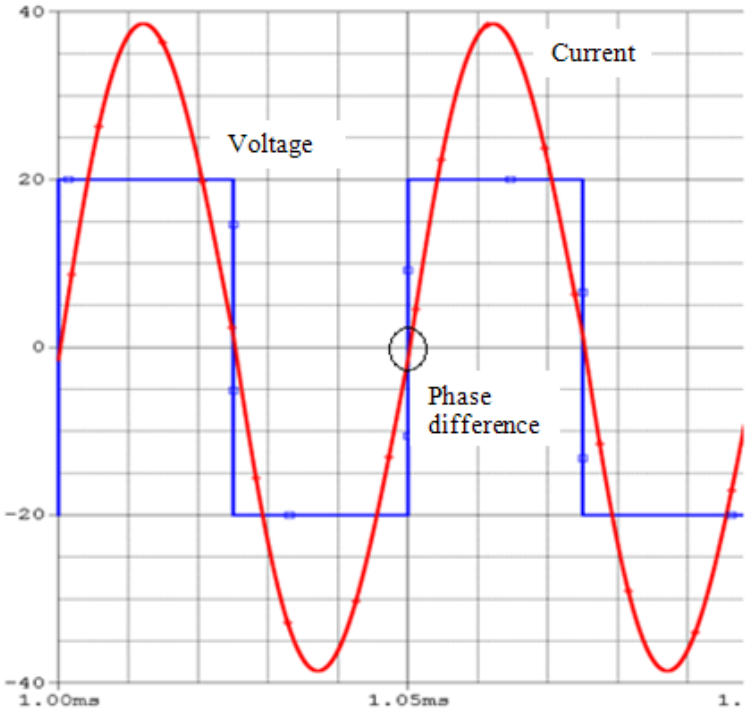

Figure 9. Voltage (blue) and current (red) in phase with each other at 20 kHz

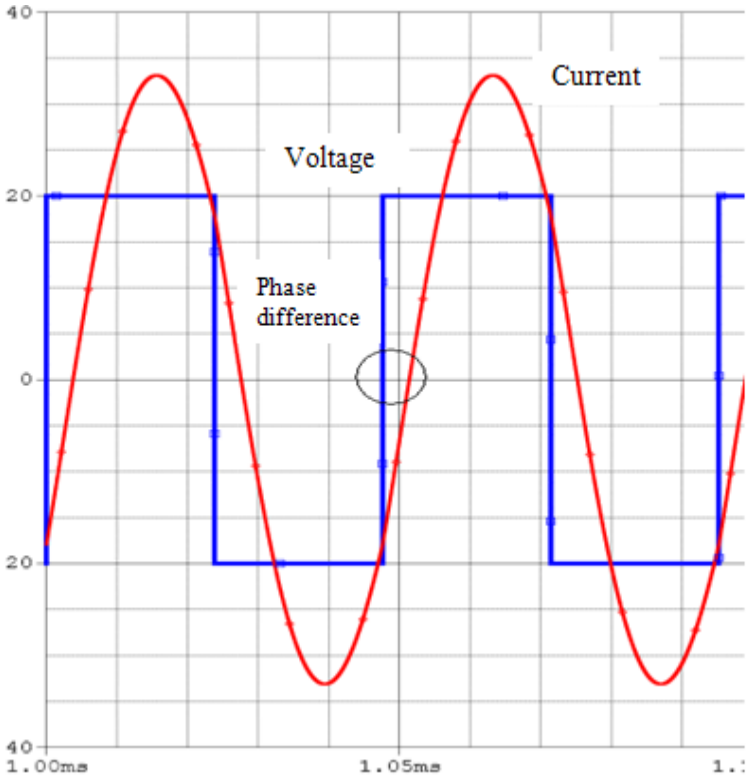

Figure 10. Voltage (blue) leading current (red) at 21 kHz

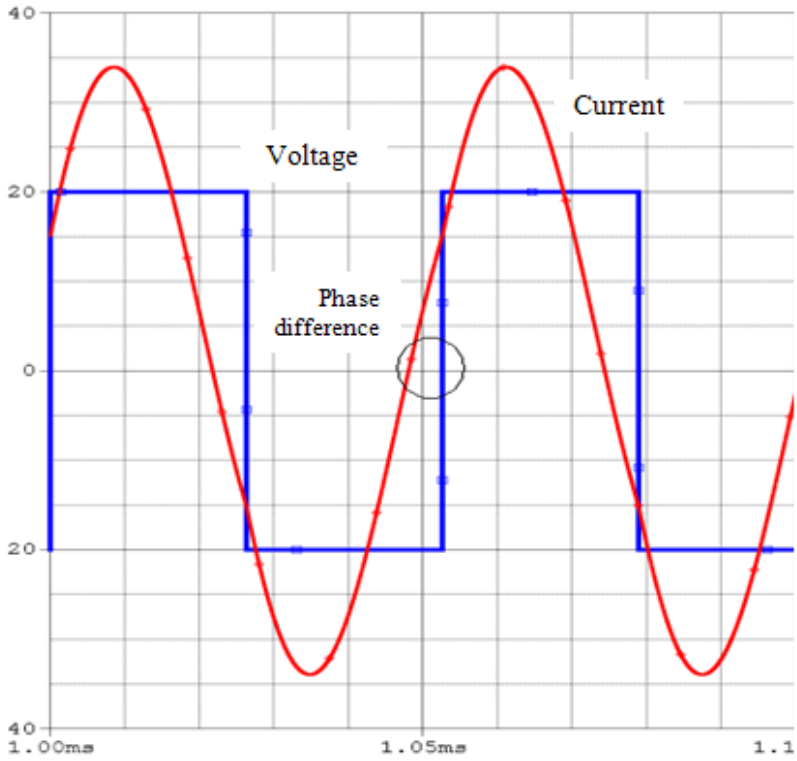

Figure 11. Voltage (blue) lagging current (red) at 19 kHz

From Table 4, three graphs were obtained. Figures 12, 13 and 14 show the graph of frequency vs. power, frequency vs. power factor and frequency vs. current respectively. Figure 12, 13 and 14 show that from 20 kHz to 35 kHz, the power, power factor and current range from 754 W to 28 W, 1 to 0.2 and 33.8 A to 6.5 A respectively. Therefore, the frequency range from 20 kHz to 35 kHz was chosen for our design.

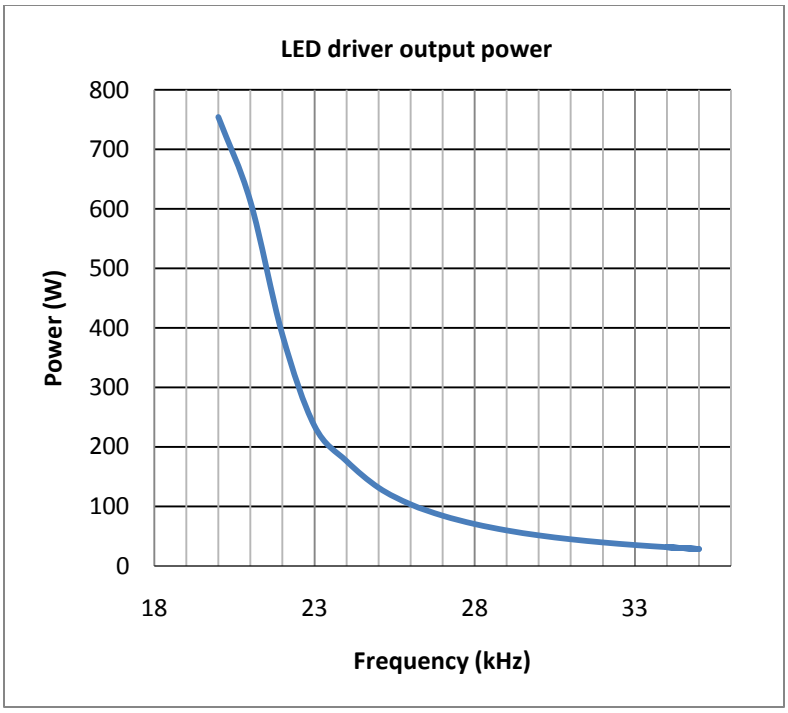

Figure 12. LED driver output power for basic resonant MOSFET driver

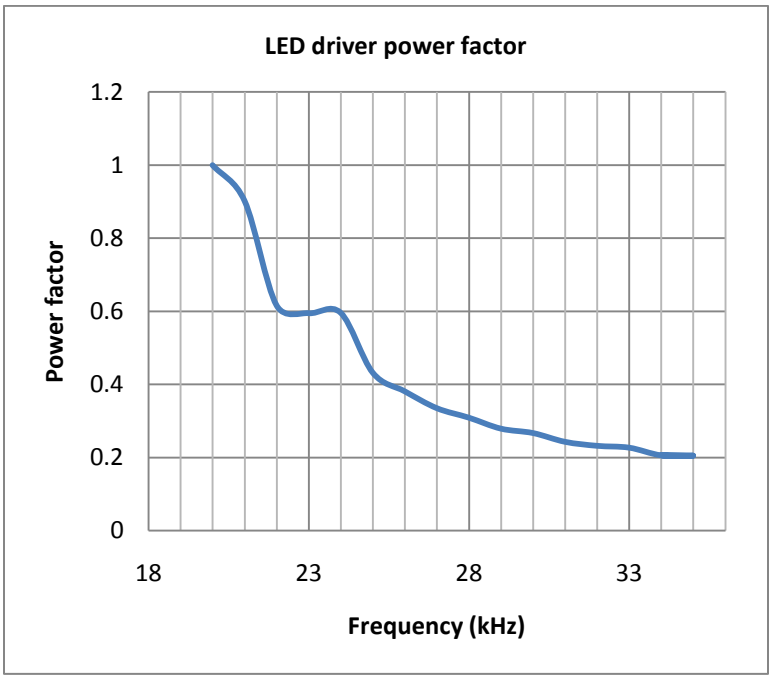

Figure 13. LED driver power factor for basic resonant MOSFET driver

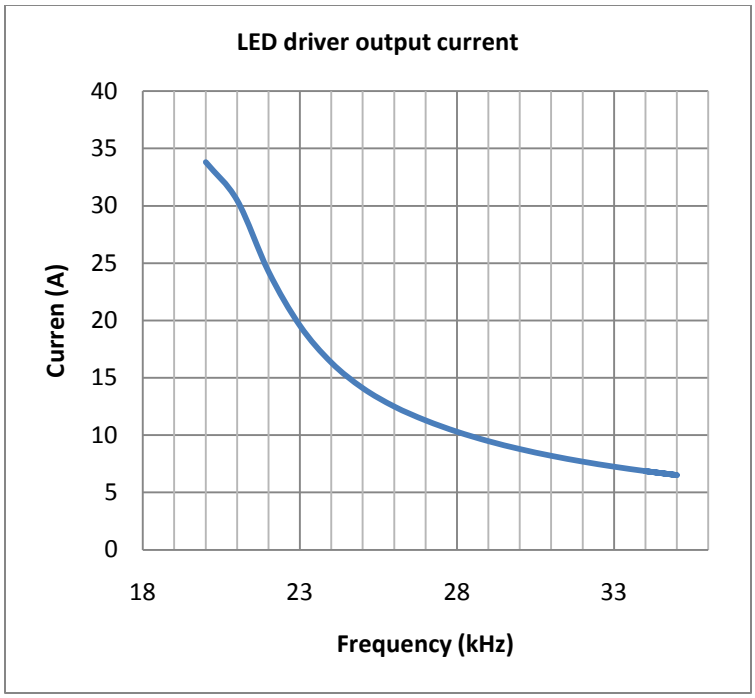

Figure 14. LED driver output current for basic resonant MOSFET driver

3.2 Resonant Power MOSFET Driver Design

The resonant power MOSFET driver circuit is designed as shown in Figure 15.

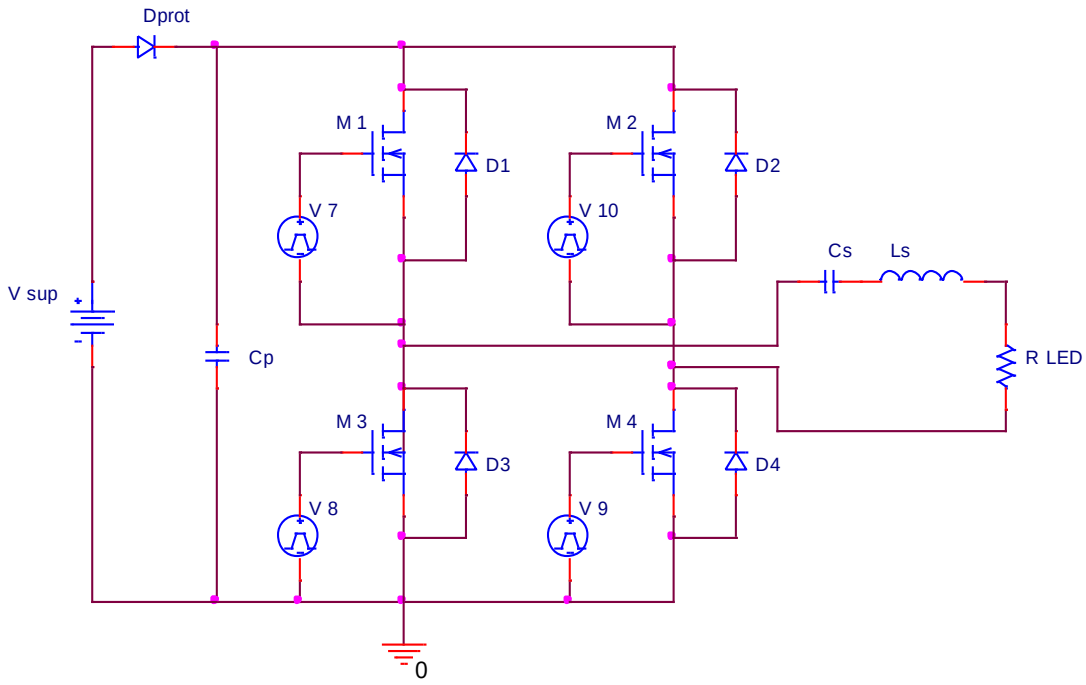

Figure 15. Resonant power MOSFET driver circuit

Voltage pulse generators V7 and V9 generate identical voltage pulses. They have minimum voltage V1 = 0 V, maximum voltage V2 = 20 V, time delay TD = 0.1*(0.5/FRQ), rise time TR = 1 µs, fall time TF = 1 µs, pulse width PW =0.8*(0.5/FRQ) and period PER = 1/FRQ. Likewise, voltage pulse generators V8 and V10 generate identical voltage pulses. The only difference is the time delay, which is set in such a way that the two sets of pulse generators will generate the pulses alternately. The pulses generated by each set of pulse generators are shown in Figure 16. Blue pulses are generated by V7 and V9, whereas red pulses are generated by V8 and V10.

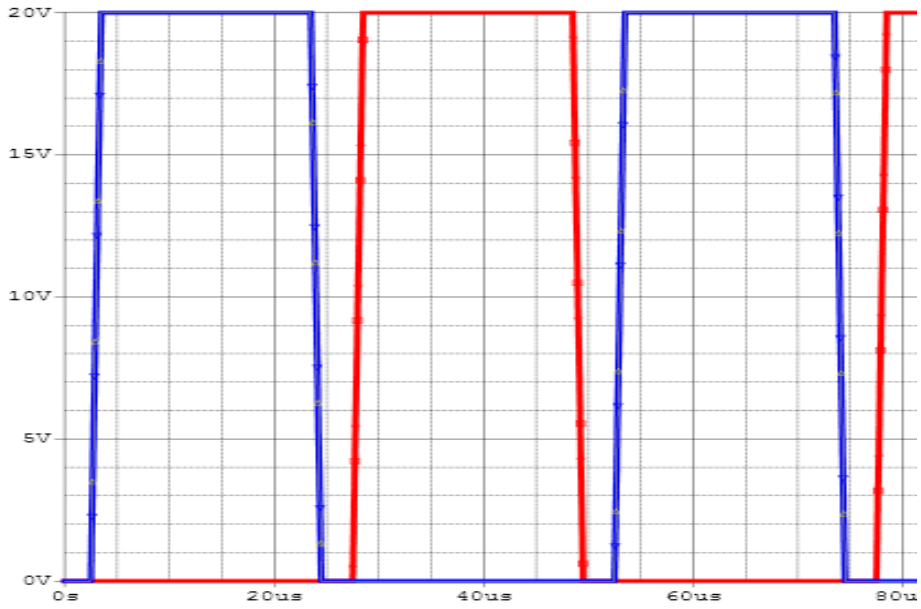

Figure 16. Pulse generated by pulse generators.

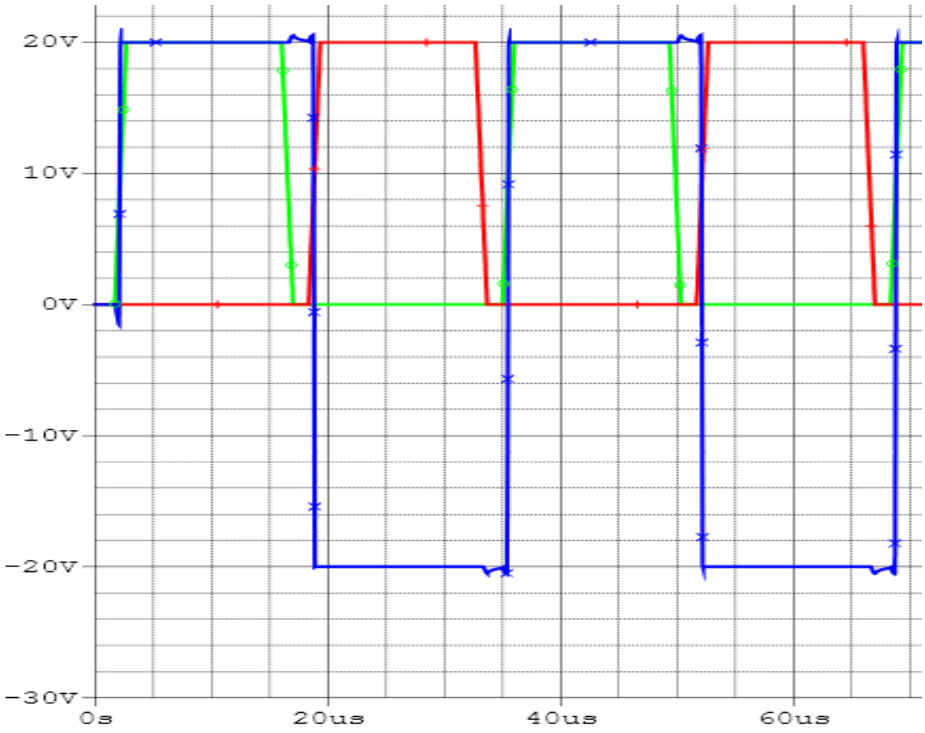

Figure 17. Output voltages (blue) of MOSFET H-bridge

At 20 kHz, the pulse width is 16 µs. Rise time (TR) and fall time (TF) are 1µs. The delay time (TD) for V7 and V9 are 2 µs. V8 and V10 voltage generators have nonzero values after 27.5 µs and require 1 µs to attain the maximum value of 20 V.

In the above topology, a fixed voltage V sup = 20 V is supplied as shown in Figure 15. MOSFETs are turned ON and OFF by means of pulse generators. MOSFET pairs M1, M4 and M2, M3 are turned ON and OFF alternately. As a result, this generates positive and negative pulses of 20 V equal to the supplied voltage as shown in Figure 17. Thus, the pulse width of MOSFET H-bridge output is equal to the pulse width of the pulse generator. This implies that the bridge output can be controlled by controlling the frequency of the pulse generators.

In Figure 15, D1, D2, D3 and D4 are connected in parallel to MOSFETs M1, M2, M3, and M4 respectively. These diodes are called flywheeling diodes. Figure 18 shows the flywheel connected in parallel to the MOSFET. Flywheel diodes also are used to prevent the switching circuit by suppressing the voltage spikes caused when the MOSFETs are turned off. Flywheel diodes also are used to protect power MOSFETs from damage by reverse battery protection as well as protection from highly inductive loads. When the frequency of the circuit becomes higher than the resonant frequency, the circuit becomes inductive. In such cases, the significant role of flywheel diodes D1, D2, D3 and D4 can be achieved. Diode D prot is used to eliminate the reverse current.

A capacitor Cp parallel to the H-bridge works as a snubber. It protects the MOSFETs by limiting the voltage during turn-off transients and currents during the turn-on transient. This snubber circuit reduces dV/dt and dI/dt by transferring the switching energy from the power MOSFET to an energy storage element.

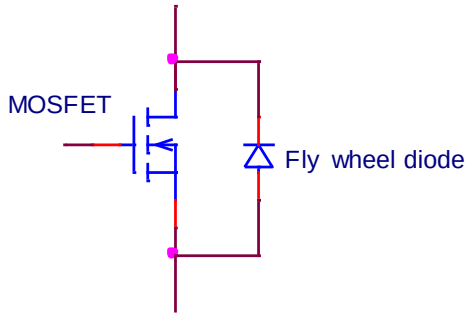

Figure 18. MOSFET protection using flywheel diode

Chapter 4 Computer Simulations and Results

The power resonant LED MOSFET driver is designed and simulated with different MOSFET SPICE models. The MOSFET is modeled with MOSFET SPICE level 1, level 3, and commercial MOSFET SPICE models. The circuit in Figure 19 was built for the simulations. In appendix 2, Figures 27, 28, and 29 shows the enlarged circuit of LED MOSFET drivers which has MOSFETs modeled with MOSFET SPICE level 1, level 3, and commercial MOSFET SPICE models respectively.

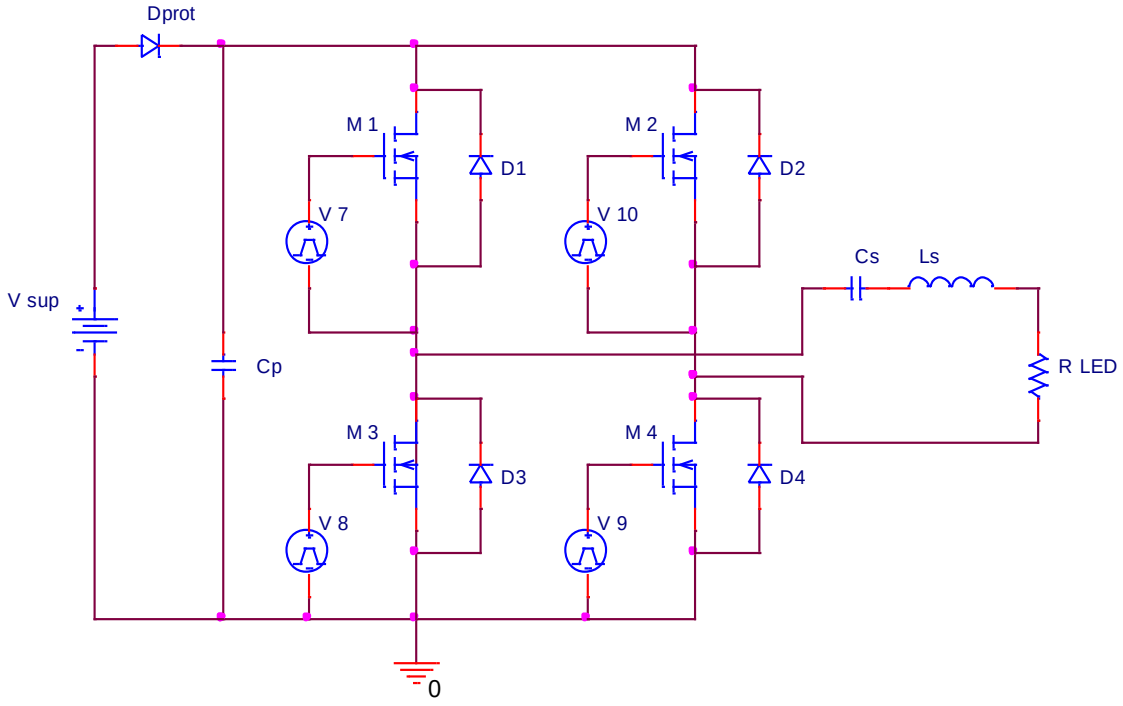

Figure 19. Resonant power MOSFET driver circuit

4.1 Simulation with MOSFET SPICE Model level 1

For simulation with MOS level 1, H-bridge was generated using a SPICE level 1 MOSFET as shown in Figure 19. By changing the switching frequency of the MOSFET, the various simulation results were taken and tabulated in Table 5. The efficiency of the

MOSFET driver was found to be 77% at 20 kHz. At 30 kHz the driver efficiency decreased to 31%. From the MOSFET SPICE level 1 simulation results, Figure 20 shows that the operating frequency increased while the driver efficiency gradually decreased. Figure 21 shows that the efficiency increased as output power increased.

Table 5: Simulation results for the driver using MOSFET SPICE level 1

Frequency (kHz)	Input Current (A)	Input Voltage (V)	Input Power (W)	Output Current (A)	Output Voltage (V)	Output Power (W)	Efficiency
18.0	11.10	20	222	15.90	10.45	166	74
19.0	17.91	20	358	20.49	13.53	277	77
20.0	20.80	20	416	22.00	14.60	321	77
21.0	18.37	20	367	20.57	13.61	280	76
22.0	12.20	20	244	10.92	16.61	181	74
23.0	8.42	20	168	8.77	13.28	117	69
24.0	6.32	20	126	7.24	10.97	79	62
25.0	5.08	20	102	6.13	9.27	57	56
30.0	3.01	20	60	3.53	5.25	19	31

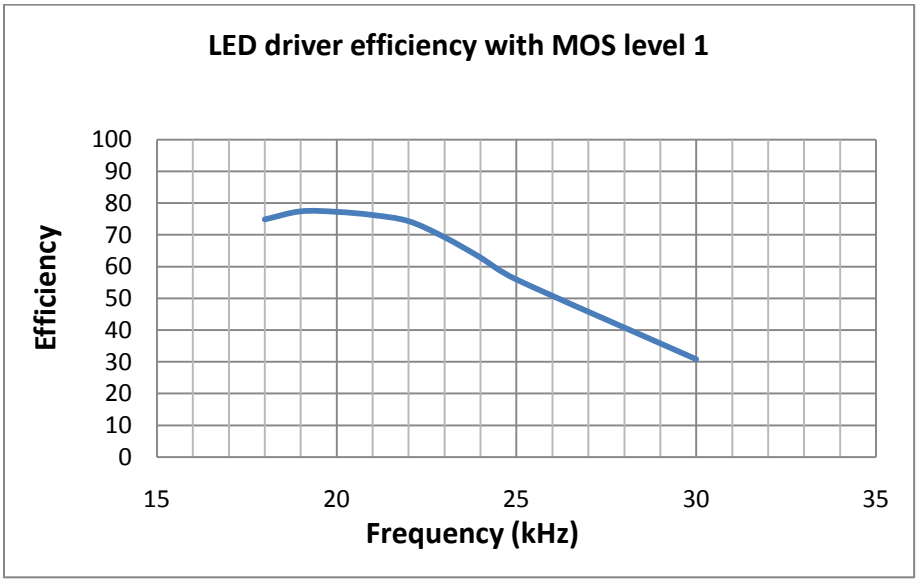

Figure 20. LED driver efficiency for MOSFET SPICE level 1

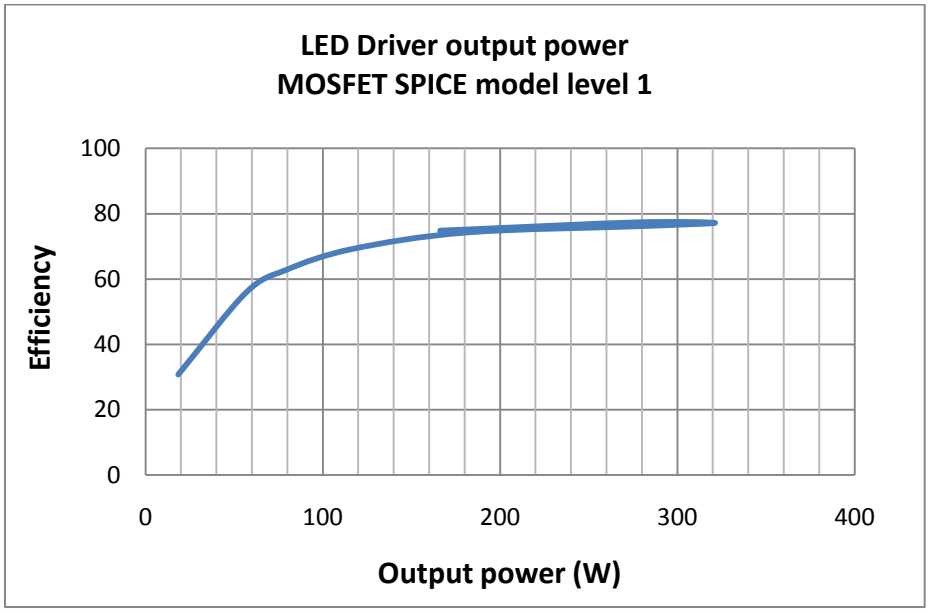

Figure 21. LED driver output power for MOSFET SPICE level 1

4.2 Simulation with MOSFET SPICE Model level 3

For simulation with MOS level 3, H-Bridge was generated using a SPICE level 3 MOSFET. Figure 19 shows the driver circuit using a level 3 MOSFET. Various measurements are tabulated in Table 6 by changing the switching frequency of the MOSFETs.

In the case of the simulation results with MOSFET SPICE level 3, at 20 kHz, the efficiency was found to be 77 %. As frequency increased the efficiency gradually increased, but at a very low rate. The efficiency of the circuit went up to 82 % at 25 kHz, keeping overall average efficiency around 80 %. The output power had a maximum value of 351 W at 20 kHz which went down up to 10 W at 35 kHz. Figure 22 shows the graph of efficiency vs. frequency and Figure 23 shows efficiency vs. output power.

Table 6: Simulation results for the driver using MOSFET SPICE level 3

Frequency (kHz)	Input Current (A)	Input Voltage (V)	Input Power (W)	Output Current (A)	Output Voltage (V)	Output Power (W)	Efficiency
18.0	9.76	20	195	15.30	10.10	154	79
19.0	15.67	20	313	19.23	12.70	244	77
20.0	17.55	20	351	20.32	13.32	270	77
21.0	15.82	20	316	19.39	12.80	248	78
22.0	10.50	20	210	15.97	10.54	168	80
23.0	6.88	20	138	13.04	8.60	112	81
24.0	4.76	20	95	10.86	7.17	77	82
25.0	3.46	20	69	9.28	6.12	56	82
30.0	1.20	20	24	5.41	3.57	19	80
35.0	0.64	20	13	3.89	2.57	10	78

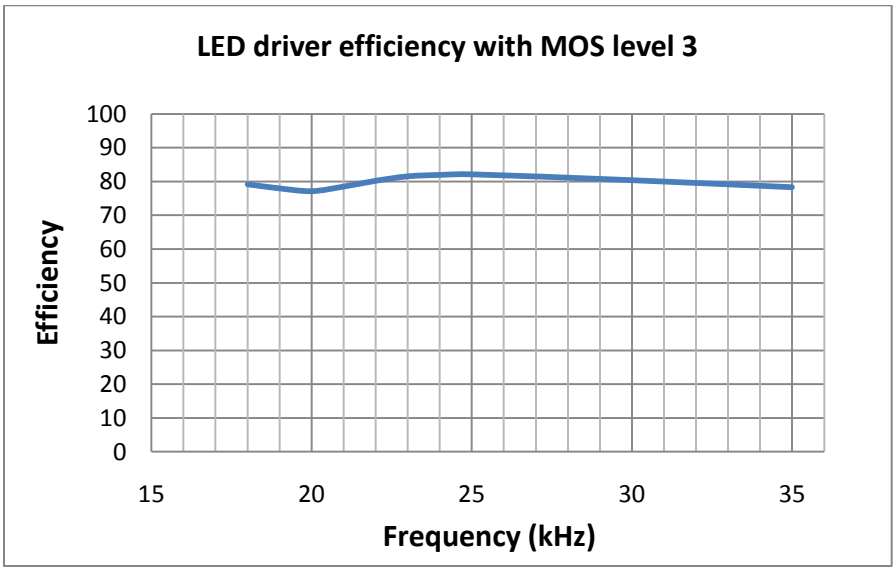

Figure 22. LED driver efficiency for MOSFET level 3

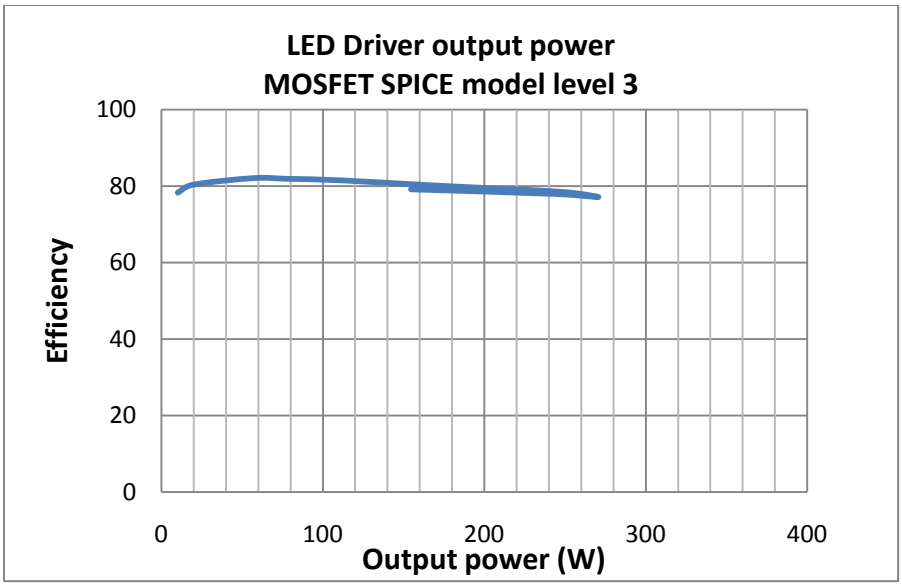

Figure 23. LED driver output power for MOSFET SPICE level 3

4.3 Simulations with Commercial MOSFET SPICE Model

For a simulation with MOS level 3, H-Bridge was built using the commercially available power MOSFET (IRF6668). Figure 19 shows the driver circuit using IRF6668. By changing the switching frequency of the MOSFET, the various simulation results are tabulated in Table 7.

Figure 24 shows the graph of efficiency vs. frequency and Figure 25 shows efficiency vs. output power. At 20 kHz, the efficiency of the circuit was 87 %. As the operating frequency increased, the efficiency of the circuit gradually increased. The output power was 323 W at 20 kHz and dropped to 50 W at 25 kHz. The efficiency verses output power plots for MOSFET drivers of various MOSFET levels and conventional resistive driver are shown in Figure 26.

Table 7: Simulation results for the driver using commercial MOSFET model.

Frequency (kHz)	Input Current (A)	Input Voltage (V)	Input Power (W)	Output Current (A)	Output Voltage (V)	Output Power (W)	Efficiency
17.0	6.87	20	138	14.07	9.29	130	95
18.0	12.63	20	253	18.56	12.25	227	90
19.0	18.11	20	362	22.00	14.52	319	88
20.0	18.66	20	373	22.13	14.61	323	87
21.0	13.03	20	261	18.61	12.31	229	88
25.0	2.76	20	55	8.78	5.80	51	92

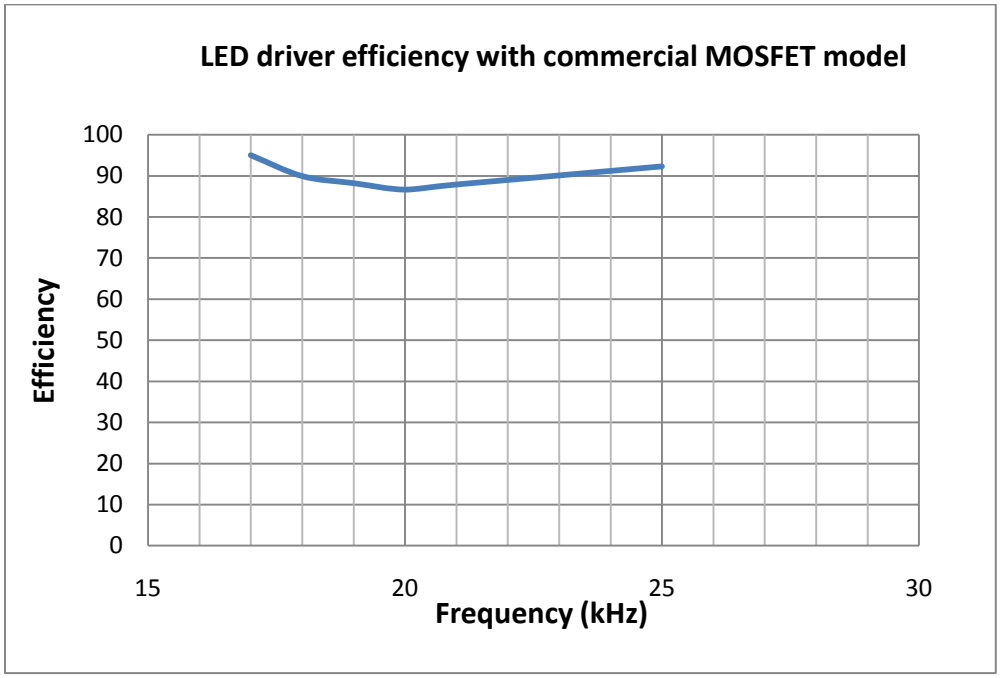

Figure 24. LED driver efficiency for commercial MOSFET model

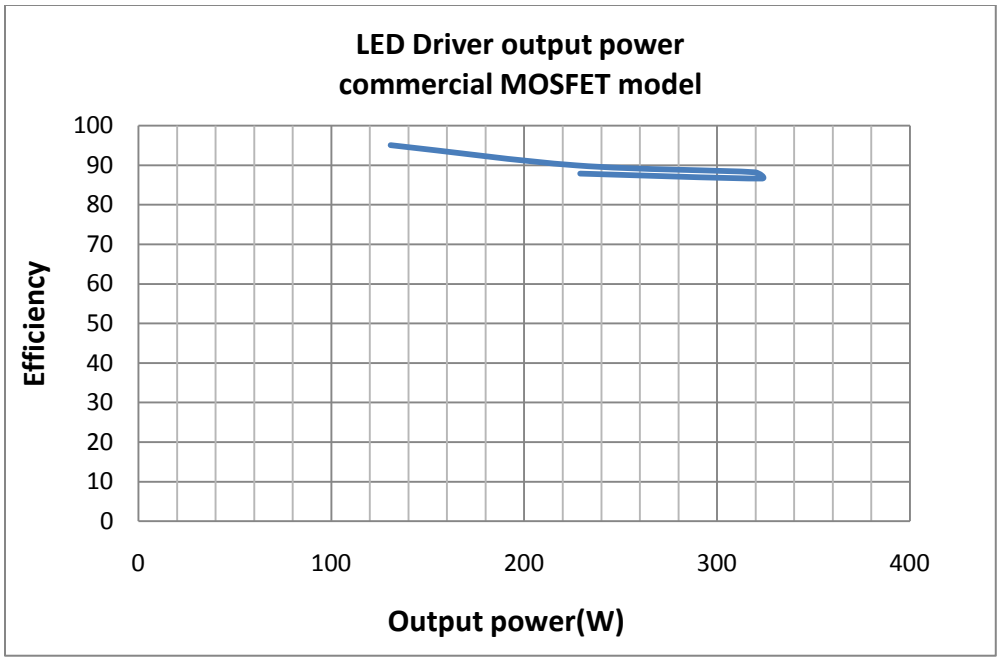

Figure 25. LED driver output power for commercial MOSFET model

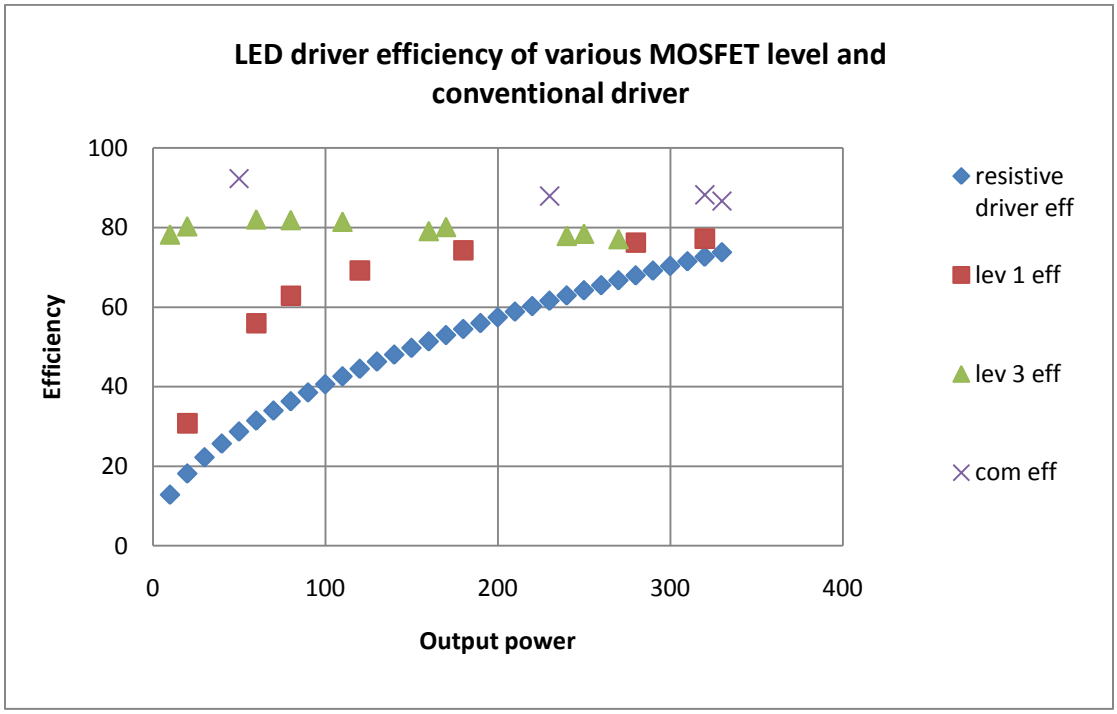

Figure 26. Comparison of efficiencies at various output power

Chapter 5 Conclusions and future work

5.1 Conclusions

The resonant power MOSFET driver was modeled and simulated. The MOSFET LED driver was designed in such a way that the output power could be controlled by the switching frequency of the MOSFET. The driver was built and tested using simulation software with various MOSFETs SPICE models, such as, MOS level 1, MOS level 3 and a commercial MOSFET.

The resonant MOSFET driver had higher efficiency compared to that of the conventional resistive driver. Among the different drivers using different MOSFET SPICE models, the driver with commercial MOSFET had the highest efficiency of an average 90% and that with level 3 and level 1 have 80% and 66% respectively. As MOSFET models develop from basic-level MOS level 1 to the high-level (commercial) models available today, the efficiency of the simulation is improved.

5.2 Future work

This thesis is completely based on the computer simulations. For the future, a frequency controller for the voltage pulse generator can be designed. A prototype MOSFET LED driver can be built. The built circuit can be tested in order to discover the limitation of the designed circuits.

Appendices

Appendix 1

COMMERCIAL MOSFET SPICE MODEL (IRF6668)

```
.SUBCKT irf6668 1 2 3
* SPICE3 MODEL WITH THERMAL RC NETWORK
**************************************
*      Model Generated by MODPEX     *
*Copyright(c) Symmetry Design Systems*
*         All Rights Reserved        *
*    UNPUBLISHED LICENSED SOFTWARE   *
*   Contains Proprietary Information *
*      Which is The Property of      *
*     SYMMETRY OR ITS LICENSORS      *
*Commercial Use or Resale Restricted *
*   by Symmetry License Agreement    *
**************************************
* Model generated on Nov  8, 05
* MODEL FORMAT: SPICE3
* Symmetry POWER MOS Model (Version 1.0)
* External Node Designations
* Node 1 -> Drain
* Node 2 -> Gate
* Node 3 -> Source
M1 9 7 8 8 MM L=100u W=100u
.MODEL MM NMOS LEVEL=1 IS=1e-32
+VTO=5.6528 LAMBDA=0.0156185 KP=68.8096
+CGSO=1.22309e-05 CGDO=4.675e-07
RS 8 3 0.00788192
D1 3 1 MD
.MODEL MD D IS=1.152e-09 RS=0.00140281 N=1.31333 BV=80
+IBV=0.00025 EG=1 XTI=3.93913 TT=1e-07
+CJO=1.85841e-09 VJ=0.606242 M=0.550721 FC=0.5
RDS 3 1 1e+07
RD 9 1 0.0001
RG 2 7 1.57367
D2 4 5 MD1
* Default values used in MD1:
*   RS=0 EG=1.11 XTI=3.0 TT=0
*   BV=infinite IBV=1mA
.MODEL MD1 D IS=1e-32 N=50
+CJO=6.28678e-10 VJ=0.5 M=0.803992 FC=1e-08
D3 0 5 MD2
* Default values used in MD2:
*   EG=1.11 XTI=3.0 TT=0 CJO=0
*   BV=infinite IBV=1mA
.MODEL MD2 D IS=1e-10 N=0.407193 RS=3e-06
RL 5 10 1
FI2 7 9 VFI2 -1
VFI2 4 0 0
EV16 10 0 9 7 1
CAP 11 10 6.28678e-10
```

```
FI1 7 9 VFI1 -1
VFI1 11 6 0
RCAP 6 10 1
D4 0 6 MD3
* Default values used in MD3:
*   EG=1.11 XTI=3.0 TT=0 CJO=0
*   RS=0 BV=infinite IBV=1mA
.MODEL MD3 D IS=1e-10 N=0.407193
.ENDS irf6668

*SPICE Thermal Model Subcircuit
.SUBCKT irf6668t 3 0

R_RTHERM1         3 2  0.317299578
R_RTHERM2         2 1  0.528270042
R_RTHERM3         1 0  0.553586498
C_CTHERM1         3 0  0.000151277
C_CTHERM2         2 0  0.000636038
C_CTHERM3         1 0  0.002653605

.ENDS irf6668t
```

Appendix 2

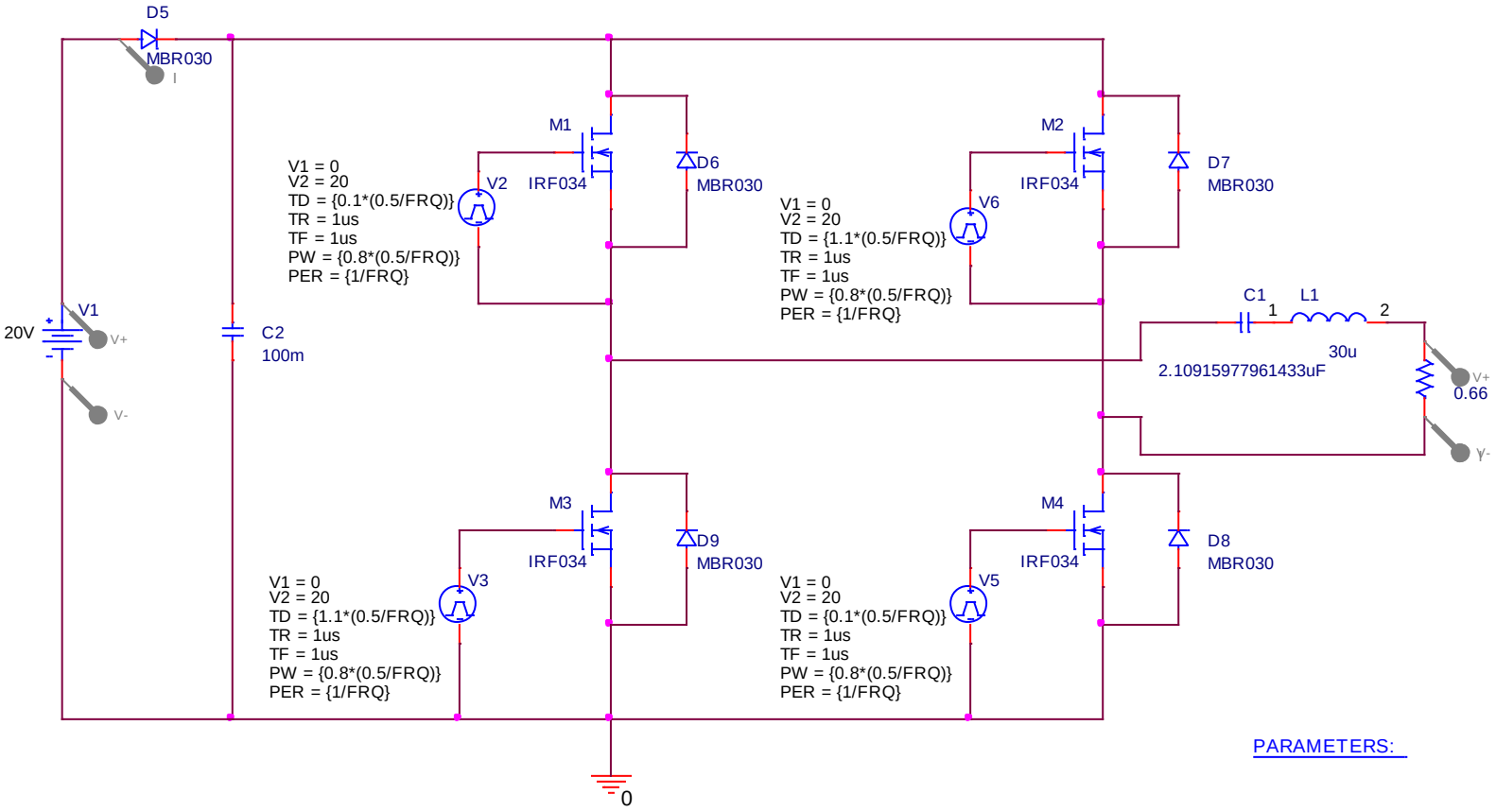

Figure 27. Resonant MOSFET driver using MOSFET SPICE level 1

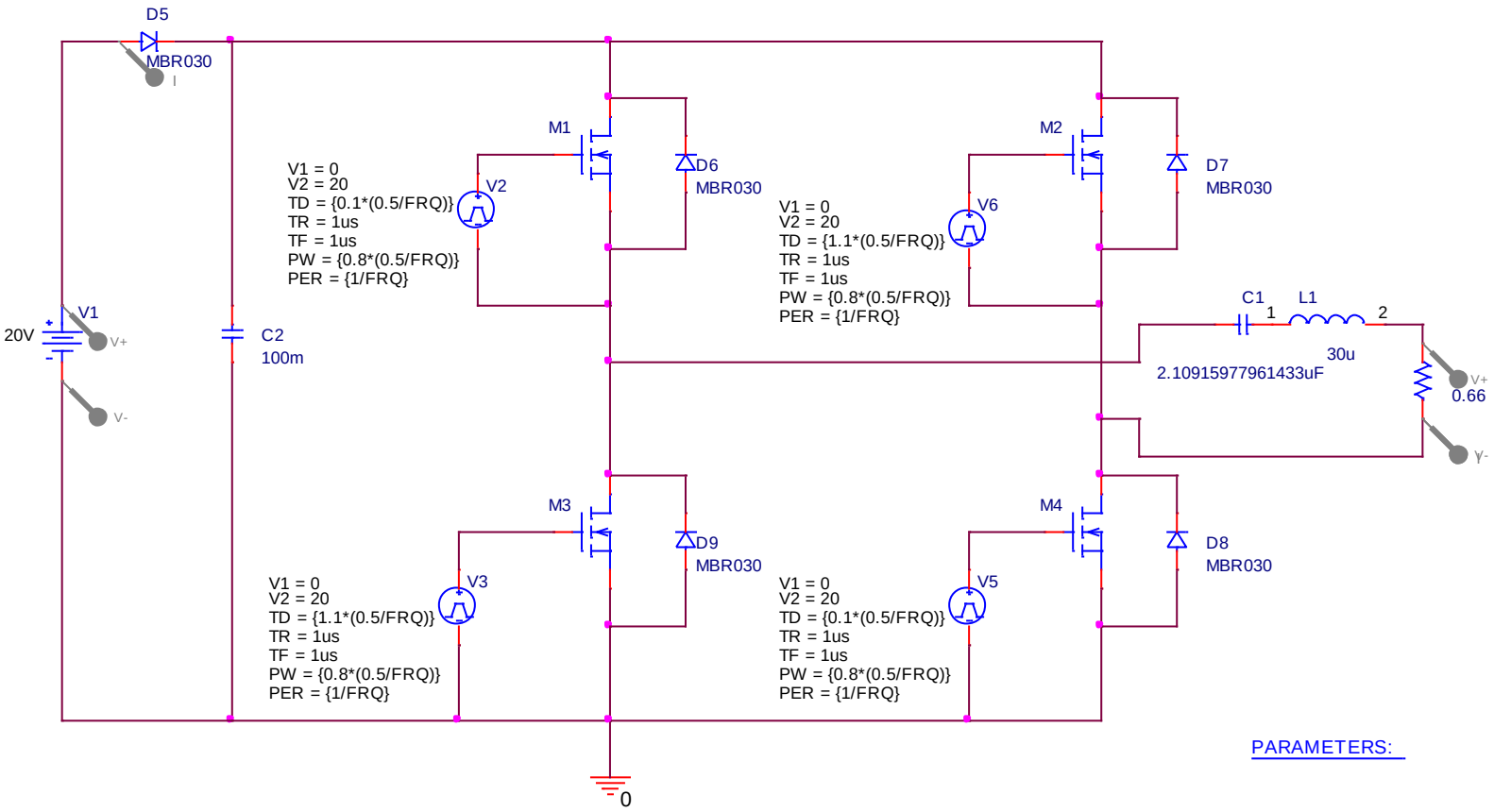

Figure 28. Resonant MOSFET driver using MOSFET SPICE level 3

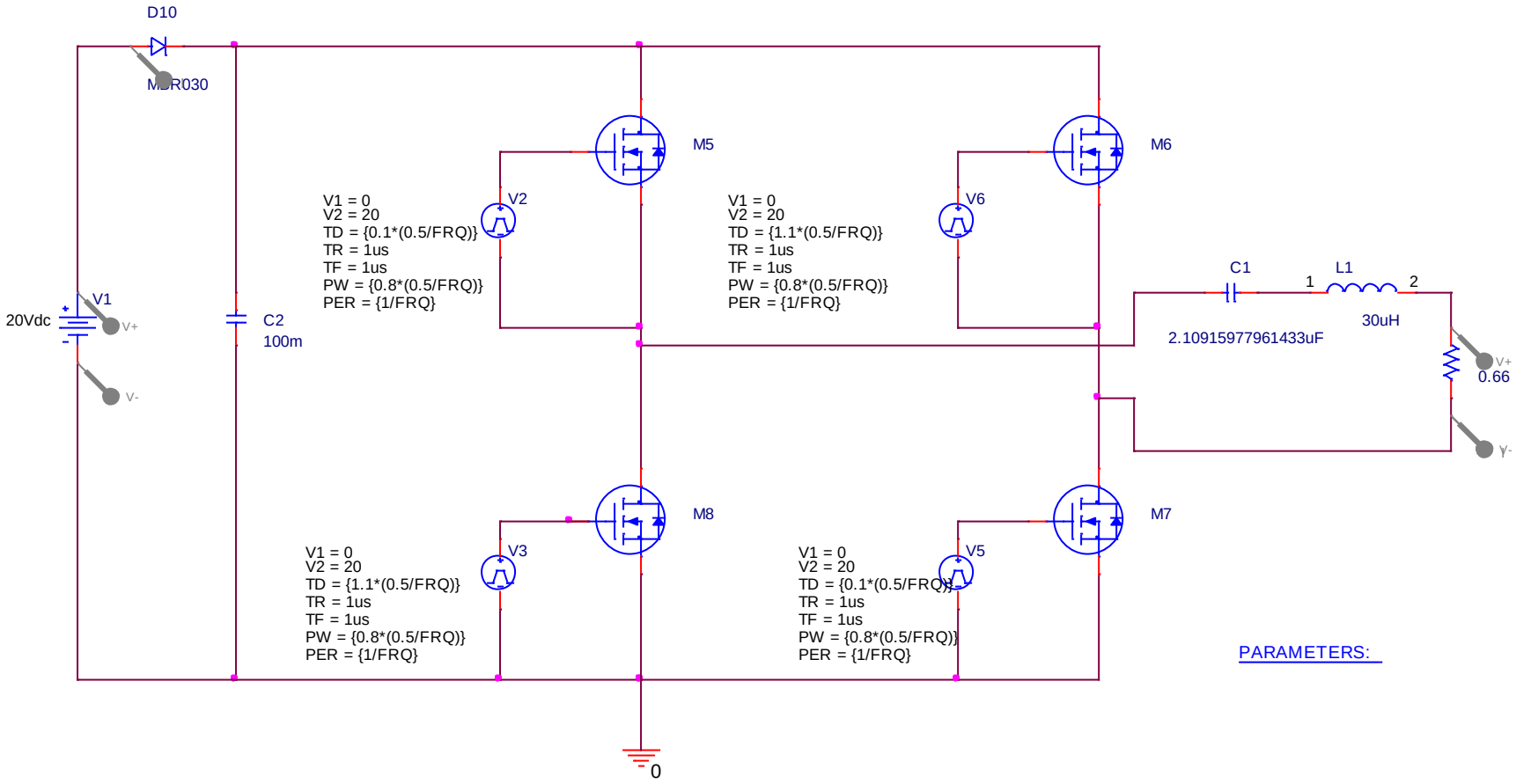

Figure 29. Resonant MOSFET driver using commercial MOSFET

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