IMPROVED SIC SCHOTTKY BARRIER DIODES USING REFRACTORY METAL BORIDES

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ABSTRACT

This research demonstrates how the deposition temperature of Schottky contacts on 4H-SiC affects the electrical and thermal properties of a Schottky diode. Several refractory metal borides are investigated for the contacts which are deposited at room temperature (20 ^{o}C) and high temperature (600 ^{o}C). The electrical properties of the diodes are characterized by using current-voltage (I-V) and capacitance-voltage (C-V) measurements. Thermal properties are investigated by using rapid thermal processor (RTP). Schottky contacts which are deposited at 600 ^{o}C produced better Schottky diodes with smaller ideality factors (from 1.05 to 1.10), barrier heights from 0.94 to 1.15 eV, smaller resistances, and smaller current density in reverse bias conditions when compared to the contacts deposited at room temperature. These values remained stable after annealing in RTP at 600° C for 20 minutes. The improved electrical properties and thermal stability of the diodes with contacts deposited at 600 ^{o}C are related to the removal of O_2 from the boride/SiC interface, as revealed by the Rutherford backscattering spectroscopy (RBS) analysis. These results indicate improved electrical and thermal properties of boride/SiC Schottky contacts, making them attractive for high temperature applications.

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LIST OF SYMBOLS:

A	Area of the diode
A*	Richardson constant ($cm^{-2}K^{-2}$)
E_v	Valence band energy level (eV)
E_C	Energy level of the conduction band (eV)
E_F	Fermi level Energy (eV)
$E_{F, M}$	Fermi level of the metal (eV)
E_G	Band gap energy (eV)
E_i	Intrinsic energy level (eV)
E_{vacuum}	Energy of the free electron (eV)
I_0	Saturation current (A)
I_F	Forward current (A)
J	Current density ($A\text{-}cm^{-2}$)
k	Boltzmann constant (J/K)
K_s	Dielectric constant
n	Ideality factor
N_A	Acceptor doping concentration ($holes/cm^3$)
N_D	Donor doping concentration ($electrons/cm^3$)
q	Electron charge (Coulombs)
R_{on}	On resistance (Ω-cm2)
R_s	Sheet resistance (Ω)
T	Temperature in Kelvin (K)
V_a	Applied bias voltage (V)

V_{bi}	Built- in potential (eV)
W	Width of the depletion region (cm)
ε_0	Permittivity of the material (F/m)
χ	Electron affinity (eV)
Φ_B	Schottky Barrier Height (eV)
Φ_m	Metal work function (eV)
Φ_s	Semiconductor work function (eV)

CHAPTER ONE

INTRODUCTION

In today's technology everyone is interested in high power and high temperature devices. The development and improvement of hybrid vehicles, electric vehicles and fuel cell hybrid vehicles is a major effort by the automotive industries to meet the challenge for reduction in fuel consumption and emission of greenhouse gases. Key performances for the next generation are high breakdown voltage, low on-resistance, high current operation and high temperature operation up to 300 ^{o}C [1, 2]. Schottky diodes are discrete devices with special functions in high power electronics and other integrated circuitry; they are basic building blocks for many transistors such as IGBJTs, MOSFETs etc. Due to their high frequency behavior, Schottky barrier diodes (as opposed to pn-junction diodes) are being extensively used in different applications such as high frequency switches, gas sensors, mixers, microwave circuits and UV detectors [3, 4].

This research demonstrates how the deposition temperature of Schottky contacts improves SiC Schottky barrier diodes for high power and high temperature applications. Schottky contacts are deposited at room temperature (20 ^{o}C) and high temperature (600 ^{o}C). Several refractory metal borides are investigated for the Schottky contacts. The diodes are characterized by using current-voltage (I-V) and capacitance-voltage (C-V) measurements.

Background information of SiC and refractory metal borides is provided. Theory and operation of Schottky diodes, and fabrication technique, and wet etching process are

discussed. The effect of deposition temperature on the fabrication process and analysis of these diodes are provided.

1.1 History of SiC and Refractory Metal Borides

SiC:

Silicon carbide (SiC) was first mentioned by Jons Jacob Berzelius in 1824, and its formation was confirmed by Eugene and Alfred Cowes in 1885 [5]. It does not occur naturally on earth, although it occurs in meteorites. In 1955, Lely introduced a new method of growing this material in the laboratory, and the current method used is a modification of this, now referred to as the modified Lely technique. This breakthrough led to the formation in 1987, of Cree, Inc, the first commercial supplier of SiC. SiC is part of a family of materials which exhibit a one-dimensional polymorphism called polytypism. The difference among the polytypes is in the arrangement of layers of Si and C. In SiC, Si and C are bonded tetrahedrally. Over 200 polytypes of SiC are known to exist. The polytypes are divided into three basic crystallographic categories; cubic (C), hexagonal (H), and rhombohedral (R) **[6]**. Some of the common polytypes includes 3C, 2H, 4H, 6H, 8H, 9R, 10H, 14H, 15R, 19R, 20H, 21H, and 24R. With the exception of 2H and 3C, all of the polytypes form one-dimensional super lattice structures.

Cubic SiC only one possible polytype, and is referred as 3C-SiC or β-SiC. In 3C-SiC, each SiC bi-layer can be oriented into only three possible positions with respect to the lattice while the tetrahedral bonding is maintained. If these three layers are denoted by A, B, and C and the stacking sequence is ABCABC…, then the crystallographic structure is cubic zinc blende. If the stacking of the bi-layers is ABAB…, then the

symmetry is hexagonal and referred to as 2H-SiC. All of the other SiC polytypes are a mixture of the zinc blende (cubic) and wurtzite (hexagonal). 4H-SiC consists of an equal number of cubic and hexagonal bonds. 6H-SiC is composed of two-thirds cubic bonds and one-third hexagonal bonds [6].

SiC is a wide gap semiconductor and this property of SiC yields electronic devices of superior power. Silicon carbide was one of the earliest semiconductors discovered and has strong bonds of silicon and carbon which makes the silicon carbide strong and hard.

Silicon carbide is not attacked by any acids up to 800° C. SiC based devices have higher breakdown voltages than the Si based devices—up to 5 to 30 times higher than the Si based devices. SiC devices are thinner and they have low on-resistance compared to the Si based devices. SiC is extremely radiation hard, meaning radiation does not degrade the electronic properties of SiC to a great extent.

In high temperatures (above 150 °C) operation, Si devices stops working due to the increased leakage current, but SiC can withstand high temperature [4]. One reason for 4H-SiC to withstand high temperature is because it has a higher band gap. The band gap of the 4H-SiC is 3.2 eV, and it can withstand up to 1200 ^{o}C. Relative conductance, breakdown field, and thermal conductivity of the 4H-SiC are greater than the Si which is shown in Table 1. Because of all the properties shown in Table 1, SiC is ideal for developing electronic circuits for high power, high temperature and high frequency applications. Under these circumstances, conventional semiconductors such as silicon (Si) and gallium arsenide (GaAs) are unable to function efficiently [7]. From the Baliga's figure of merit (relative Z_B) 4H-SiC is 2500 times better than the conventional Si

semiconductor for high power and high temperature applications, which is shown in Table 1 (highlighted rows). In Table 1, 4H-SiC properties are highlighted to compare with the other semiconductors.

Table 1. Comparison of SiC with Si [6-12]

Property	**Si**	**GaAs**	**6H-SiC**	**4H-SiC**	**GaN**
Band gap (eV)	1.1	1.4	3	3.2	3.4
Max. Temp. (^{o}C)	300	460	1000	1200	600
Electron Mobility (300K, cm^2/V-s)	1500	8500	370	800	900
Hole Mobility (300K, cm^2/V-s)	450	400	101	115	50
Relative Conductance (λ)	1	7.8	15	90	650
Breakdown field (E_b, 10^6 V/cm)	0.3	0.4	3.2	3	3.3
Thermal Conductivity (σ, W/cm-^{o}C)	1.5	0.5	4.9	3.7	1.3
Sat. electron drift velocity (v_s, 10^7 cm/sec)	1	1	2	2	2.5
Dielectric Constant (K)	11.9	13.1	10.3	10.3	9
Relative $Z_J \sim (E_b v_s)^2$ (pwr/freq)	1	7	250	200	750
Relative $Z_K \sim \sigma(v_s/K)^{1/2}$ (speed)	1	0.5	5	5	2
Relative $Z_B \sim \sigma\lambda E_b$ (pwr/high temp)	1	2.6	400	2500	6200

Consequently, a great deal of research effort has recently focused on wideband gap semiconductor materials, leading to the development of new electronic device structures with remarkable performance. One such device is the Schottky barrier diode (SBD), which if based on SiC would have faster switching speed, large blocking voltage, and function more reliably at higher temperatures, making it very attractive for high power applications. Due to their attractive high frequency behavior, Schottky barrier diodes are being extensively used in different applications such as mixers and detectors, and are actually the most progressed SiC power devices already commercially available. Schottky barrier diodes, along with several other key microelectronic devices such as photo detectors, sensors, and hetero-junction field effect transistors, employ a Schottky

contact where its thermal stability becomes a very important factor at a high input power level. However, the SiC Schottky diodes currently on the market are available up to 1200 V/20 A and are rated for operations only up to 175 °C. Contacts that remain stable up to a target temperature of 500 °C would ensure reliability especially in high temperature applications such as the propulsion systems where engine case temperatures can reach 600 °C [7].

In this research, I worked with 4H-SiC which has a higher band gap compared to the 6H-SiC as shown in Table 1. 4H-SiC was purchased from Cree, Inc., (http://www.cree.com) and it consisted of a low resistive n-type substrate with two n-type epilayers. The epilayers were grown 8° off to the basal (0001) plane of the substrate. The heavily doped n^+ epilayer was first grown on top of the substrate, followed by growth of the lightly doped n^- epilayer.

Refractory Metal Borides and Their Properties:

Boron reacts with many metals in the periodic table to from a wide variety of metal boride compounds. The strong covalent bonding of most borides is responsible for their high melting points and hardness. Most borides are excellent electric conductors with low electrical resistance values [13]. The borides of the high-melting point metals of the fourth, fifth, and sixth periodic groups have properties that render them potentially valuable in very high-temperature structural applications. The high melting metal borides and carbides are about the only refractories suited for use at temperatures around 2500 ^oC and above because of their nonvolatility. The refractory metal borides W_2B_5, W_2B, WB, TiB_2, HfB_2, CrB_2 and ZrB_2 are found to be stable in the presence of carbon [14].

The borides are of no value where an electrically insulating refractory is required because of their conductivity. However, they can be heated inductively or by self-resistance. They make excellent radiation shields because of their high reflectivity and low volatility. The high temperature hardness of the borides is such that they are suitable for high temperature use under abrasive conditions. Because of the three-dimensional boron frameworks, boron-boron bonding results in a lattice of high stability through which the valence electrons, and at high temperatures the metal atoms themselves, can diffuse readily. Such compounds have desirable thermionic emission properties [14].

Refractory metal borides have properties such as very high hardness, very high melting points, and excellent chemical resistance yet very low electrical resistance, making them very attractive as contact metallization for high temperature device applications with the SiC materials. Table 2 shows some properties of the metal borides.

Table 2. Some properties of the borides

Boride	Lattice Const. (°A)	Melting Point (°C)	Thermal Expansion Coeff. ($x10^{-6}$ K^{-1})	Elec. Res. (μΩ-cm)
ZrB_2	3.17	3220	5.9	4.6 (Zr = 42)
CrB_2	2.97	2200	10.5	21
TiB_2	3.03	2600	4.6	28 (Ti = 40)
W_2B_5	3	2860	7.8	19
HfB_2	3.14	3250	5.5	11 (Hf = 30)

1.2 Theory and Operation of a Schottky Diode

The Schottky diode is named after Walter H. Schottky who played a major role in developing the Schottky effect in Schottky diodes. The Schottky diode is a semiconductor diode which has a very low turn-on voltage, approximately 0.15 to 0.45 V

compared to p-n junction diodes. Forward current in a Schottky diode is due to majority carrier injection from the semiconductor to the metal. Reverse current is also due to majority carriers that overcome the Schottky barrier and this is very dependent on temperature. The Schottky diode has fast switching action, and switching speed is controlled by thermalization of hot injected doping carriers of semiconductors across the junction. The switching speed of a Schottky diode will occur in few picoseconds [15].

The semiconductor material used in the research was 4H-SiC with n-type doping. The Schottky diode has two different metal contacts on a semiconductor, a Schottky (rectifying) contact and an ohmic contact. Metal to semiconductor contacts are important since they are present in every semiconductor device. A metal to semiconductor contact can behave as a Schottky barrier or as an ohmic contact depending upon the characteristics of the interface. A metal can be characterized by a work function (Φ_m), the minimum energy required to move an electron from the metal to the vacuum level.

The barrier between the metal and semiconductor can be identified on an energy band diagram. In an energy band diagram, metal and semiconductor are aligned using the same vacuum level as shown in Fig. 1 and Fig. 2. When the metal and semiconductor are brought together there will be a barrier established between the metal and semiconductor interface. This barrier height Φ_B is the energy required to free up an electron from metal (Φ_m) minus the energy required to remove the electron from n-type semiconductor material (called electron affinity, χ) which is given by Eq. 1.1 [15].

$$\Phi_B = \Phi_m - \chi \tag{1.1}$$

Barrier height is measured in the eV and the electron affinity for 4H-SiC is 4.17 eV.

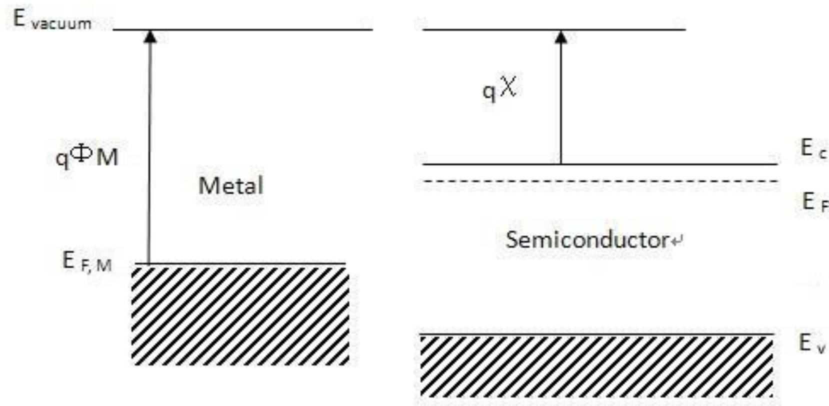

Fig. 1. Energy band gap of M-S before contact

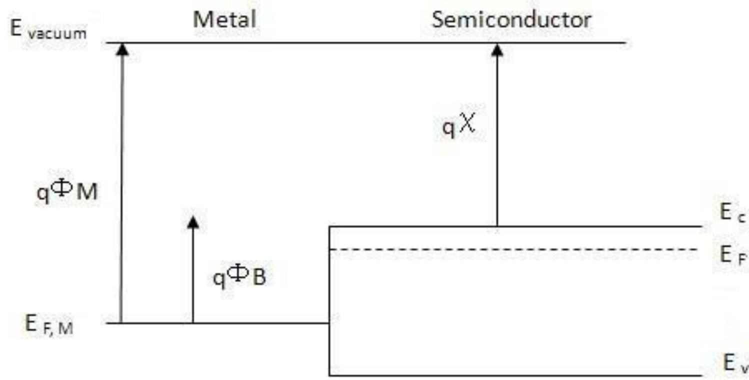

Fig. 2. Energy band gap of M-S after contact and before thermal equilibrium

Whenever metal and semiconductor align together, only a small number of electrons have the energy to get over the barrier and cross to the metal. When a bias voltage is applied to the junction, it can have two effects: it can make the barrier appear lower from the semiconductor side, or it can make it appear higher. The bias does not change the barrier from the metal side. When the barrier is large, the electrons need more

energy to cross the barrier and the contact has rectifying behavior also called Schottky contact. When the barrier is small, electrons can move freely from the semiconductor to the metal and the contact is called ohmic contact. The ohmic behavior is indicated by a linear current-voltage characteristic.

Experimental barrier height often differs from the calculated barrier height due to the chemical reactions between the metal and the semiconductor. The cleaning procedure used and the ideal metal-semiconductor theory assumes both the materials are pure, and that there is no interaction between the two materials and no unwanted interfacial layer [15].

Electrons in the n-type semiconductor can lower energy by traversing the junction. As electrons leave the semiconductor, a positive charge stays behind due to the ionized donor atoms. Electrons flow into the metal until equilibrium is reached between the diffusion of electrons from the semiconductor into the metal and the drift of electrons caused by the field created by ionized impurity atoms. This equilibrium is called thermal equilibrium and it is characterized by a constant Fermi level throughout the structure as shown in Fig. 3. Under thermal equilibrium with no external voltage applied, there is a region in the semiconductor close to the junction which is depleted of mobile carriers; this is called depletion region [15]. The built-in potential, the applied voltage, and the doping concentration play a large role in the width of the depletion region.

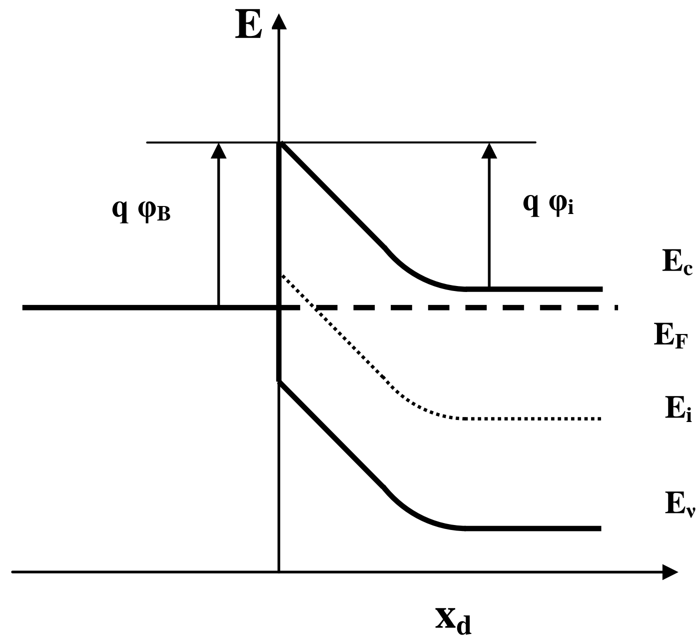

Fig. 3. Energy band diagram of an M-S contact in thermal equilibrium

When a forward-bias voltage V_a is applied to the Schottky barrier, the contact potential will be reduced by qV_a. As a result, electrons in the semiconductor conduction band diffuse across the depletion region to the metal. This gives rise to a forward current. Conversely, a reverse bias increases the barrier and the electron flow from semiconductor to metal is negligible [16].

1.2.1 Current-Voltage (I-V) Characterization

Current flows in a Schottky barrier diode because charge transfers from the semiconductor to the metal or vice versa. The four basic mechanisms by which carrier transportation can occur are:

1) Thermionic emission over the energy barrier

2) Tunneling through the barrier

3) Carrier recombination or generation in the depletion region

4) Carrier recombination in the natural region of the semiconductor

Thermionic emission is the dominant mechanism in Schottky barrier junctions. The thermionic emission is derived from the assumption that the barrier height (ϕ_B) is much larger than kT. Thermal equilibrium established at the junction determines emission and the existence of a net current flow. At the junction, there are two currents, one flow from the metal to the semiconductor and the other flows from the semiconductor to the metal. The current flow depends on the barrier height. In thermionic emission theory, the effect of drift and diffusion in the depletion region is assumed to be negligible [8, 17]. Therefore, the standard thermionic emission relation for electron transport from the metal to the semiconductor with low doping concentration is given by Eq. 1.2a:

$$I_F = I_O \exp\left(\frac{q(V_a - IR_S)}{nkT}\right)\left[1 - \exp\left(\frac{-q(V_a - IR_S)}{kT}\right)\right] \tag{1.2a}$$

I_0 is the reverse saturation current which is dependent on the barrier ϕ_B for electron injection from the metal into the semiconductor and is given by

$$I_O = AA^*T^2 \exp\left(\frac{-q\Phi_B}{kT}\right) \tag{1.2b}$$

where I_F is the forward current, A = area of the Schottky contact, ϕ_B = Zero bias Schottky barrier height, A* = Richardson constant, R_S = series resistance, k = Boltzmann constant and n = ideality factor.

The barrier is unaffected by the applied bias voltage. Under negligible series resistance and high bias ($3kT/q << V_a << IR_S$), the forward current simplifies to Eq. 1.3

$$I_F = I_O \exp\left(\frac{qV_a}{nkT}\right) \tag{1.3}$$

From the forward bias current equation Schottky diodes behave as rectifiers with easy current flow in the forward direction and little current in the reverse direction. Fig. 4 shows the energy band diagram of the metal semiconductor junction under forward and reverse biased conditions.

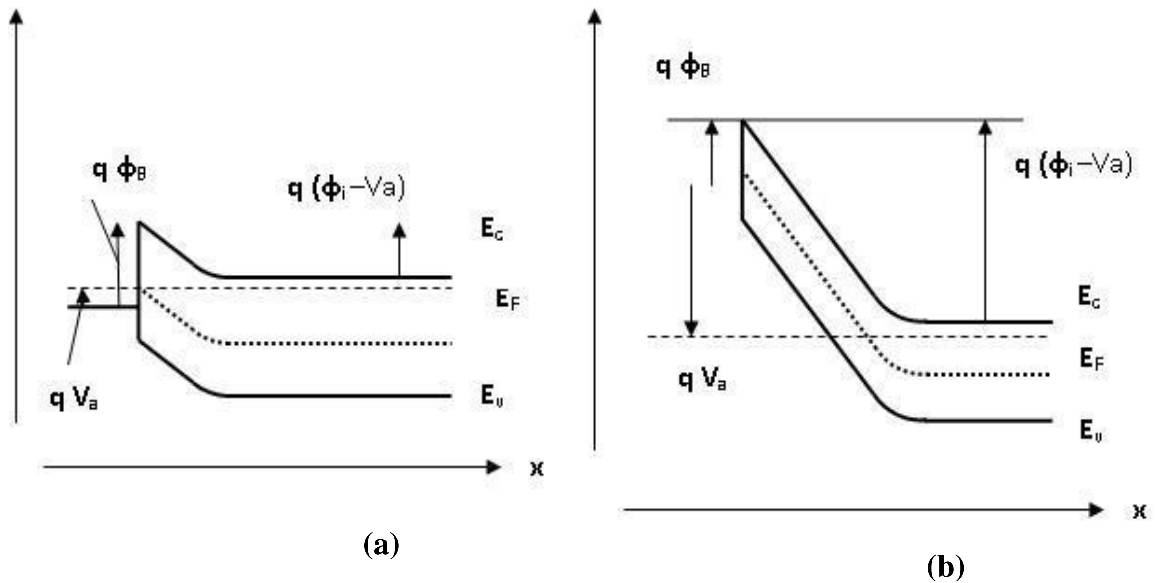

Fig. 4. Energy band diagram of (a) forward biased (b) reverse biased M-S junction

The depletion width is also dependent on the high doping density. High doping concentration makes a thin depletion width and promotes more tunneling. The depletion width is given by Eq. 1. 4.

$$W = \sqrt{\frac{2\varepsilon(V_{bi} - V_a)}{N_D}} \tag{1.4}$$

Where W= Width of the depletion region

V_{bi} = Built-in potential.

V_a = Applied voltage.

N_D = Doping concentration.

ε = permittivity

Taking natural logs of both sides of Eqn. (1.3) gives

$$\mathrm{Ln}(I_F) = \mathrm{Ln}(I_O) + \frac{q}{nkT} V_a \tag{1.5}$$

From eq. (1.2b), we get

$$\mathrm{Ln}(I_O) = \mathrm{Ln}(AA^* T^2) - \frac{q}{kT} \Phi_B \tag{1.6}$$

From the Eq. 1.4, the plot of $\ln(I_F)$ versus the applied voltage V_a gives a straight line whose slope is q/nkT and intercept is $\ln(I_0)$. From this current-voltage (I-V) characterization, the ideality factor (n) can be determined from the slope and the barrier height (ϕ_B) can be determined from the intercept and by using Eq. 1.5.

1.2.2 The On-Resistance (R_{on})

The specific on-resistance (R_{on}) of the diode is an important parameter for high efficiency power devices. In this study, on-resistance was obtained by first determining the series resistance R_s of the diode for the non-linear region of the $\ln(I_F)$ versus V_a plot.

For V>> 3kT/q, Eq. (1.2a) simplifies to

$$I = AA^{*}T^{2}\exp\left(\frac{-q\Phi_B}{kT}\right)\exp\left[\frac{q(V - IR_S)}{nkT}\right] \tag{1.7}$$

where now I_F is represented by I and V_a is represented by V. Eq. (1.6) can be rearranged to give

$$I = \frac{1}{R_S}\left[\frac{dV}{d\ln(I)}\right] - \left(\frac{kT}{q}\right)\left(\frac{n}{R_S}\right) \tag{1.8}$$

By plotting current (I) against dV/d[ln(I)], the series resistance is obtained from the reciprocal of the slope of the linear section of the graph or from the intercept. The on-resistance (R_{on}) is determined by multiplying series resistance with the area of the diode.

1.2.3 The Current-Voltage-Temperature (I-V-T) Characterization

In this research, the current-voltage-temperature (I-V-T) measurements were performed to find out the barrier height, the Richardson constant (A*), and the characteristic energy (E_{oo}) from which the dominant mechanism for the current conduction can be deduced. I-V measurements were performed in the dark at different temperatures ranging from 25 ^{o}C to 250 ^{o}C in steps of 25 ^{o}C. The sample was glued to a heated stage whose temperature was monitored by a thermocouple and the I-V

measurements were performed using the Keithley Sourcemeter. From Eq. (1.2b), the saturation current (I_o) is expressed as

$$I_O = AA^* T^2 \exp\left(\frac{-q\Phi_B}{kT}\right)$$

which can be rearranged to give

$$\mathrm{Ln}\left(\frac{Io}{AT^2}\right) = \mathrm{Ln}(A^*) - \left(\frac{q\Phi_B}{kT}\right) \qquad (1.9)$$

From this, a plot of $\ln(I_s/A_eT^2)$ versus 1/kT referred to as a Richardson plot, can be done and the slope gives $-q\Phi_B$ from which the barrier height Φ_B can be determined. The y-intercept gives the $\ln(A^*)$ from which the Richardson's constant, A*, can be determined. In another version, a plot of $\ln(I_o/AT^2)$ versus 1/nkT, called the modified Richardson plot, can be performed to give values that are independent of the ideality factor.

1.2.4 The Capacitance-Voltage Characterization

The depletion region created when the semiconductor is sandwiched between the ohmic and Schottky contacts is analogous to a parallel plate capacitor. The electrons in the n-type material tunnels into the metal and have a mirrored electric positive charge in the semiconductor which is shown in Fig. 5 [16].

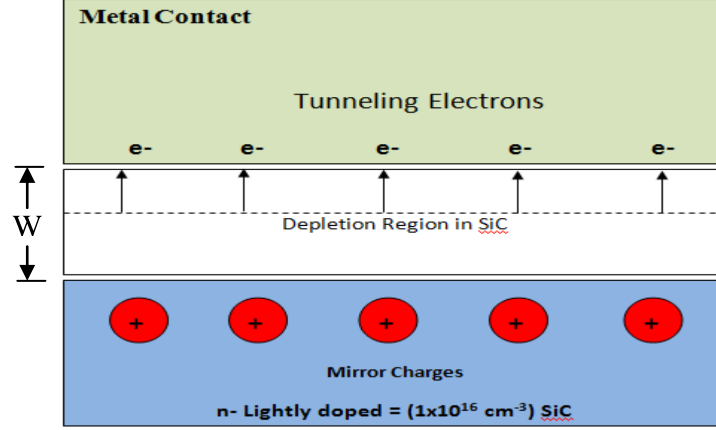

Fig. 4. Schottky contact depletion Region

The capacitance of the Schottky diode is given by Eq. 1.10,

$$C(V) = \frac{\varepsilon A}{W(V)} = A\sqrt{\frac{\varepsilon N_D}{2(V_{bi} - V_a)}} \tag{1.10}$$

where W is the width of the depletion region, V_{bi} is the built-in potential, and A is the area of the diode. Both the built-in voltage (V_{bi}) and doping density (N_D) can be found from $1/C^2$ versus V plot [15].

The C-V measurement is performed by gluing the sample on a copper plate with the Schottky contact facing up. The copper plate, electrically connected to the ohmic contact is wired to the low bias side, while the Schottky contact is connected through a pin-shaped probe to the high bias side of the capacitance meter used. In this work, we used the Agilent Precision LCR meter. C-V values were obtained by superimposing a small alternative voltage of 10 mV at 1 MHz on the reverse dc bias and the resulting data was analyzed using the relation

$$\left(\frac{\mathrm{A}}{\mathrm{C}}\right)^2 = \frac{2\left[V_{bi} - \frac{kT}{q}\right]}{qk_s\varepsilon_0 N_D} + \frac{2\mathrm{V}}{qk_s\varepsilon_0 N_D} \qquad (1.11)$$

where A = Area of the Schottky contact, V_{bi} = built-in potential, k_s = semiconductor dielectric constant, N_D = doping concentration of the semiconductor, k = Boltzmann constant, T = temperature in Kelvin and ε_0 = permittivity of free space.

By plotting $(A/C)^2$ versus the reverse bias voltage V, a straight line is obtained whose slope is $2/q\varepsilon_0 N_D$. From the value of the slope, the semiconductor doping concentration N_D, can be computed. The intercept on the V-axis is numerically equal to $V_i = -V_{bi} + kT/q$, and from this value, the built-in potential V_{bi} is obtained. Then the Schottky barrier height is computed using the relation

$$\Phi_B = \mathrm{Vi} + \left(\frac{kT}{\mathrm{q}}\right)\left[1 + \ln\left(\frac{N_O}{N_D}\right)\right] \qquad (1.12)$$

where the value $N_o = 1.69\times10^{19}$ cm^{-3} was used for the effective density of state for 4H-SiC [7].

CHAPTER TWO

SCHOTTKY DIODE FABRICATION

2.1 Preparing SiC Substrate and Ohmic Contacts

A Schottky diode consists of both ohmic and Schottky contacts. An ohmic contact was deposited on the heavily doped backside of the n-type 4H-SiC substrate and a Schottky contact was deposited on the lightly doped n-type 4H-SiC epilayer on the front side. The n-type 4H- SiC used consisted of a 400-um thick substrate with a resistivity of 0.019 Ω-cm which contained two n-type epilayers grown 8° off the basal (0001) plane. The first epilayer was 0.5 μm thick with $N_D \sim 1 \times 10^{18}$ cm^{-3} and the second epilayer was 4.6 μm thick with $N_D \sim 1\times 10^{16}$ cm^{-3}. The SiC wafer was diced into 5×5 mm^2. A sacrificial layer of SiO_2 of 30 nm thickness was grown at 1150 ^oC on the SiC surface to help improve the surface morphology. These were cleaned using the standard RCA (Radio Corporation of America) cleaning process, which was boiling in acetone (3 min), boiling in isopropyl alcohol (3 min), and rinsing with de-ionized water. The samples were then kept in diluted hydrofluoric acid (1HF: $10H_2O$) for three minutes to strip the sacrificial layer, rinsed with de-ionized water and dried. The samples were mounted in the vacuum chamber with the thickness monitor attached. The samples were placed 10 cm away from the sputter target. The vacuum chamber was pumped down to a base pressure of 8.4×10^{-7} Torr. After reaching this pressure, argon gas was allowed in the chamber with its flow controlled by a mass flow controller. The Ar gas flow rate was maintained at 15 SCCM (standard cubic centimeters per minute) and the pressure of the

chamber during deposition was held at 2 mTorr. Metals used for the ohmic contact were Titanium (Ti) and Nickel Gallide ($Ni_{0.9}Ga_{0.1}$), that is reported to form low resistance ohmic contact on n-type 4H-SiC [18]**.** The ohmic contact was deposited on the heavily doped substrate (backside). The heavy doping decreases the junction barrier height and makes the thickness of the depletion width extremely narrow, and promotes the probability of electron tunneling from the semiconductor to the metal. The titanium was sputtered at a current of 0.1 A to a thickness of 20 nm, followed by nickel gallide sputtered at a current of 0.05 A to a thickness of 80 nm thickness, and finally, another titanium layer sputtered to a thickness of 10 nm. Thickness of the ohmic contact metals was monitored by the thickness monitor, which was calibrated for each metal. One minute of pre sputtering time was allowed before depositing each metal to clean the surface oxides from the target. Fig. 6 shows the SiC with an ohmic contact on the backside.

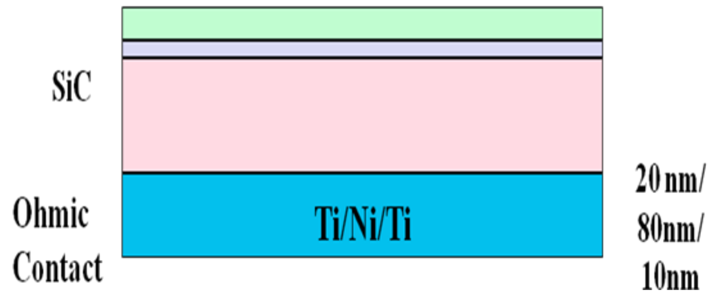

Fig. 5. Silicon carbide with an ohmic contact on the back side

After depositing the ohmic contact the samples were taken out of the vacuum chamber and cleaned in boiled acetone, alcohol, and rinsed with de-ionized water. The

samples were annealed using rapid thermal processor (RTP) in pure nitrogen (N_2) at 950 ^oC for 2 min. Pure N_2 limits oxidation of the contact during annealing. By annealing, the metal will interact with the semiconductor and form a contact with very low electric resistance.

2.2 The Schottky Contacts

Schottky contacts are formed when the metal work function is greater than the n-type semiconductor work function. If the metal work function is greater than the n-type semiconductor work function, then a potential barrier will be established between the metal and the semiconductor. This potential barrier makes the electrons flow from the semiconductor to the metal and blocks the electrons that flow from the metal to the semiconductor. Breakdown voltage occurs when electrons flow from the metal to the semiconductor. Schottky contacts are always deposited on the lightly doped side of the n-type 4H-SiC.

The samples were cleaned again in boiled acetone and alcohol, rinsed with de-ionized water and dried. The samples were attached to a heater (two 500-W halogen lamps) and a thermo couple used for monitoring the temperature of the sample. The heating temperature was controlled by an external voltage controller. The vacuum chamber was then pumped down to a base pressure of 8.8×10^{-7} Torr and the refractory metal borides used as Schottky contact were deposited. The samples were preheated at 600 ^oC for about an hour enable thermal desorption that helps make the surface of the sample cleaner through evaporating away unwanted contaminants such as water vapor or dust on the sample surface. The Schottky contacts were deposited at a base pressure of 2 mTorr by allowing argon gas to flow at a rate of 15 SCCM. The metal borides which

were deposited were W_2B_5, W_2B, WB, TiB_2, HfB_2, and CrB_2. All these metals were sputtered at room and high temperature (600 ^oC) on different samples for an hour with a current of 0.05 A. The choice of these deposition temperatures is explained in Chapter 3 section 1. The temperature was increased slowly with a power stat and monitored with the thermo couple. After reaching the desired temperature (600 ^oC), metal was pre sputtered for two minutes and sputtered for an hour to make the Schottky contact. Note that the Schottky contact metals are deposited on the whole sample (called blanket deposition). Fig. 7 and Fig. 8 show the high vacuum chamber, the sputter targets, and the plasma sputter deposition process.

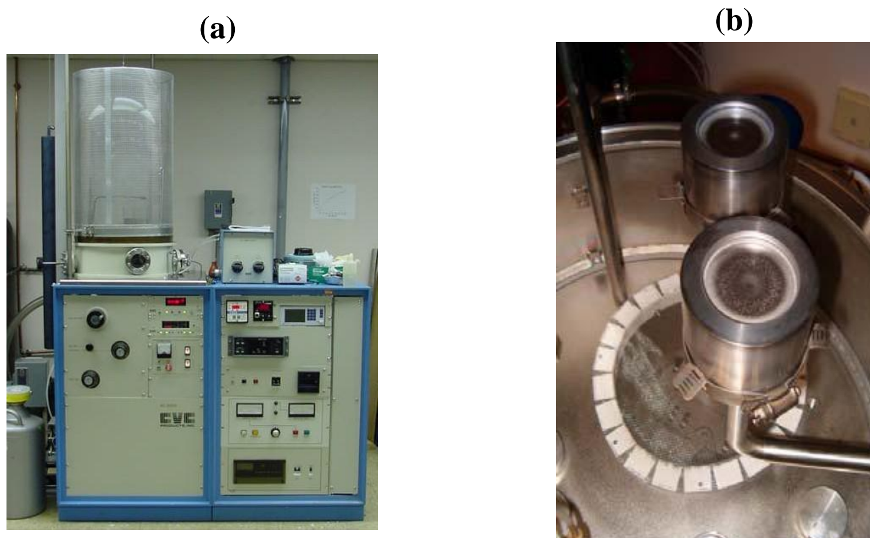

Fig. 6. (a) Plasma sputter deposition chamber and (b) the sputter targets

2.3 Patterning the Schottky Contact

To make individual Schottky diodes, the blanket deposited Schottky contact metal requires patterning where unwanted metal is removed in appropriate acidic etchants. To accomplish this, the samples were cleaned again in boiled acetone and alcohol, rinsed with de-ionized water and dried. A photolithographic process was carried by uniformly

spreading a positive photoresist (AZ5214) using a spin coater on the sample surface. The spin coater was operated at 5000 rpm for 30 sec to spread the photo resist uniformly into a thin layer on the sample surface. The samples were then placed on a hot plate at 110 ^{o}C for one minute to bake the photoresist and evaporate the resist solvent. The samples were exposed to UV light through photo mask for 3 minutes in the mask liner. The photo mask image transferred to the samples after being exposed to UV light.

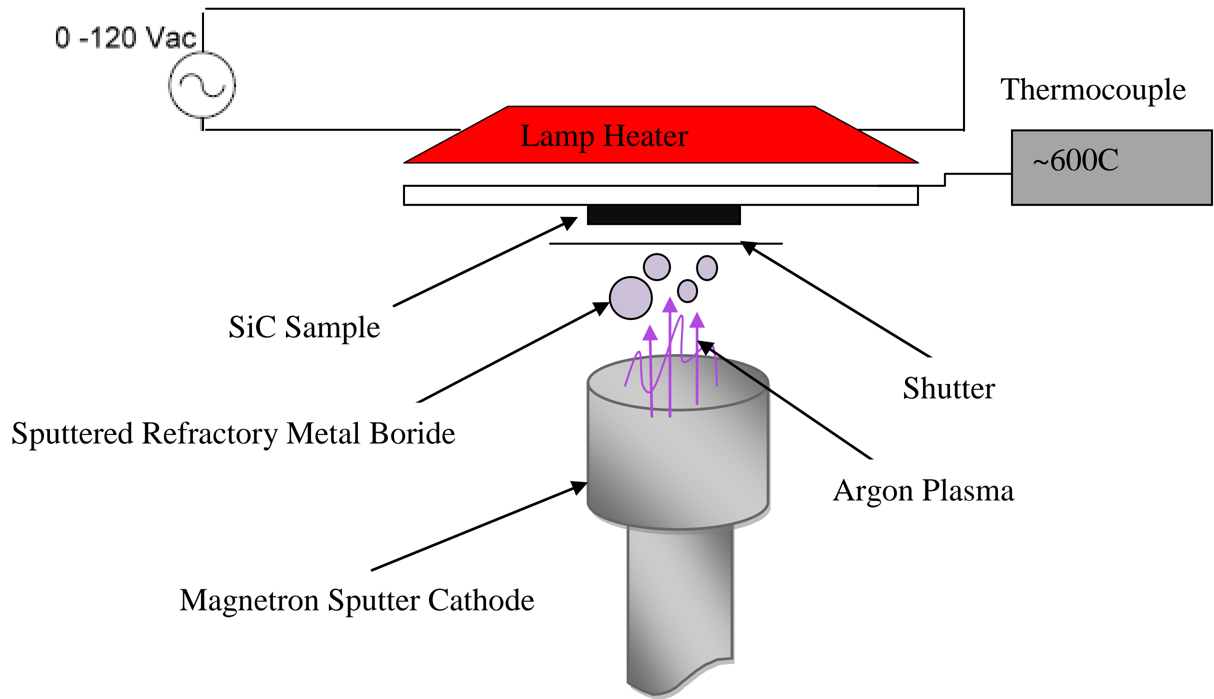

Fig. 7. Plasma deposition process

These samples were developed using the AZ 400K developer for 45 sec and quickly rinsed in water for 40 sec. The developer which used was diluted with water, that is, 1 part AZ400K to 4 parts H_2O. In the positive photolithography process exposure to UV light breaks the chemical bonds in the material so that the exposed region dissolves in the developer and the unexposed region remains. The pattern on the sample is the same as the pattern on the mask. Fig. 9 shows the UV mask liner and the spin coater.

Fig. 8. (a) UV mask liner and (b) spin coater

After completing the positive photolithography the samples were baked at 120 ^{o}C on a hot plate for 2 minutes to harden the photo resist, a critical step needed when acid etching is to be performed. The ohmic contact was protected by mounting the backside of the sample to a Si wafer before dipping the samples in the acid. The acidic solution used to etch most of the refractory metal borides was three parts hydrochloric acid to one part nitric acid (1HCl: 3HNO_3). The samples were placed in the acid solution for 1 minute, dipped in water, and observed under the microscope and this was repeated to ensure that all the unwanted metal was removed. If left too long in the acid solution, it was found that all the Schottky contact got etched away. The contacts deposited at room temperature required about 5 min dip in the acid solution while the boride Schottky contacts deposited at 600 ^{o}C required about 3 min acid dipping. The chemical for etching HfB_2 was one part

hydrofluoric acid to one part nitric acid (HF: HNO_3), which was different from the ones used for the other refractory metal borides. All the samples needed to be rinsed thoroughly in water after being removed from the acid. In chemical etching, the metal covered by the photo resist is protected and metal not covered by the photo resist is etched away. Finally, photo resist was removed by soaking the sample in acetone for 10 minutes, rinsing in alcohol and water and dried. After the lift-off process, the samples were left with many Schottky diodes that had an ohmic contact on the backside and a Schottky contact on the front side. The defined circular Schottky contact had diameters of approximately 150 µm, 170 µm, 180 µm, 190 µm, and 200 µm. The final structure and top view of the diode is shown in Fig. 10.

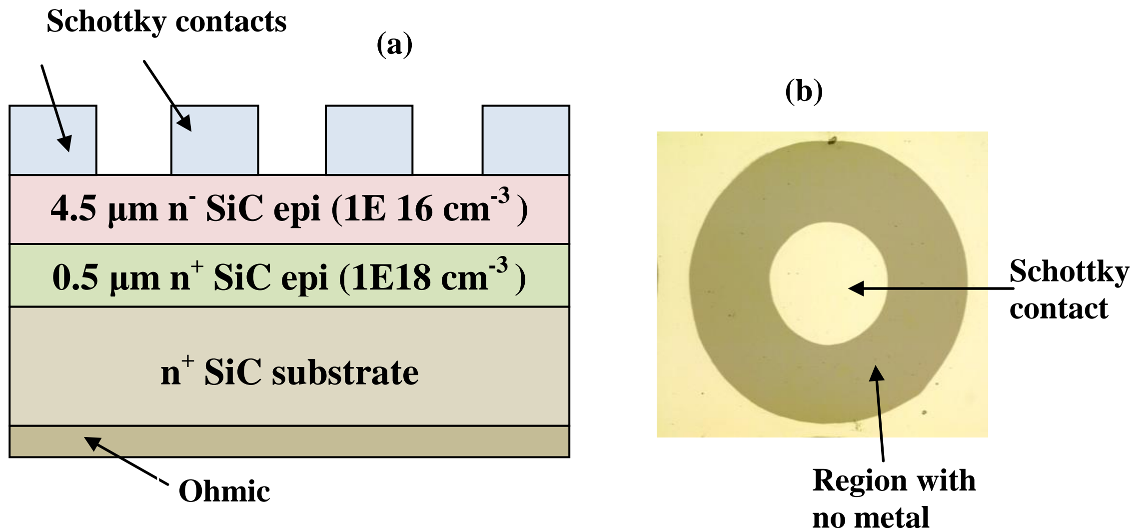

Fig. 9. (a) Final Schottky diode structure and (b) Top view showing the Schottky contact

CHAPTER THREE

EFFECT OF DEPOSITION TEMPERATURE USING I-V MEASUREMENTS

3.1 Previous Work with ZrB_2

The refractory metal boride Schottky contacts used in this work were deposited at two different temperatures: 20 ^oC (room temperature) and 600 ^oC (high temperature). The choice of the 600 ^oC used was based on previous results performed on ZrB_2 contact and reported by Oder et al. [19]. ZrB_2 was deposited as a Schottky contact on n-type 4H-SiC at different temperatures of 20 ^oC, 200 ^oC, 400 ^oC, 600 ^oC and 800 ^oC and the resulting Schottky barrier diodes were characterized.

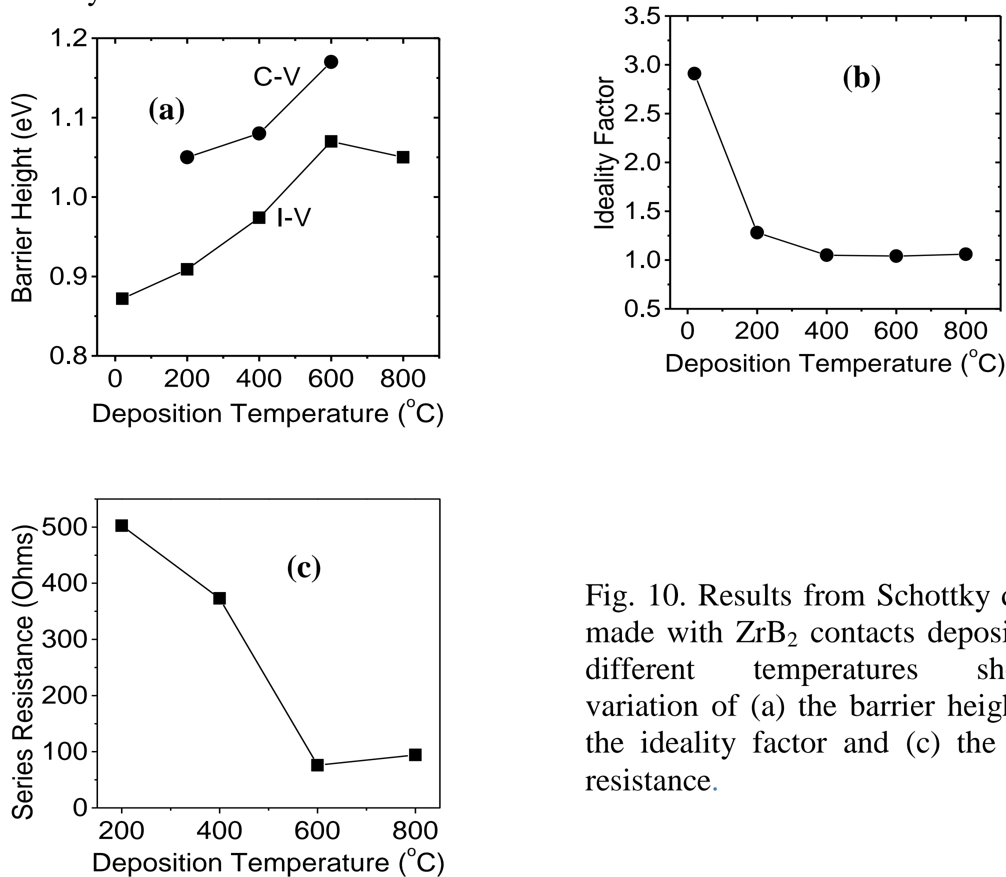

Fig. 10. Results from Schottky diodes made with ZrB_2 contacts deposited at different temperatures showing variation of (a) the barrier height, (b) the ideality factor and (c) the series resistance.

Fig. 11 (a) shows a plot of the Schottky barrier height (SBH) versus the deposition temperature of the ZrB_2/SiC Schottky contacts. As can be seen from this figure, there is a remarkable increase of the SBH from 0.87 eV for deposition temperature of 20 ^{o}C to 1.07 eV for a deposition temperature of 600 ^{o}C from the I-V measurements ($\Delta\Phi_B = 0.20$ eV). The C-V measurements revealed a similar trend with slightly higher values for the SBH of 1.05 eV for contacts deposited at 200 ^{o}C to 1.17 eV for contacts deposited at 600 ^{o}C. Fig. 11 (b) shows the variation of the ideality factor (n) with the deposition temperature. It is seen here that the ideality factor decreases from 2.91 for contacts deposited at 20 ^{o}C to 1.06 for contacts deposited at 600 ^{o}C, indicating improvement of the interface homogeneity.

A no ideal Schottky diode with ideality factor greater than one suggests the presence of other carrier transport mechanisms in addition to thermoinic emission. For such a diode, the flat band Schottky barrier height, independent of the current conduction mechanism, provides a more representative value. Thus for the results of our I-V measurements shown in Fig. 11 (a) and (b), the larger ideality factors at lower deposition temperatures result in underestimated barrier heights that can reduce the trend of SBH increase with increasing deposition temperature. However, theoretical and experimental studies have shown that SBH determined by C-V method essentially match the flat band SBH [20, 21]. The values of the SBH we determined by C-V measurements shown in Fig. 11 (a) confirm the trend of increasing SBH with the deposition temperature. Note that the trend is less for the C-V measurements than for the I-V measurements. An estimate of the series resistance (R_S) of the as-deposited Schottky contacts was made using the procedure outlined in chapter 2. Fig 11 (c) shows the variation of the average

values of R_S with the deposition temperature. As can be seen here, there is a decrease in the value of R_S from about 502 Ω to 76 Ω as the deposition temperature was varied from 200 °C to 600 °C, and slightly rising to about 94 Ω for contacts deposited at 800 °C.

To study the physical properties of the boride/SiC films with the alteration of the substrate temperature during deposition, several unpatterned SiC samples were prepared. ZrB_2 films were deposited on each sample at different temperatures of 20 °C, 200 °C, 400 °C and 600 °C. The samples were then analyzed using Rutherford backscattering spectroscopy (RBS), and the resulting spectra from these films are shown in Fig. 12. The inset is an expanded view of the spectra showing the decrease in the oxygen peak with the deposition temperature. From the simulation of these spectra, the Zr:B:O ratios at these deposition temperatures are 1:2:1 at 20 °C; 1:2:0.4 at 200 °C; and 1:2:0 at 400 °C and 600 °C.

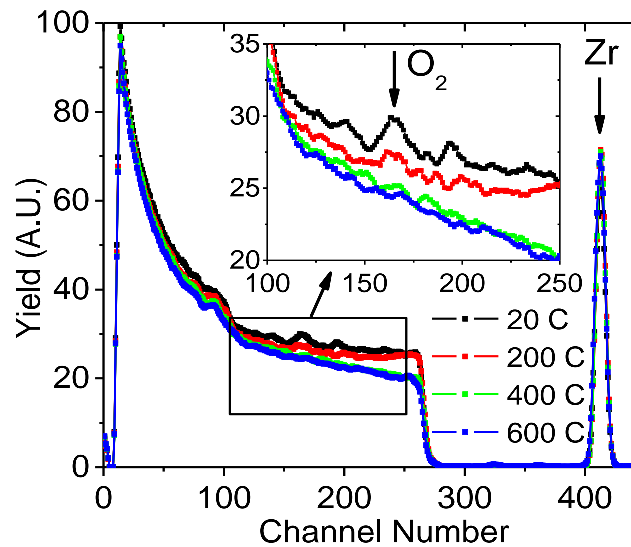

Fig. 11. Rutherford backscattering spectra of ZrB_2 films deposited on SiC at different temperatures. The inset shows an expanded view of the spectra showing the decrease of the O_2 peak with deposition temperature.

This implies that deposition of the borides on SiC held at or above 400 ^{o}C results in little or no O_2 in the boride/SiC contacts. The escape of O_2 in the form of volatile B_2O_3 has been reported in investigations of CrB_2 and TiB_2 films [22, 23]. It is therefore plausible to expect that in the boride contacts here studied, O_2 would similarly escape by way of oxides such as B_2O_3 or H_3BO_3 known to be volatile at 300 ^{o}C, when these borides are deposited on SiC substrates held at 400 ^{o}C and above [24, 25]. Since the presence of impurities such as O_2 at the interface is known to contribute to undesirable electrical characteristics, the improvement of the barrier properties of the boride/SiC contacts is possibly due to the escape of O_2 from the metal/SiC interface. For this reason, the temperature of 600 ^{o}C was selected as the one at which all the boride contacts in this study would have their optimum electrical properties, when compared to boride contacts deposited on unheated SiC samples.

3.2 I-V Characterization

The current-voltage (I-V) measurements were taken on at least five different Schottky diodes separately for those with the Schottky contacts deposited at room and those with the contacts deposited at 600 ^{o}C. The samples were glued to a copper plate using conductive silver paste with the backside ohmic contact attached to the copper plate which was connected by a wire to the negative terminal of the Keithley Sourcemeter (model 2400). The Schottky contact on the top side of the sample was connected to the positive terminal through a small probe. A Labview software program written for the I-V measurements was used to collect the data, where the current was measured as the voltage was varied from 0 to 3 volts for the forward bias measurements. In this range,

300 data points were collected. For reverse bias measurements, the voltage was varied from -20 V to 0 volts. Figure 13 (a) shows the Keithley Source meter used for this characterization and Fig. 13 (b) shows three samples glued to the copper plate used in the measurements.

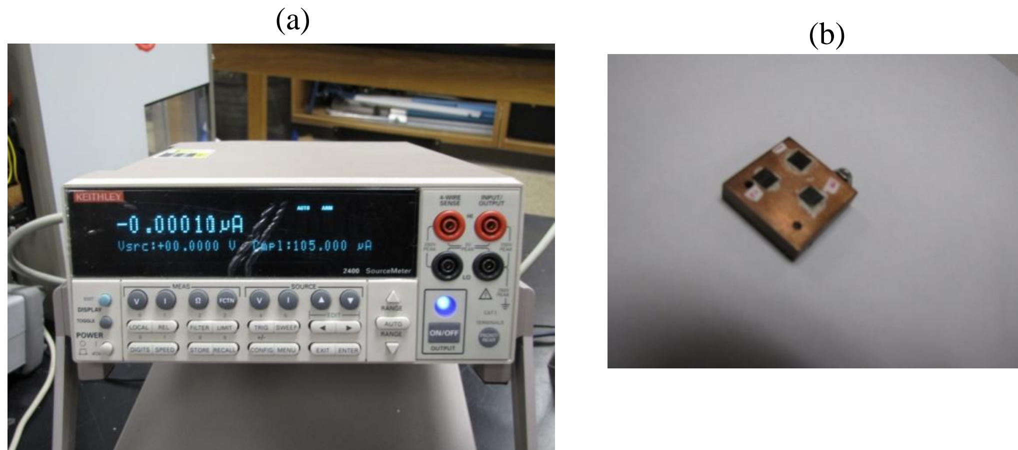

Fig. 12. (a) Keithley source meter (b) samples on a copper plate

To test for thermal stability of the diodes, the samples were then removed from the copper plate, thoroughly cleaned with acetone to remove residual silver paste and placed in the rapid thermal processor for annealing. The annealing was performed in a pure nitrogen environment to eliminate oxidation of the samples when raised to a high temperature. Each sample was annealed at 600 ^{o}C for 20 minutes. Following the annealing, the samples were again glued to the copper plate and the I-V measurements repeated. Where possible, the I-V measurements were performed on the same diodes for accurate comparison of the results obtained before and after annealing. The results from these measurements were analyzed using the Schottky-Mott theory where thermionic emission is assumed as the dominant charge transport mechanism. Fig. 14 shows the plot

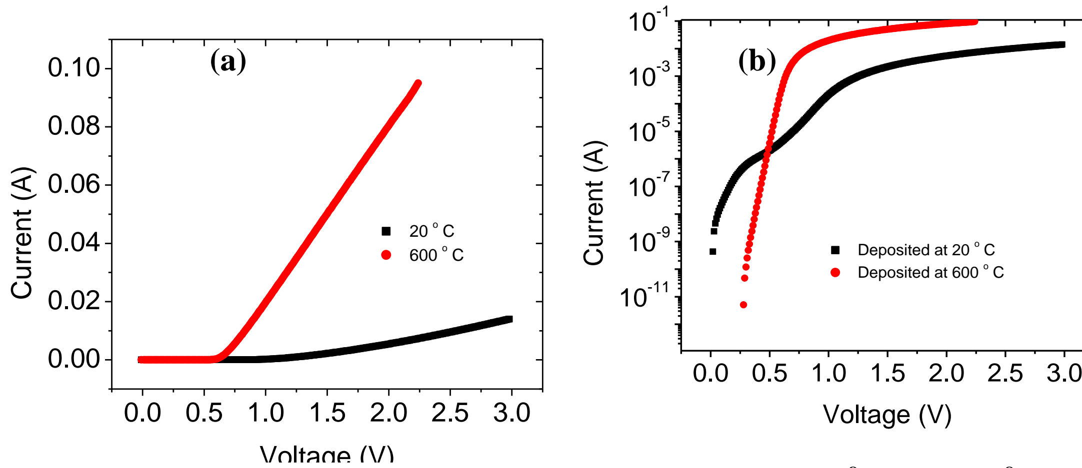

Fig. 13. Current- voltage data for the borides deposited at 20 ^{o}C and 600 ^{o}C. (a) shows the plot with both I and V on linear scales and (b) shows the plot with I on a log scale while V is on a linear scale.

of the data on a linear scale and on a semi log scale. The linear portion of the semi log plot (under low voltage, prior to roll-over, Fig. 14 (b)) is extracted and analyzed. Its slope is used to compute the ideality factor and its intercept is used to compute the Schottky barrier height. Since the slope = q/nkT, it implies that the steeper linear portion will yield a smaller value of the ideality factor.

Fig. 15 shows a semi log I-V plot from diodes made with WB Schottky contacts and deposited at 20 ^{o}C. I-V measurements were done on as-deposited Schottky contacts and then after the diodes were annealed at 600 ^{o}C for 20 min. As can be seen, the low-voltage linear portion of this plot is not very straight, indicating a poor quality diode. By contrast, similar plots for diodes with WB contacts deposited at 600 ^{o}C (Fig. 16) shows a more linear semi log plot which remains unchanged even after the annealing at 600 ^{o}C for 20 min in N_2. The calculations and analyses of these measurements were conducted with the help of equations explained in Chapter 2 and the results are shown in Fig. 17 and Fig. 18.

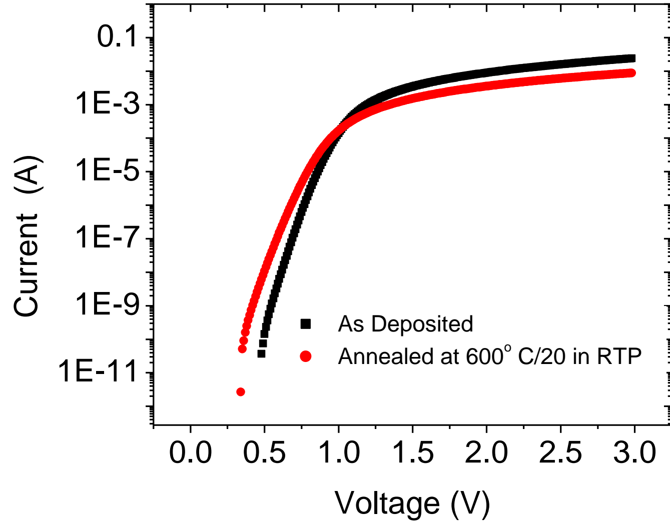

Fig. 14. Semi log I-V plot from diodes made with WB Schottky contacts deposited at 20 °C before annealing and after annealing at 600 °C/20 min in N_2.

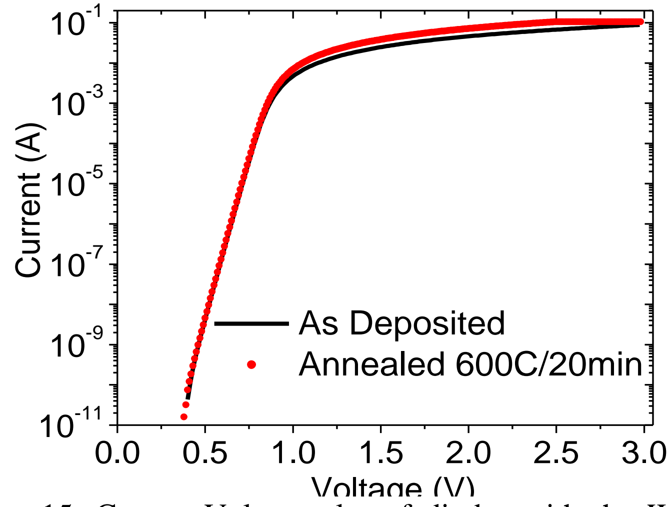

Fig. 15. Current-Voltage plot of diodes with the WB deposited at 600 °C before (as-deposited) and after annealing at 600 °C for 20 min in N_2.

A contrast can be seen in diodes with the Schottky contacts deposited at room temperature compared to the Schottky contacts deposited at high temperature (600 °C). For WB and W_2B metals, room temperature deposition didn't yield good ideality values

because the data was not good enough to extract these values. When ideality value was close to one, the value of the barrier height could be trusted. The Schottky contacts which were deposited at 600 ^{o}C have ideality values approximately equals to one when compared to those deposited at 20 ^{o}C.

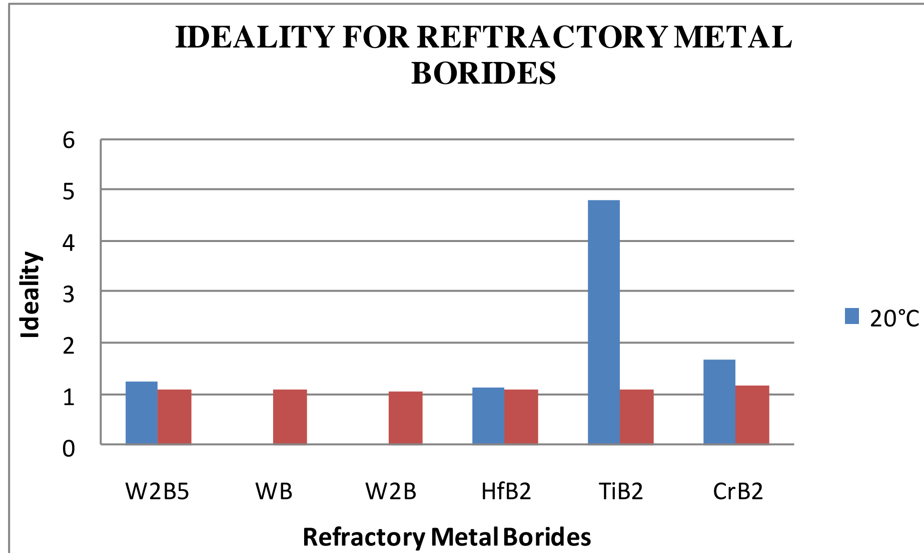

Fig. 16. Values of the ideality factor for the refractory metal borides

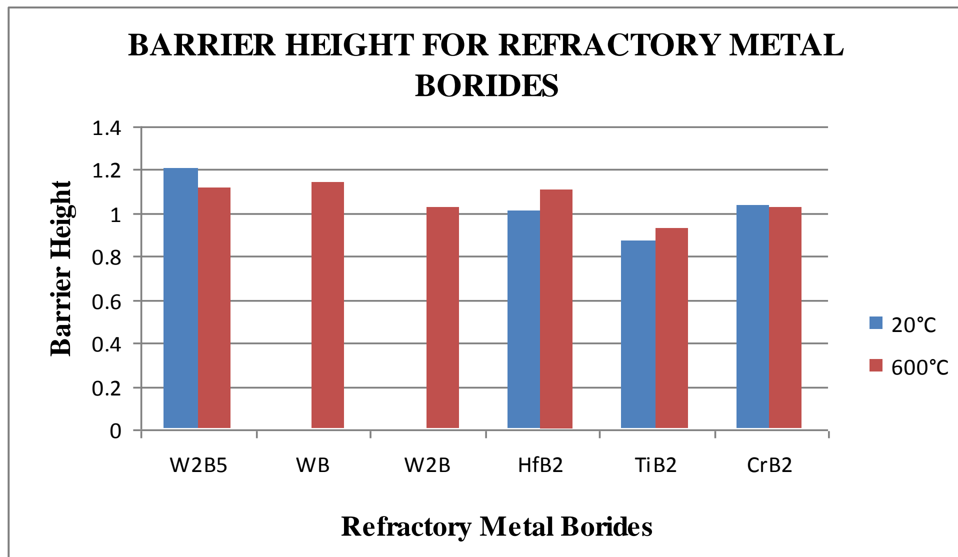

Fig. 17. Values of the Schottky barrier heights for the refractory metal borides

3.3 Measurement and Analysis of the Contacts in Reverse Bias

Reverse bias I-V characteristics were performed to find the leakage current density and breakdown voltage of the Schottky diodes. The Keithley source meter available in our laboratory for this investigation has a voltage range of 5 µV to 20 V. This range is not sufficient to measure the breakdown voltage of the Schottky diode. However, leakage current densities at -15 V were measured for the Schottky diodes which were deposited at room and high temperature (600 ^{o}C). Fig. 19 shows the leakage current densities at room and high temperature. From the appendix 5 and 6 and from Fig. 19, a contrast can be seen in the Schottky contacts deposited at high temperature compared to the Schottky contacts deposited at room temperature.

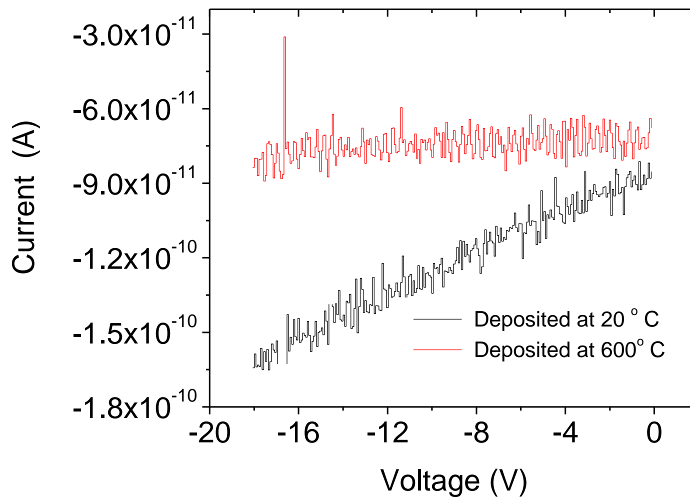

Fig. 18. I-V plots of W_2B contact diodes deposited at 20 ^{o}C and 600 ^{o}C

3.4 Determination of the Specific on-Resistance

The specific on-resistance (R_{on}) of the diode is an important parameter for high efficiency power devices. In this study, on-resistance was obtained by first determining the series resistance R_s of the diode for the non-linear region of the ln(I) versus V plot. As explained in Chapter 2, if V >> 3kT/q, we can use the equation

$$I = AA^{*}T^{2}\exp\left(\frac{-q\Phi_{B}}{kT}\right)\exp\left[\frac{q(V-IR_{S})}{nkT}\right] \tag{3.1}$$

which can be rearranged to give,

$$I = \frac{1}{R_S}\left(\frac{dV}{d[\ln(I)]}\right) - \left(\frac{kT}{q}\right)\left(\frac{n}{R_S}\right) \tag{3.2}$$

A graph of I versus dV/d[ln(I)] was plotted and the series resistance was then obtained from the reciprocal of the slope of the linear section of graph. The specific on-resistance was determined by multiplying series resistance (R_S) by the area (A) of the diode.

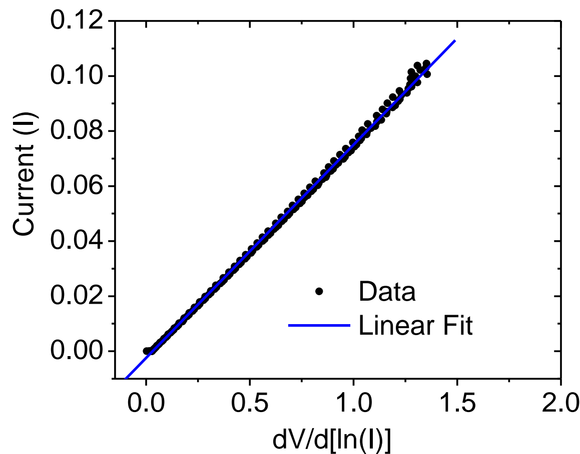

Fig. 19 A plot of current I versus dV/d[ln(I)] of a W_2B contact deposited at 600 ^{o}C

Fig. 20 shows a plot of I versus dV/d[ln(I)] with non-annealed W_2B deposited on silicon carbide at 600 ^oC, yielding a typical resistance of 13Ω with the diode contact area 2.83×10^{-4} cm^2; the calculated specific resistance was 3.72m Ω-cm [7]. The series resistances of all the Schottky diodes were obtained. Different Schottky diodes have different series resistance. Appendices 7 and 8 show the steps for the calculation of series resistance.

3.5 Results from I-V-T Measurements

In this research, current-voltage-temperature (I-V-T) measurements were performed only on CrB_2/SiC samples. The I-V-T measurements were performed to find out the Richardson constant, and barrier height of the diodes. The characteristic energy values, from which the current-conduction mechanism can be deduced, were not determined in this work. The I-V-T measurements were performed when the samples were glued using silver paste to a plate underneath which was a ceramic heater. The temperature of the sample was monitored using a thermocouple and the I-V measurements were performed for each set temperature ranging from 25 ^oC to 250 ^oC in steps of 25 ^oC. I-V characteristics were obtained with Keithley source meter after the temperature stabilized in increments of 25 ^oC. The ideality factor and the saturation current parameters were extracted from the linear region of the forward bias I-V characteristics. The standard diode equation Eq. 3.1 was used to extract the ideality factor (n) and saturation current (I_s), which is expressed as

$$I_o = AA^*T^2\exp\left(-\frac{q\Phi_B}{kT}\right) \tag{3.3}$$

After rearranging the Richardson constant A^*, zero-bias barrier height Φ_{bo} can be obtained from

$$\ln\left(\frac{Io}{AT^2}\right) = \ln(A^*) - \left(\frac{q\Phi_B}{kT}\right) \tag{3.4}$$

Plot of 1/kT versus $\ln(I_s/A_eT^2)$ is referred to as a Richardson plot where the slope gives the barrier height and the y-intercept is $\ln(A^*)$. From the y-intercept a Richardson constant was obtained.

Current density-voltage data at selected temperatures of CrB_2/SiC Schottky diodes are shown in Fig. 21 (log plot). Linear plot of the CrB2/SiC at 25 °C and 250 °C is shown in Fig. 22. From the log plot, intercept and slope were obtained, and from those values ideality factor and barrier height values were obtained. After finding I_s from the standard diode equation, plotted 1/kT versus $\ln(I_s/A_eT^2)$ and the Richardson constant were obtained. The value obtained did not match the theoretical Richardson constant for n-type SiC which is 146 $AK^{-2}cm^{-2}$. In the investigation of the effect of threading dislocation on n-type GaN Schottky diode, A.R Arehart et al. reported a modified

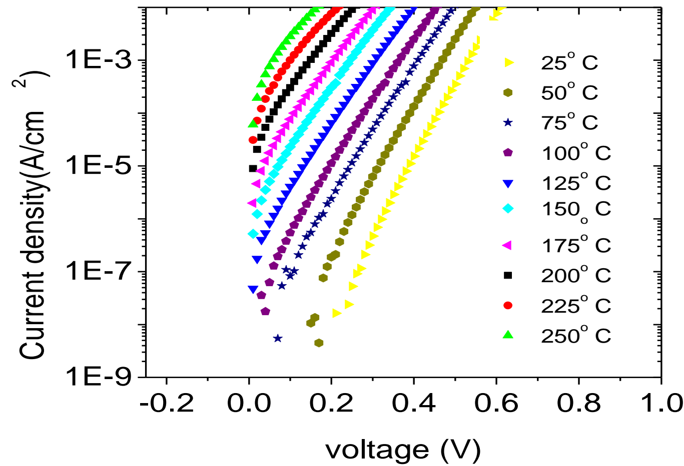

Fig. 20. Current density versus voltage plots in 25 °C increments

Richardson plot [26]. The plot between $\ln(I_s/A_eT^2)$ versus 1/nkT is called the modified Richardson plot. Fig. 23 shows the Richardson and modified Richardson plots for the CrB_2/SiC Schottky diode. Also, the Richardson constant value obtained from the modified Richardson plot did not match the theoretical Richardson constant.

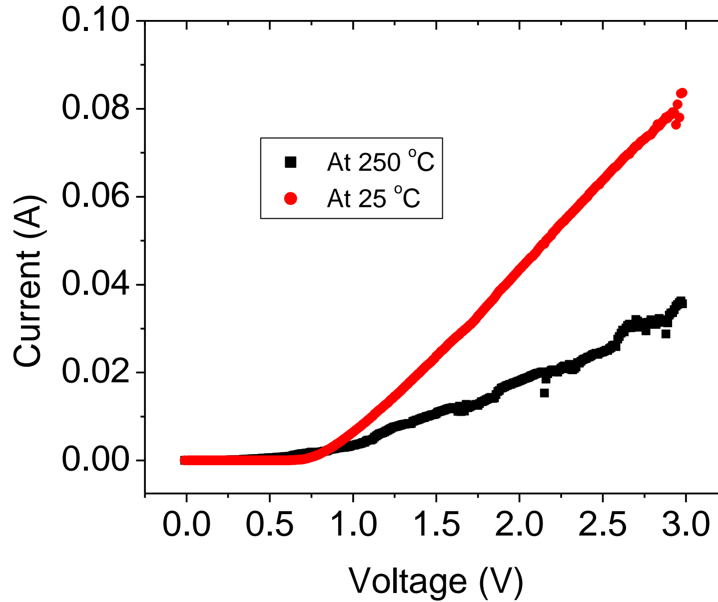

Fig. 21. I-V at measuring temperatures 25 °C and 250 °C

Table 3 shows the values of the Richardson constant and modified Richardson constant values obtained for the CrB_2/SiC Schottky contact.

Table 3. Richardson Constants obtained for CrB_2/SiC contacts

	Deposition	Measurement	Richardson constant	($AK^{-2}cm^{-2}$)
Metal	Temperature	temperature	from Richardson	from Modified
			Plot	Richardson plot
CrB_2	600 °C	25-250 °C	0.14	4925814
CrB_2	600 °C	250-25 °C	0.30	741181
CrB_2	600 °C	25-250 °C	33.78	591253

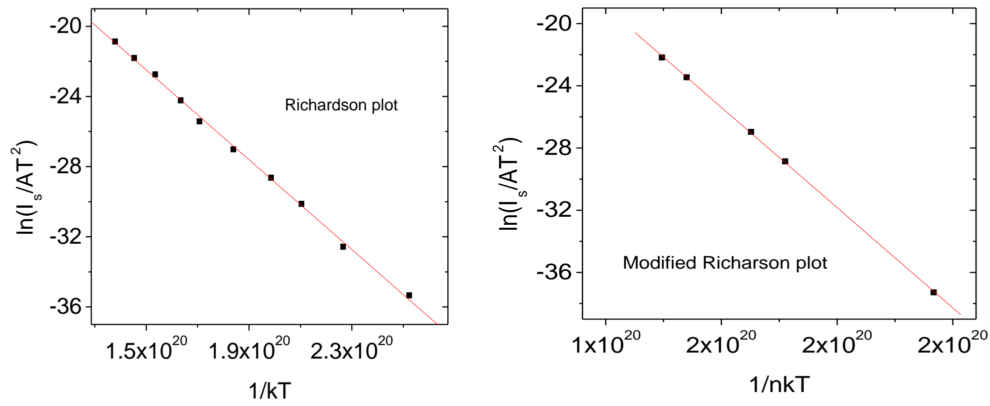

Fig. 22. (a) Richardson and (b) modified Richardson plot

The effect of ideality factor and barrier height with the temperature measurement was also studied. The plots of ideality versus temperature and barrier height versus temperature are shown in Fig. 24 and Fig. 25. From the ideality and temperature plot, it seems that the ideality is inversely proportional to the measuring temperature until 250 ^{o}C. As the temperature increased the ideality approached to unity.

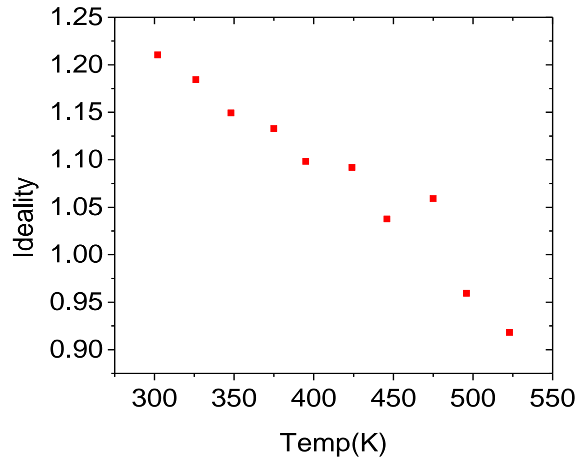

Fig. 23. Temperature versus ideality plot using IVT measurements

Based on the barrier height versus temperature plot, it seems that the barrier height is directly proportional to the measuring temperature. Along with the increase in temperature, barrier height also increased.

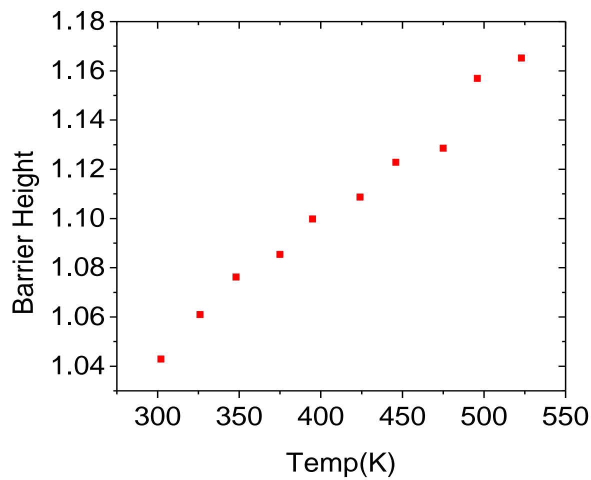

Fig. 24. Temperature versus barrier height plot using IVT measurements

Table 4. Schottky contacts deposited at 20 °C (a) measured from 25 °C to 250 °C and (b) measured back from 250 °C to 25 °C

Temp(K)	Ideality factor	Barrier Height(eV)
295	1.24	1.02
327	1.19	1.05
351	1.18	1.06
371	1.17	1.07
399	1.1	1.10
428	1.05	1.12
446	1.04	1.12
473	1.07	1.12
498	0.98	1.14
523	0.91	1.16

(a)

Temp(K)	Ideality factor	Barrier Height(eV)
523	0.91	1.16
496	0.95	1.15
475	1.05	1.12
446	1.03	1.12
424	1.09	1.10
395	1.09	1.09
375	1.13	1.08
348	1.14	1.07
326	1.18	1.06
302	1.21	1.04

(b)

Table 4 and 5 shows the vales of the ideality factors and the barrier height values for the samples deposited at 20 ^{o}C and 600 ^{o}C with the measuring temperature. The temperature measurement was from 25 ^{o}C to 250 ^{o}C and back to 25 ^{o}C. In Table 4 and 5, temperature is expressed in Kelvin.

Table 5. Schottky contacts deposited at 600 ^{o}C (a) measured from 25 ^{o}C to 250 ^{o}C (b) measured back from 250 ^{o}C to 25 ^{o}C

Temp(K)	Ideality Factor	Barrier Height (eV)
294	1.25	1.07
323	1.19	1.09
348	1.23	1.08
376	1.17	1.09
397	1.16	1.09
426	1.17	1.09
447	1.13	1.09
472	1.12	1.1
501	1.15	1.1

(a)

Temp(K)	Ideality factor	Barrier Height (eV)
473	1.75	1.52
452	1.22	1.13
427	1.21	1.13
398	1.24	1.13
376	1.27	1.11
347	1.28	1.11
328	1.3	1.1
299	1.31	1.11

(b)

CHAPTER FOUR

EFFECT OF DEPOSITION TEMPERATURE USING C-V CHARACTERIZATION

The electric field and potential distribution in the depletion region of the Schottky barrier junction depends on the barrier height, the applied voltage, and the impurity concentration. The barrier height and the doping concentration can also be determined by capacitance-voltage measurement. The capacitance-voltage technique relies on the fact that the width of a reverse-bias space charge region of a semiconductor junction device depends on applied voltage. Considering the Schottky barrier diode in Fig. 26, the semiconductor is n-type 4H-SiC with doping density N_D. A dc bias voltage is applied to the metal contact and the reverse bias produces a space charge region (scr) of width W. In Fig.26 dW is the slight increase in the scr after dc and ac biasing of the diode.

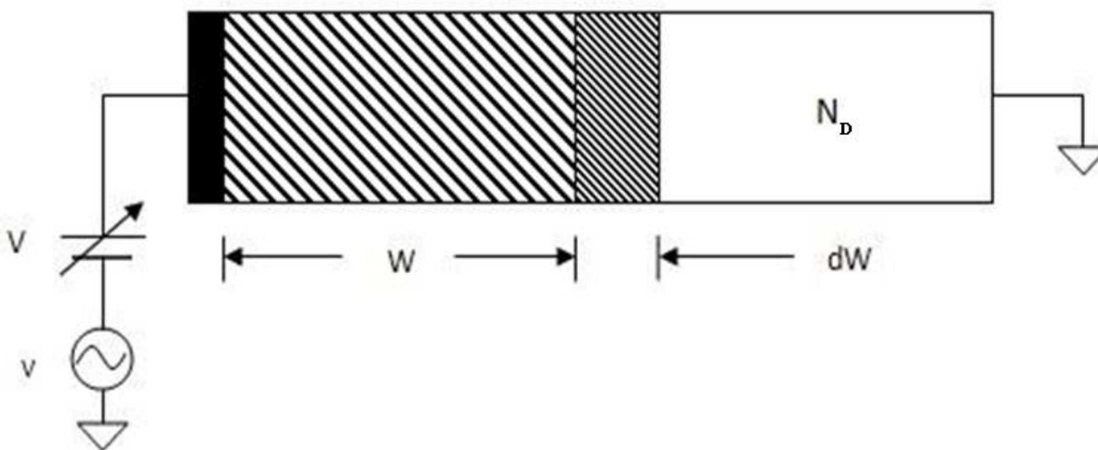

Fig. 25. Schottky diode with bias

The differential or small signal capacitance is defined by,

$$C = -\frac{dQ_s}{dV} \tag{4.1}$$

where Q_s is the semiconductor charge. The negative sign accounts for more negative charge in the semiconductor space charge region for higher positive voltage on the metal. The capacitance was determined when a small ac voltage was superimposed on a dc bias. Charges of one sign are induced on the metal surface and charges of the opposite sign on the semiconductor [27]. The voltage change affects the depletion width which is inversely proportional to the capacitance. The C-V curves are also affected by the frequency at which they are being measured. The curve for low and high frequency in the accumulation region is the same but this is not the case in the inversion region. As explained in Chapter 2, the relationship between capacitance (C) and voltage (V) is given by the Eq. 4.1,

$$C = \sqrt{\frac{q\varepsilon_o N_D}{2\left(V_{bi} - V - \frac{kT}{q}\right)}} \tag{4.2}$$

Eq. 4.1, can be written in the form,

$$\frac{1}{C^2} = \frac{2\left(V_{bi} - V - \frac{kT}{q}\right)}{q\varepsilon_o N_D} \tag{4.3}$$

The capacitance-voltage (C-V) measurements were taken on the Schottky diodes before and after the annealing where the Schottky contacts were deposited at room and

high temperature (600 ^{o}C). From the Eq. 4.3, the plot of $(A/C)^{2}$ versus the reverse-bias voltage gives a straight line graph from which the values of doping concentration (N_D) and barrier height (ϕ_B) can be determined. Fig. 27 shows the plots between C versus V and $1/C^2$ versus V for a Schottky diode made with one of the refractory metal boride as the Schottky contact. For uniformity doped materials, $1/C^2$-V data was linear whereas C-V data is not as linear as $1/C^2$-V data.

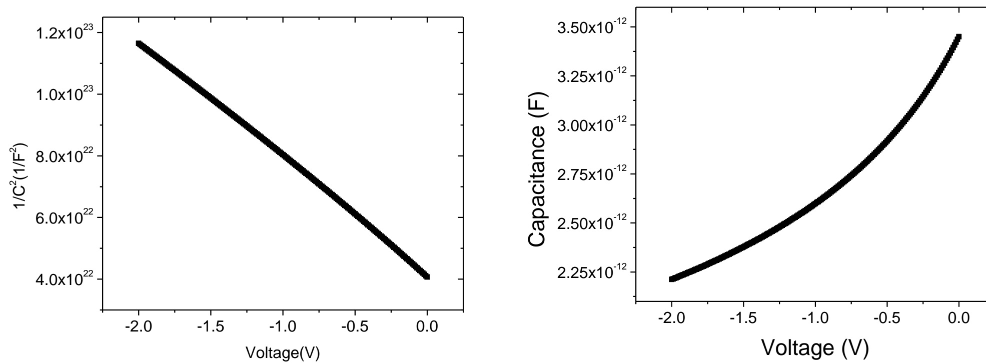

Fig. 26. (a) $1/C^2$ versus V and (b) C versus V.

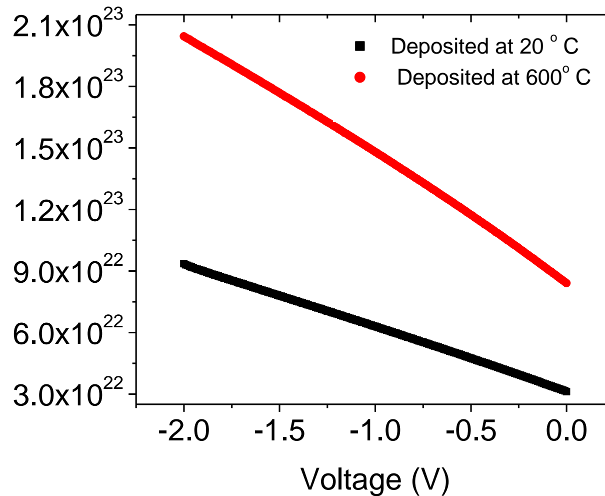

Fig. 27. $1/C^2$-V plots of diodes with W_2B contact deposited at 20 ^{o}C and 600 ^{o}C

Fig. 28 shows the $1/C^2$-V graphs for the Schottky diodes which were deposited at room and high temperature. Appendices 3 and 4 show the steps to find the barrier height and doping concentration of the Schottky diodes from the slope and intercept of the plot.

4.1 Testing Method for C-V Characterization

The reverse bias C-V characterization was taken with the help of the Agilent precision LCR meter model E4980A. The Agilent LCR meter was connected to a PC which was running LabView by using a GPIB cable. For each negative voltage applied, a corresponding capacitance measurement through the diode was taken. The LCR meter has four probes. Two of these probes are named as 'high' and connected together. The other two probes are named as 'low' and also connected together. The SiC sample was mounted on the copper plate with silver paste and C-V measurements were taken. All the circular Schottky contacts were tested with a single needle probe attached to the high terminals of the Agilent precision LCR meter with the copper substrate attached to the low terminals. Capacitance-voltage measurements are very sensitive to noise and light means capacitance measurement was not linear if the samples were not measured with in an isolated container. So, all the measurements were done by covering the sample and the single needle probe in an isolated container as shown in Fig. 29. The C-V measurements were performed by superimposing a small alternative voltage of 10 mV at 1 MHz on the reverse dc bias and the capacitance was recorded when the voltage was changed from -5 V to 0 V. Different circular Schottky contacts were selected for each measurement. Five Schottky diodes were characterized for each sample. Fig. 29 shows the setup for the C-V measurements and the samples on the copper plate.

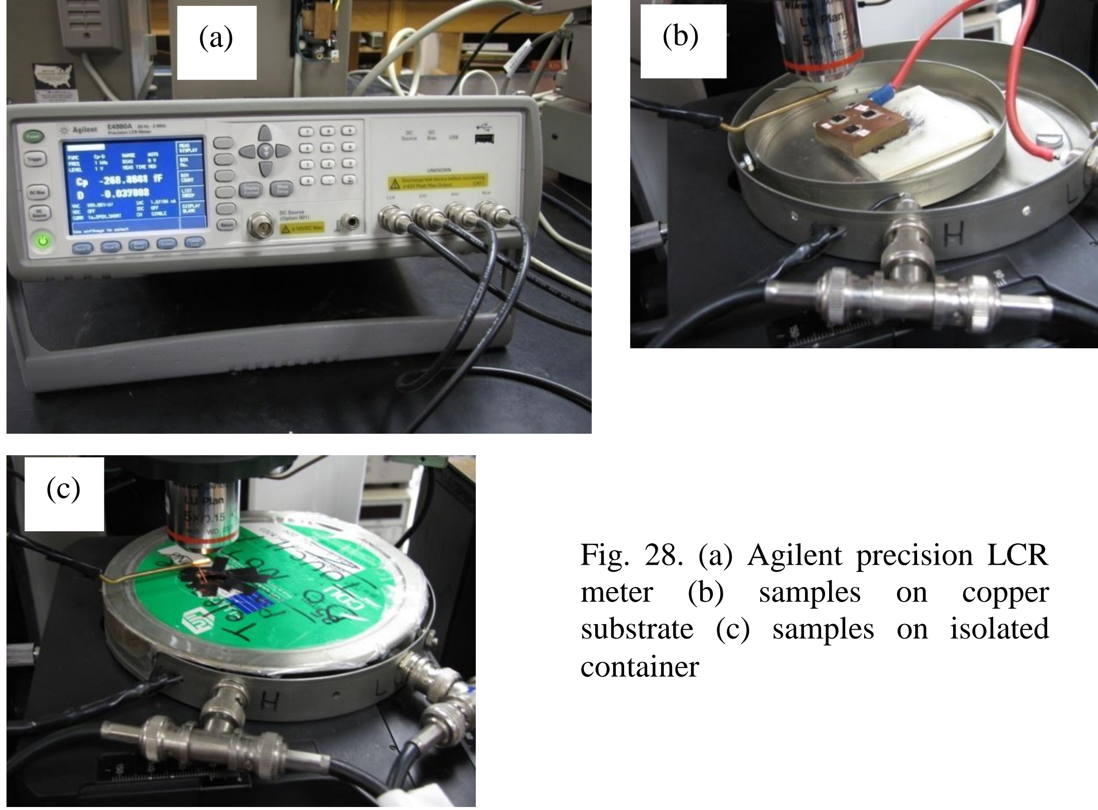

Fig. 28. (a) Agilent precision LCR meter (b) samples on copper substrate (c) samples on isolated container

By plotting $(A/C)^2$ versus the reverse bias voltage V, a straight line was obtained whose slope is $2/q\varepsilon_0 N_D$ and the intercept on the V-axis is $V_i = -V_{bi}+kT/q$. From the relation of the Schottky barrier height (SBH) and the built-in potential, we obtain

$$\Phi_B = V_i + \left(\frac{kT}{q}\right)\left[1 + \ln\left(\frac{N_O}{N_D}\right)\right] \tag{4.4}$$

and the value $N_o = 1.69\times10^{19}$ cm^{-3} was used for the effective density of state for 4H-SiC [7]. The C-V plots of sputter-deposited Schottky contacts of all refractory metal borides at room and high temperatures are shown in Fig. 28. The Schottky diodes were tested using the C-V method and the capacitance measurements were recorded. The measurements were done on each Schottky diode before and after being annealed in RTP at 600 ^{o}C for 20 minutes using single needlepoint probes. After recording the capacitance

and voltage, the quality of the diode junction was investigated by examining the doping concentration and barrier height. Five different sets of Schottky diodes for each contact were chosen for analysis and the average of the values was used for the barrier height and doping concentration.

Another plot of $(A/C)^2$ versus V of non annealed W_2B/SiC diodes is shown in Fig. 30 and from this, a barrier height of 1.28 eV was obtained. This is larger than the value of 1.03 eV obtained from the I-V measurements. The difference in the values of the SBH could be a result of factors such as image force lowering and in homogeneities at the metal/SiC interface [7]. The average value of N_D obtained from this plot was 1.2×10^{16} cm^{-3}, which is close to 1×10^{16} cm^{-3}, the value specified by Cree, Inc., for this wafer.

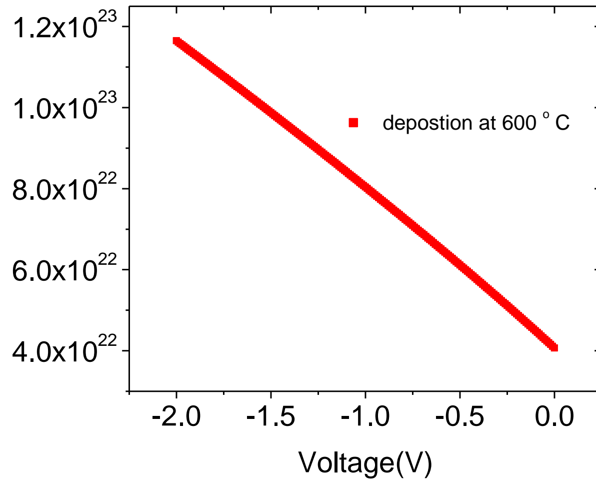

Fig. 29. C-V Plot for W_2B/SiC deposited at 600 ^oC

4.2 Sheet Resistance Measurements

Sheet resistance of each of the boride films was obtained by using four-point probe measurements. Fig. 31 shows the set up for four probe measurements. Fig. 32 shows a microscopic view of the four probes. In the four-point probe measurement, current was sourced through two probes and the resulting voltage was measured across the other two probes positioned in the middle as shown in Fig. 33. Keithley source meter was used to measure the voltage. For improved accuracy, the spacing (s) between all the probes must be equal. The sheet resistance (R_{sheet}) was then obtained by dividing the voltage with the current.

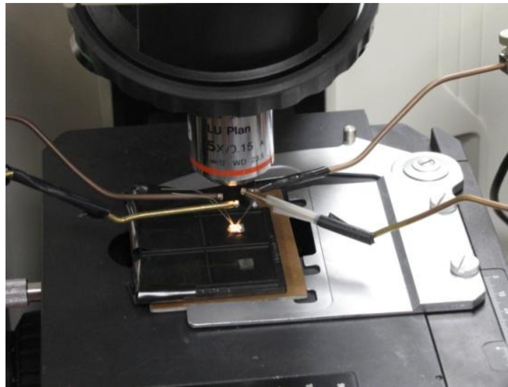

Fig. 30. Four point-point probe measurement setup

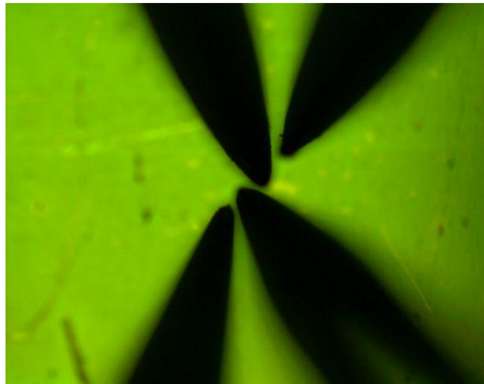

Fig. 31. Microscopic view of the four-point probes

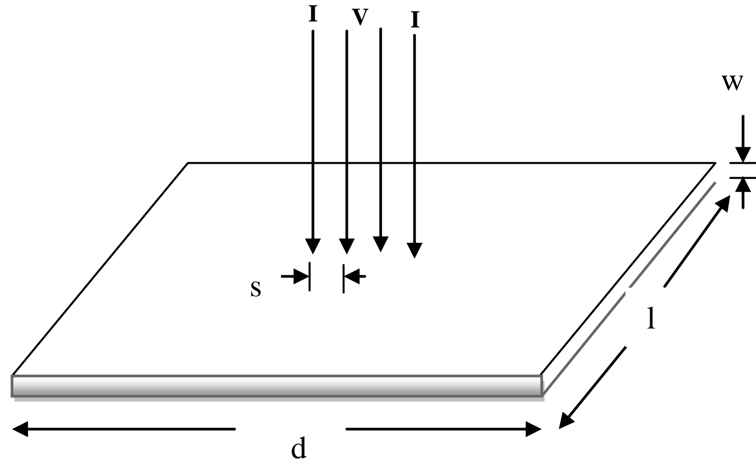

Fig. 32. Set up of four-probes on the film

The conductivity of a diode (sample) depends upon the number of free carriers and their mobility or the ease with which they move through the diode (sample). If the resistivity of the material (film) is known, the resistance of the film can be determined from Eq. 4.5.

$$R = \rho l/A \tag{4.5}$$

where R = Resistance of the material.

l = Length of the film.

A = Cross-sectional area of the film.

Area of the film is height (l) × width (w). So the resistance of the film is given by the Eq. 4.5,

$$R = \rho l/wl = \rho/w \tag{4.6}$$

The resistance of the film is related to the applied voltage (V) and the current flow (I) by Eq. 4.7,

$$R = \frac{V}{I} \tag{4.7}$$

Because of the geometry of the sample and the measurement dimensions, a correction factor is often required for the value of the sheet resistance, which can be written as shown in Eqn. 4.8 [28].

$$R_{sheet} = (V/I) \times CF \tag{4.8}$$

where CF = correction Factor = 4.54

Eq. 4.8 is valid when

1. Thickness of the film is much less than the spacing between the probes.
2. The size of the sample is much greater in length and width than the probe spacing.

Table 6 shows the sheet resistance values obtained for the films deposited at room and high temperature.

Table 6. Sheet resistance of the film deposited at 20 ^{o}C and 600 ^{o}C

METAL	Deposition TEMP	R_s(Ohm)
W_2B_5	600C	60.89
	20C	18.48
W_2B	600C	96.57
	20C	189
WB	600C	1851
	20C	29995
CrB_2	600C	446
	20C	2387.4
HfB_2	600C	573.25

CHAPTER FIVE

DICUSSION ON THE RESULTS

This research concerned studies of Schottky barrier diodes fabricated using refractory metal borides. The Schottky contacts were fabricated using refractory metal borides. Comparison was made between the diodes with the Schottky contacts deposited at 20 °C (room temperature) and at 600 °C (high temperature). The diodes with the contacts deposited at high temperature exhibited better electrical properties as indicate by

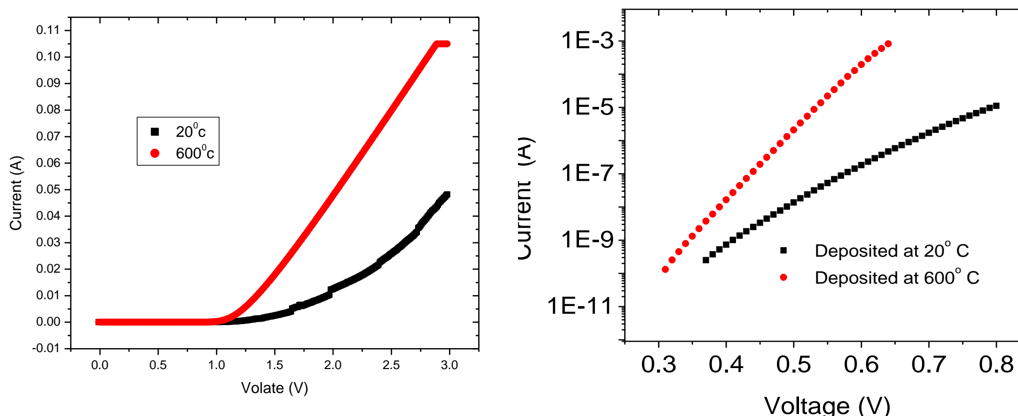

Fig. 33. Current-Voltage plots for diodes with the contacts deposited at 20 °C and 600 °C showing (a) the linear I-V plots and (b) the linear portions of the semilog I-V plots.

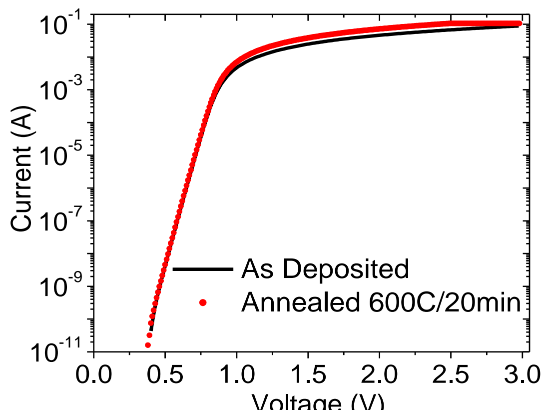

Fig. 34. Current-Voltage plots for WB diodes with the contacts deposited at 600 °C showing no change even following annealing in N_2 at 600 °C/20 min.

Fig. 34 and 35. In Fig. 34 (a), the I-V characteristics show a clear difference between the two diodes. Diodes with the boride contacts deposited at room temperature has a larger turn-on voltage under positive bias and shows a higher resistance compared to the diodes with the contacts deposited at high temperature. In Fig. 34 (b), the linear portions of the semilog plots show a clear difference. At first glance, the plot appears more linear for the contact which was deposited at high temperature. Using appropriate equations, the saturation current and ideality factors at each temperature were extracted from the linear regions of the curves. The Schottky contact which was deposited at high temperature had a linear region of approximately six decades. Contacts deposited at high temperature have steeper slope compared to the contacts deposited at room temperature, which indicates smaller ideality factors. In Fig. 35, the diodes with the contacts deposited at 600 ^{o}C show very little or no change even after annealing for a long time.

Table 7 shows a summary of results of the values of ideality factor (n), the leakage current density (J) at -15V, and the on-resistance obtained from the current-voltage measurements, the barrier heights (ϕ_B) obtained from the current-voltage and capacitance-voltage measurements. These values were average values obtained from measurements taken on at least five diodes with standard deviations ranging from 1% to 4% of the mean values. In Table 7, values outside the parentheses were obtained for the diodes deposited at room and high temperature. The values inside the parenthesis were obtained after the diodes annealed in RTP. N/G means data is not good enough for obtaining these values and N/A means data is not available. From Table 6, it was clear that the room temperature deposition did not yield good values for the ideality and barrier height. After annealing, the diodes with the Schottky contacts deposited at 20 ^{o}C showed

moderately improved electrical properties as evidenced by a reduction in the ideality factors as showed in Table 7.

Table 7. Summary of the results. (Values outside the bracket are for diodes with as-deposited boride contacts and those inside the brackets are obtained after the diodes were annealed inN2 using RTP at 600 °C/20 min).

Schottky Contact	**Substrate Temp(°C)**	**Ideality Factor**	**SBH (eV) using IV**	**SBH (eV) using CV**	**J at -15 V ($x10^{-7}$ A/cm^2)**	**R_{on} (mΩ-cm^2)**
W_2B_5	20	1.28(1.17)	1.20(1.28)	1.44(1.55)	-5.29(N/A)	5.77(6.00)
	600	1.09(1.11)	1.11(1.08)	1.35(1.35)	-4.19(N/A)	6.36(3.26)
WB	20	N/G(1.31)	N/G(1.15)	N/G(1.55)	-6.24(-6.11)	N/G(18.7)
	600	1.07(1.06)	1.15(1.16)	1.54(1.42)	-4.70(-5.33)	3.87(4.29)
W_2B	20	N/G(1.20)	N/G(1.57)	N/G(1.83)	-3.25(-8.08)	N/G(6.17)
	600	1.05(1.04)	1.03(1.02)	1.28(1.20)	-4.87(-7.68)	3.61(3.70)
HfB_2	20	1.12(1.10)	1.01(0.94)	N/A(1.22)	-3.64(-3.16)	34.0(41.2)
	600	1.07(1.09)	1.10(1.08)	N/A(1.32)	-4.13(-3.84)	7.58(6.95)
CrB_2	20	1.35(N/A)	1.08(N/A)	N/A	-17.0(N/G)	71.2(66.0)
	600	1.12(N/A)	1.12(N/A)	N/A	-12.0(N/G)	22.2(56.0)
TiB_2	20	4.80(1.34)	0.87(0.90)	1.12(1.34)	-44.8(-11.1)	17.2(29.3)
	600	1.10(1.11)	0.94(0.92)	1.19(N/A)	-9.60(-6.22)	19.0(28.3)

The barrier heights obtained from the I-V and C-V measurements have higher values compared to the values obtained from the room temperature deposition. For most of the refractory metal borides, reverse leakage current was much smaller for the metal deposited at high temperature compared to the metal deposited at room temperature.

Based on all values of the Schottky diodes it is clear that high temperature deposition yields better electrical properties than those with the contacts deposited at room temperature. Characteristics such as ideality factor and the Schottky barrier height of the Schottky diode remain unchanged significantly after annealing for 20 min with RTP. As seen in the log plot of current versus voltage, it is clear that the annealing did not change the slope and intercept of the line. From the graph and analysis, 600 ^{o}C depositions and 600 ^{o}C annealing gave good electrical properties and good thermally stable diodes.

From the RBS spectra, oxygen is removed from the boride/SiC interface when the borides are deposited at 600 ^{o}C. The removal of a significant amount of O_2 from the boride/SiC interface could occur by escape of oxides such as B_2O_3 and H_3BO_3 known to be volatile at 300 ^{o}C [23]. Since the presence of impurities such as oxygen at the interfaces is known to contribute to undesirable electrical characteristics, the improvement in the barrier properties of the boride/SiC contacts is possibly due to the escape of oxygen from the boride/SiC interface.

CHAPTER SIX

CONCLUSION AND RECOMMENDATION FOR FUTURE WORK

6.1 Conclusion on Temperature Deposition

From Tables 6 and 7, the Schottky contacts deposited at high temperature have better electrical and thermal properties compared to the Schottky contacts deposited at room temperature. The contacts deposited at 600 ^oC have smaller ideality factor values and an average barrier height as large as 1.15 eV compared to the contact deposited at room temperature. This implies that the deposition at higher temperature in Schottky barrier diodes have superior electrical quality than those contacts deposited at 20 ^oC. In addition, the ideality factor and SBH of the diodes with the Schottky contacts deposited at 600 ^oC remain unchanged after annealing at 600 ^oC/20 min using RTP, implying excellent thermal stability of the diodes.

The diodes with Schottky contacts deposited at 20 ^oC show moderately improved electrical properties after annealing in RTP, as evidenced by a reduction in the ideality factors. The leakage current densities determined at -15V were, in general, smaller for the diodes with contacts deposited at 600 ^oC compared to the contacts deposited at 20° C, and several of these values were less than 5×10^{-7} A/cm^2 even after the RTP annealing. The specific on-resistance values were similarly smaller for diodes with contacts deposited at 600 ^oC (many less than 10 mΩ-cm^2) than for those contacts deposited at 20 ^oC. Diodes with the combination of smaller average ideality factor (1.07), larger average SBH (1.15 eV), smaller average reverse-bias leakage current density (4.70×10^{-7} A/cm^2), and smaller

specific on-resistance (3.87 mΩ-cm^2) were obtained from the WB contacts deposited on SiC held at 600 ^{o}C [7]. These improvements in the electrical properties and thermal stability of our boride/SiC Schottky contacts will further improve the performance of 4*H*-SiC Schottky diodes for high power and high temperature applications.

6.2 Recommendation for Future Studies

In future, work needs to be performed on I-V-T measurements on all the Schottky diodes to find out the dominant transport mechanism, Richardson constant (A^*) from the Richardson plot and modified Richardson plot. The Richardson constants obtained needs to be compared with the theoretical Richardson constant which is 146 AK^{-2}cm^{-2} for n-type SiC. It is further necessary to find how the ideality factor and the barrier height depend on the measuring temperature for the rest of the boride Schottky contacts. Finally, the dominant transport mechanism should be investigated. This is found by plotting ideality (n_{00}) versus temperature and by comparing the Eq. 6.1, characteristic energy, E_{00} can be estimated [26].

$$n_{00} = \left(\frac{E_{00}}{kT}\right)\cosh\left(\frac{E_{00}}{kT}\right) \tag{6.1}$$

Future studies need to investigate how the deposition temperature affects the current conduction mechanism. RBS analysis is needed to be performed on all the unpatterned samples.

APPENDICES

Appendix 1: Calculation of Ideality Factor and Barrier Height for the Contacts Deposited at Room Temperature using I-V Method.

Slope and intercept were found from the linear fit of the data at smaller voltages. From the slope and intercept of the I-V graph, barrier height and ideality factor can be determined. Eq. 3.1 is used to find the ideality factor and the barrier height of the Schottky diode. Fig. 36 shows W_2B_5 contact deposited at 20 ^oC. All the values are analyzed in origin-pro.

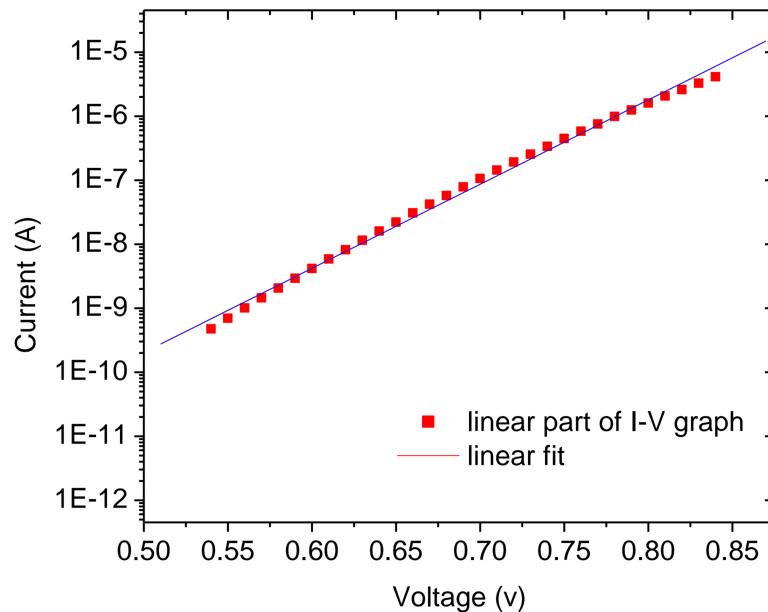

Fig. 35. W_2B_5 contact deposited at 20 ^oC

From the linear fit, the slope is 30.82 and the intercept is -37.46 and the radius of the particular diode is 0.0095 cm.

Ideality factor, $n = \frac{q}{kT} \times \frac{1}{slope}$

$= (1.6\times 10^{-19}$ coulombs$) / (1.38 \times 10^{-23}$ j/K$\times$300K$\times$30.28)

= 1.28

Barrier Height, $\Phi_B = \frac{kT}{q}\left(\ln(AA^{*}T^{2}) - \text{intercept}\right)$

$=((1.3\times10^{-23}\times300)/ (1.6 \times 10^{-19})(\ln(2.83\times10^{-4}cm2\times146cm^{-2}k^{-2}\times300^{2}k^{2})+37.26)$

= 1.18 eV.

Appendix 2: Calculation of Ideality Factor and Barrier Height for the Contacts Deposited at High Temperature using I-V Method.

Fig. 37 shows the linear fit for the W_2B_5 contact deposited at 600 ^oC. Analysis of the graph was done in origin-pro.

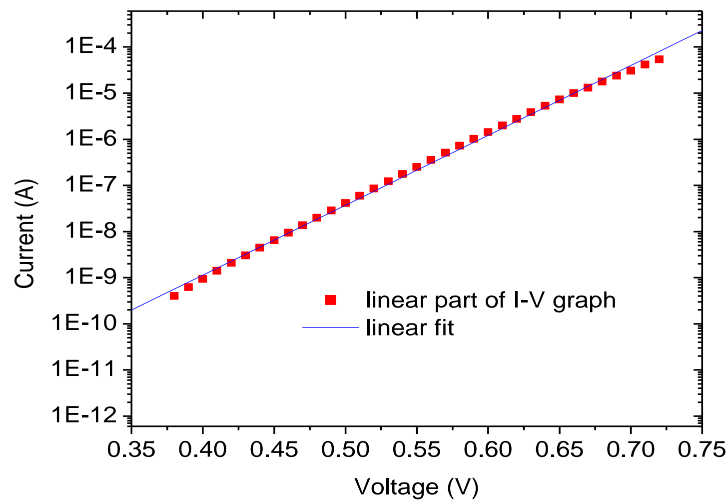

Fig. 36. W_2B_5 contact deposited at 600 ^oC

Slope and intercept of Fig. 40 are 34.88 and -34.549 in log scale. The radius of the diode is 0.0085 cm and the shape of the diode is circular.

Ideality factor, $n = \frac{q}{kT} \times \frac{1}{slope}$

$$=1/\ (0.02585 \times \text{slope})$$

$$= 1.10$$

Barrier Height, $\Phi_B = \frac{kT}{q}\left(\ln(AA^{*}T^{2}) - \text{intercept}\right)$

$$=0.02585((\ln (2981.0061) +34.549)$$

$$= 1.09 \text{ eV.}$$

Calculation of ideality factor and the barrier height of the diodes which were annealed at 600 ^{o}C in pure N_2 with RTP are same as above.

Appendix 3: Calculation of the Barrier Height and Doping Concentration for the Contacts Deposited at Room Temperature using C-V Method.

Barrier height and doping concentration can be determined from the slope and intercept of the C-V graph. Eq. 4.2 is used to find the ideality factor and the barrier height of the Schottky diode. Fig. 38 shows the linear fit for the WB contact deposited at 20 ^{o}C.

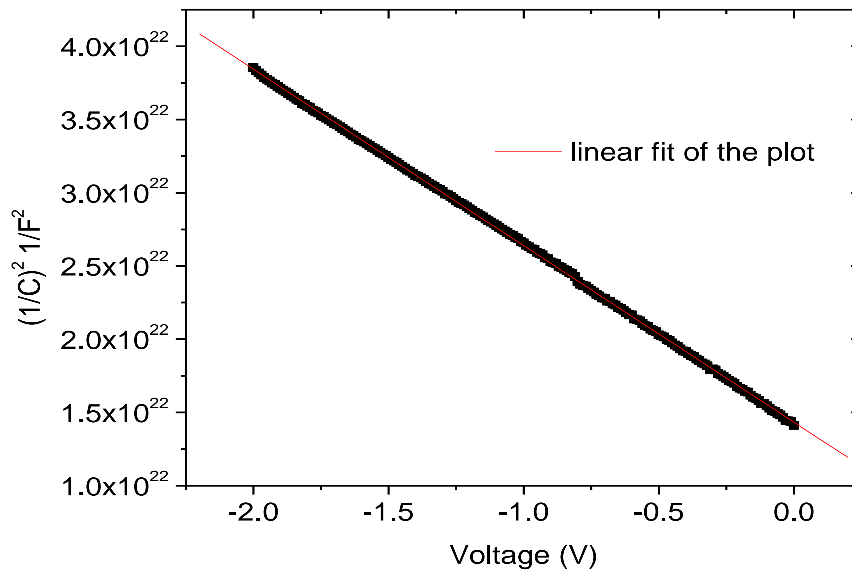

Fig. 38. WB contact deposited at 20 ^{o}C

Slope and intercept of Fig. 38 are -1.20E22 and 1.43E22 and the radius of the diode is 0.0095cm. A new slope can be found by multiplying area^2 of the diode with the slope.

New slope = 8.03071E-8×-1.20499E22

=-9.63685E14

X-intercept = - (intercept/slope)

$= 1.43E22/1.20E22 = 1.19167$

Doping Concentration, $N_D = \frac{-2}{(newslope \times q \times k_s \varepsilon_0)}$

$=-2/ (-9.63685 \times 1.6 \times 9.7 \times 8.85 \times 10^{-19})$

$=1.51 \times 10^{16}$

Barrier Height, $\Phi_b = X - Intercept + \left(\frac{kT}{q}\right)\left[1 + \ln\left(\frac{N_O}{N_D}\right)\right]$

$= 1.19 + (3 \times 1.38)/ (1.6 \times 10^{-2}) \ln [1 + (1.69 \times 10^{19}/ 1.51 \times 10^{16})]$

$= 1.39$ eV.

Appendix 4: Calculation of the Barrier Height and Doping Concentration for the Contacts Deposited at High Temperature using C-V Method.

Fig. 39 shows the linear fit for the W_2B contact deposited at 600 ^oC.

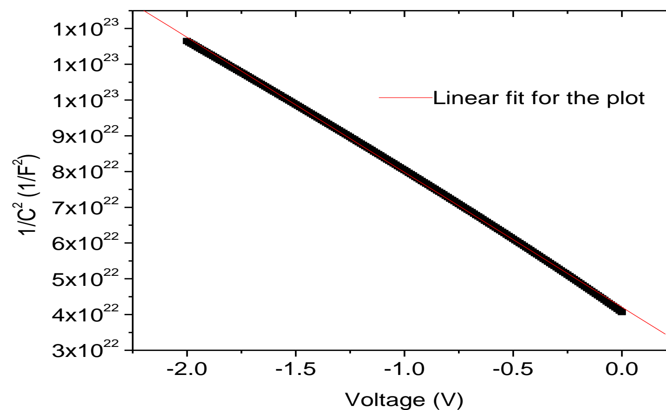

Fig. 39. W_2B contact deposited at 20 ^oC

Plot was analyzed using origin-pro. Slope and intercept of Fig. 39 are -3.77284E22 and 4.20737E22 and the radius of the diode is 0.075cm. New slope can be found by multiplying area^2 of the diode with the slope.

New slope = 3.11964E-8×-3.77284E22

=-1.1761E15

X-intercept = - (intercept/slope)

= 4.20737E22 / 3.77284E22 = 1.11406

Doping Concentration, $N_D = \frac{-2}{(newslope \times q \times k_s \varepsilon_0)}$

$=-2/(-1.1761E15 \times 1.6 \times 9.7 \times 8.85 \times 10^{-19})$

$=1.24 \times 10^{16}$

Barrier Height, $\Phi_b = X - Intercept + \left(\frac{kT}{q}\right)\left[1 + \ln\left(\frac{N_O}{N_D}\right)\right]$

$= 1.11406 + (3 \times 1.38)/(1.6 \times 10^{-2}) \ln [1 + (1.69 \times 10^{19}/ 1.24 \times 10^{16})]$

= 1.326 eV.

Calculation of the doping concentration and the barrier height of the diodes which were annealed at 600°C in pure N_2 with RTP are same as above.

Appendix 5: Calculation of the Current Density for the Contacts Deposited at Room Temperature.

For the WB contacts current at -20 is -0. 1864E-9 A, and the radius of the diode is 0.00785 cm.

Current Density, $J = \frac{I}{A}$

= - 0. 1864E-9/0.000193495

= -9.63E-07 A/cm^2.

Appendix 6: Calculation of the Current Density for the Contacts Deposited at High Temperature.

For the WB contacts current at -20 is -1.05E-10 A, and the radius of the diode is 0.0075 cm.

Current Density, $J = \frac{I}{A}$

= - 1.05E-10/0.000176625

= -5.95E-07 A/cm^2.

Appendix 7: Calculation of the Series Resistance after Annealing at 600 ^{o}C for the Contacts Deposited Room Temperature.

After recording the current-voltage, we need to find the derivative of voltage and derivative of logarithmic current. After finding those values, we need to plot the current versus dV/d[ln(I)]. Fig. 40 shows the linear fit for the series resistance plot, for the W_2B contacts after annealing with RTP where the contact was deposited at 20 ^{o}C.

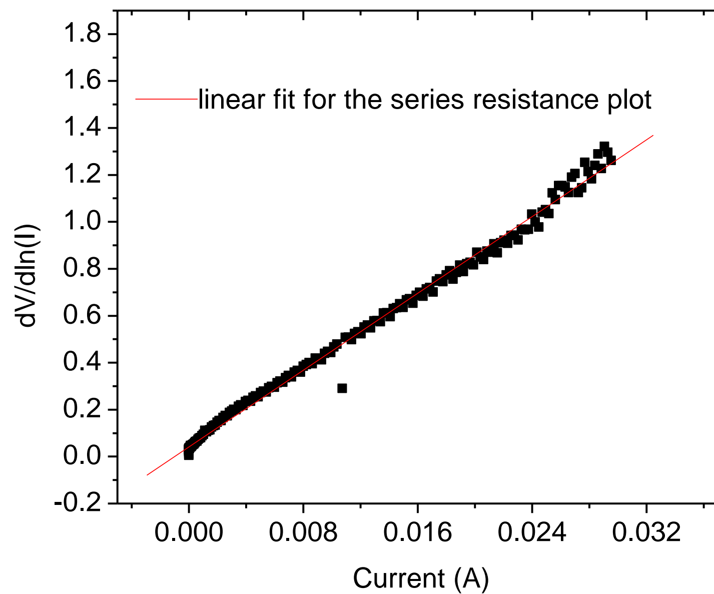

Fig. 37. W_2B contacts after annealing where the contact was deposited at 20 ^{o}C.

From Fig. 40, intercept of the graph is the series resistance. If we multiply the series resistance with the area of the diode we will get on- resistance.

Series resistance = 40.09

On-resistance = area of the diode× series resistance

$$= 1.77\times10^{-4}\times 40.09 = 7.03 \times10^{-3}\Omega\text{-cm}^2.$$

Appendix 8: Calculation of the Series Resistance for the Contacts Deposited at 600 ^{o}C.

Fig. 41 shows the linear plot of the series resistance plot for the W_2B contact deposited at 600 ^{o}C. Plotting series resistance is same as Appendix 7.

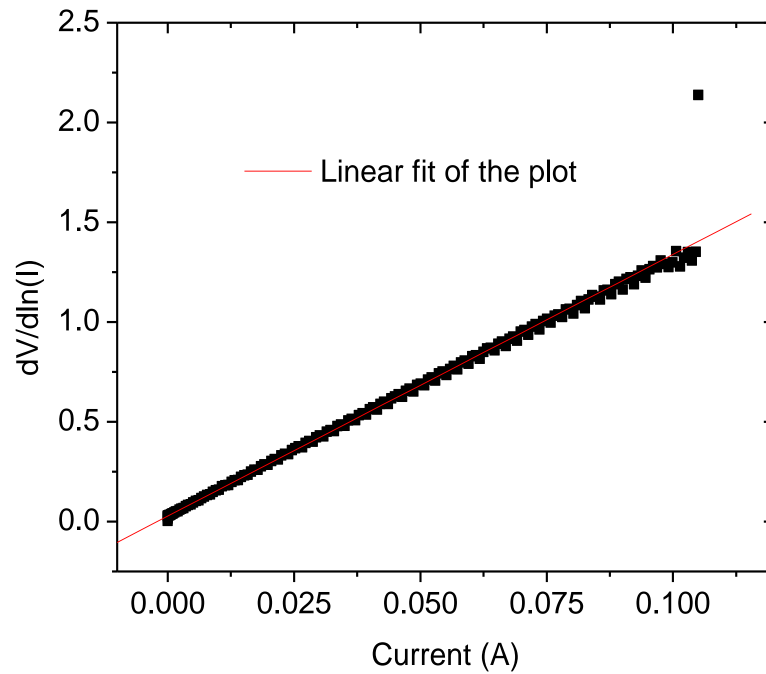

Fig. 38. W_2B contact deposited at 600 ^{o}C

From the liner fit, Intercept or series resistance = 13.12Ω

On- resistance = area of the diode × series resistance

$= 2.83\times10^{-4} \times 13.12$

$= 3.72\times10^{-3}\Omega\text{-cm}^2$.

REFERENCES

[1] SiC'08 *"The power electronics next electronics,"* accessed from http://www.yole.fr/pagesAn/products/Report_sample/SiC_silicon_carbide_compound_materia l_market_report.pdf, retrieved September 21, 2009.

[2] A. El Fatimy, S. Boubanga Tombet, F. Teppe, W. Knap, D.B. Veksler, S. Rumyantsev, M.S. Shur, N. Pala, R. Gaska, Q. Fareed, X. Hu, D. Seliuta, G. Valusis, C. Gaquiere, D. Theron and A. Cappy, "*Terahertz detection by GaN/AlGaN transistors,*" Electronic Letters, vol. **42**, no. 23, pp. 1342-1344,2006.

[3] J.J. Chang, T. Nozokido, C. M. mann, T. Suzuki, and K. Mizuni, *"Development of Schottky barrier diodes for the submillimeter wave region,"* RIKEN Review no. 11 Dec. 1995 Focused on the Frontiers of Photo dynamics Research. Accessed from, http://www.riken.go.jp/lab-www/library/publication/review/pdf/No_11/11_009.pdf, retrieved on September 22, 2009.

[4] L. M. Tolbert, B. Ozpineci, S. K. Islam, F. Z. Peng *"Impact of SiC power electronic devices for hybrid electric vehicles,"* accessed from http://www.ornl.gov/~webworks/ cppr/y2001/pres/113883.pdf , retrieved October 25, 2009.

[5] T. N. Oder*, "Fabrication and characterization of ohmic contacts to p- and n-type silicon carbide with applications to p-n junction diodes,"* PhD dissertation, Auburn University, Auburn, AL, 1999.

[6] J. B Casady and R. W. Johnson, *"Status of SiC as a wideband gap semiconductor for high temperature applications,"* Solid State Electronics, vol. **39**, no. 10, pp. 1409-1422, 1996.

[7] T. N. Oder, E. Sutphin, and R. Kummari *"Ideal SiC Schottky barrier diodes fabricated using refractory metal borides,"* J. Vac. Sci. Technol. B, vol. **27**, no. 4, pp. 1865-1869, 2009.

[8] S. M. Sze, *"Physics of Semiconductor Devices*," 2nd ed, John Wiley & Sons, New York, 1981.

[9] G.L. Harris, *"Properties of Silicon Carbide,"* EMIS Data Review Series 13, INSPECT, London, 1995.

[10] P. G. Neudeck, "*Progress in silicon carbide semiconductor electronics technology,"* J.Electronic Materials, vol. **24**, no.4, pp. 283-288, 1995.

[11] D. Pelletier, D. Gervais, & C. Pomot, *"Application of wide-gap semiconductors to surface ionization: work functions of AIN and SiC single crystals,"* J. Appl, Phys., vol. **55**, no. 4, pp. 994-1002, 1984.

[12] A. Agarwal, R. Singh, S. H. Ryu, J. Richmond, C. Capell, S. Schwab,B. Moore, and J. Palmour, *"600 V, 1–40 A, Schottky diodes in SiC and their applications,"* from http://www.cree.com/products/pdf/PWRTechnicalPaper1.pdf , retrieved November 30, 2009.

[13] R. A. Cutler, *"Engineered materials handbook,"* ceramics and glasses, ASM International, vol. **4**, 1991.

[14] I.E. Campbell and E.M Sherwood, *"High temperature materials and technology,"* John Wiley & Sons Inc, New York, 1967.

[15] "Chapter 3: Metal Semiconductor Junctions" Retrieved: February 15, 2009 Copyright 2004 B. Van Zeghbroeck http://ece-ww.colorado.edu/~bart/book/book/chapter3/ch3_3.htm.

[16] Ben G Streetman, *"Solid State Electronic Devices,"* 3rd Edition, Prentice hall series, 1990.

[17] B.L Sharma, *"Metal –Semiconductor Schottky Barrier Junctions and Their Applications,"* Plenum press, New York, 1984.

[18] M. Siad, C. Pineda Vargas, M. Nkosi, D. Saidi, N. Souami, N. Daas, and A.C. Chami. "*Characterization of Ni and Ni/Ti contact on n-type 4H-SiC,*" Appl Surf Sci., vol. **256**, no. 1, pp. 256-260, 2009.

[19] T. N. Oder, P. Martin, A. V. Adedeji, T. Isaacs-Smith, and J. R. Williams, *"Improved Schottky contacts on n-Type 4H-SiC using* ZrB_2 *deposited at high temperatures,"* J. Electron. Mater., vol. **36**, pp. 805-810, 2007.

[20] V. W. L. Chin, M. A. Green and J. W. V. Storey, *"Correlation between current-voltage and capacitance-voltage Schottky barrier height on (100) and (110) GaAs and (110) InP surfaces,"* J. Appl. Phys. Vol. **68**, pp. 3470, 1990.

[21] H. Sheng, S. Muthukumar, N. W. Emanetoglu and Y. Lu, *"Schottky diode with Ag on* $(11\bar{2}0)$ *epitaxial ZnO film,"* Appl. Phys. Lett. Vol. **80**, pp. 2132, 2002.

[22] T.N. Oder, J.R. Williams, M.J. Bozack, V. Iyer, S.E. Mohney, and J. Crofton, *"High temperature stability of chromium boride ohmic contacts to p-type 6H-SiC,"* J. Electron. Mater. **27**, pp. 324-329, 1998.

[23] R.J. Irving and I.G. Worsley, *"The oxidation of titanium diboride and zirconium diboride at high temperatures,"* J. Less Common Met., vol. **16**, pp. 103- 112, 1968.

[24] J.R. Shappirio, J.J. Finnegan, R.A. Lux, and D.C. Fox, *"Resistivity, oxidation kinetics and diffusion barrier properties of thin film* ZrB_2*,"* Thin Solid Films, vol. **119**, pp. 23-30, 1984.

[25] T. N. Oder. R. Williams, M. J. Bozack, V. Iyer, S. E. Mohney, and J.Crofton, *"Refractory metal boride ohmic contacts to p-type 6H-SiC,"* J. Electron. Mater., vol. **27**, no. 1, pp. 12-18, 1998.

[26] A.R Arehart, B Moran, J S. Speck, U K. Mishra, S P. DenBaars, and S A. Ringel, *"Effect of Threading Dislocation Density on Ni/n-GaN Schottky Diode I-V Characteristics,"* J. Appl. Phys., vol. **100**, no. 2, pp. 1-10,2006.

[27] Dieter K. Schroder, *"Semiconductor Material and Device Characterization,"* John Wiley & Sons, Inc., New York, 1998.

[28] Fairchild Corporation, *"Semiconductor & integrated circuit fabrication techniques,"* Reston publication company, Inc., Virginia, 1979.