BINARY LOGIC TUTORS FOR TRAINING INDUSTRIAL ELECTRICAL TECHNICIANS

by

Alfred W. Vahey

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Dean of the Graduate School Date

YOUNGSTOWN STATE UNIVERSITY

ABSTRACT

BINARY LOGIC TUTORS FOR TRAINING

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This thesis represents the results of obtaining and building tutoral equipment, and developing a series of experiments that can be performed on this equipment to adequately train industrial electrical maintenance technicians in the basics of logic circuitry through a "hands on" approach to understanding.

Although this type of tutoral equipment is becoming more economically available on the market in recent years, there is little available information aimed at practical laboratory reinforcement in this area for industrial electrical technicians.

ACKNOWLEDGEMENTS

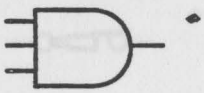
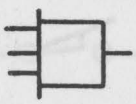
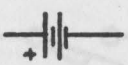
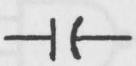
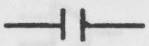
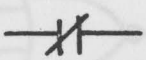
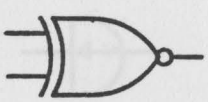
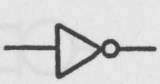
My love has deepened for my family as a result of this thesis. The many hours I was removed from them and the house while researching and writing placed an extra burden on them. The completion of this work was possible only through their sacrifice and willingness to do many of the male role chores around the house. I appreciate this sacrifice and will try now to devote the extra hours to my wife, Mary, and my children, Walter, Judee, Andy, Susie, and Stephen.

I express my sincere thanks to Mr. Kramer, Mr. Skarote and Dr. Siman from the Electrical Engineering Department for their guidance and advice in this project, to Barbara Rolla for her typing and special efforts in finalizing this thesis, and to Mr. Joseph Parlink for his photographic contributions.

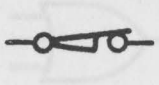
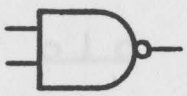
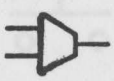
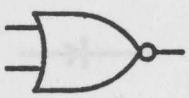
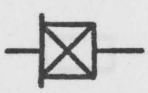
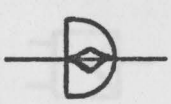
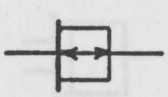
I am indebted to Mr. Chris Hastings for his help in providing data sheets and DSL materials for experimentation, to Mr. J. Fred Bucy from Texas Instruments, Inc. for providing a number of TTL integrated circuits for experimental use, to Mr. Gary W. Breeding from Monsanto Company for his help in obtaining LED displays, and to the Youngstown Sheet and Tube Company for making available prodac materials.

TABLE OF CONTENTS

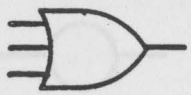
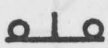
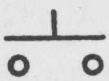
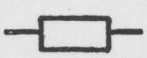
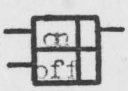
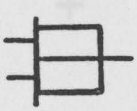
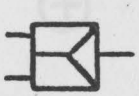
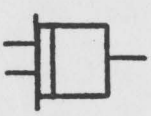
LIST OF SYMBOLS

SYMBOL	DEFINITION
	AND Gate
	AND Gate
	Battery
	Capacitor
	Contact (normally open)
	Contact (normally closed)
	D.C. Signal Converter
	Exclusive NOR
	Exclusive OR
	Ground
	Indicating Light
	Inverter

LIST OF SYMBOLS

SYMBOL	DEFINITION
	Limit Stop (normally closed)
	Limit Stop (normally closed-held open)
	Limit Stop (normally open)
	NAND Gate
	NOR Gate
	NOR Gate
	NOT Gate
	OFF Delay Timer
	ON Delay Timer
	On and OFF Delay Timer
	ON and OFF Delay Timer
	OR Gate

LIST OF SYMBOLS

SYMBOL	DEFINITION
	OR Gate
	Power AND (10 volt)
	Power AND (24 volt)
	Push Button (closed return)
	Push Button (open return)
	Rectifier
	Resistor
	Retentive Memory
	Retentive Memory
	Set-Reset Memory
	Set-Reset Memory

LIST OF SYMBOLS

SYMBOL	DEFINITION
	Solenoid or relay coil
	Transistor (NPN)
	Transistor (PNP)
/	Prime operator (negation)
−	Line over letter or number (negation)
•	Dot operator (Series Connection)
+	Plus operator (Parallel Connection)
⊕	Exclusive OR operator

LIST OF FIGURES

LIST OF FIGURES (CONT.)

LIST OF TABLES

CHAPTER I

INTRODUCTION

The object of this thesis is to develop a practical approach whereby electrical maintenance technicians and apprentices could through a "hands on" approach be able to understand and work with digital circuits and hardware.

The scope will be limited to developing a sufficient number of experiments to enable the electrical technician to adequately understand basic industrial digital circuitry. Three manufacturer's circuitry will be utilized. Cutler Hammer's DSL (Direct Static Logic) which employs conventional logic will be covered, as well as Westinghouse's Prodac and Texas Instruments TTL (Transistor-Transistor Logic) which utilizes inverting logic (NOR circuitry).

In many industries today the continued education of electrical technicians in the area of logic circuitry troubleshooting is seriously lacking. I will confine my remarks here to the basic steel industry with which I am more familiar.

This type of circuitry is becoming much more common in industry today and will be more so in the near future with new equipment installations and revamps on older equipment. This new equipment for a period of time generally requires little maintenance and the manufacturer probably handles problems for the first year. As the equipment ages and the responsibility to maintain it falls on the industrial maintenance people, the training or lack of training impact reveals itself.

Generally, a crash program of one or two weeks duration follows the installation of a new line or updating of control on an older installation. The men absorb a lot in a short time, but there is very little time to digest sufficiently for retentive purposes an adequate amount of the material covered. Often times the design engineers who have lived with the control from its start conduct these sessions. They understand the circuitry thoroughly but in many instances take a lot for granted and don't give the students a proper understanding of the overall system operation or how the control system accomplishes its purpose. There is a tendency to get directly into the theory of semiconductors or the design circuitry itself. My intention is not to be cricical because on one hand the design engineer probably doesn't understand too well what a blast furnace does or perhaps has never seen a hot strip mill operate and on the other hand, the technician probably doesn't grasp very rapidly, without experimenting with it, the latest circuit design capabilities. Each most likely feels more comfortable in the area he is most familiar with. Thus the design engineer will tend to stick with circuit design and operation while avoiding the overall system functions and the technician on the other hand, will probably be somewhat overwhelmed with his lack of understanding of the circuit details and quietly absorb what information he can.

From the training standpoint and for the average technician or maintenance man, a better approach would be to review the operation of the facility involved (Blast Furnace, Hot Strip, etc.) using flow diagrams, photographs, etc. and then take an individual unit (skip car, turnaround, etc.) and show how the control will accomplish the operations involved for that unit. Next, take a second unit (perhaps a little more advanced) break it down and show how the control accomp-

lishes this function. After general descriptions of what the control is expected to do, the basic building blocks can be developed and then the more complex circuitry of the building blocks can be explained.

It is probably critical to proper understanding that the individual get his hands on the parts and experiment with them. This is the basic intent of my thesis, that a technician by experimentation with inputs and outputs and interconnections of various logic devices will be more adequately equipped to maintain and understand industrial logic systems.

CHAPTER II

THEORY AND BASIC BUILDING BLOCKS

In comparing relay type circuits and static logic circuits, consider the following comparison

TABLE 1

RELAY-STATIC LOGIC COMPARISON

Relay Control	Static Control
Input Devices	Input Devices
Push buttons	Push buttons
Limit switches	Limit switches
Control Devices	Control Devices
Relays	Static logic
Output Devices	Output Devices
Contactors	Contactors
Solenoids	Solenoids

Figure 1 shows a basic diagram for a static logic control system.

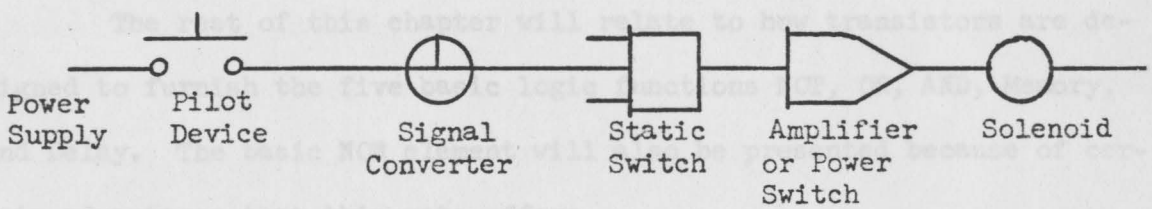


FIG. 1.--BASIC LOGIC SYSTEM

The power supply provides the required d.c. voltages for the operation of the static control components. This is generally 5, 10, or

24 volts, although higher voltages might be required for better reliability of the pilot devices and output devices.

The pilot devices could consist of push buttons, selector switches, limit switches or other similar devices for initiating intelligence for the control circuit. These pilot devices do not operate satisfactorily at low energy levels encountered in static switching. Higher voltages are needed to break through the contact resistance of these devices. The signal converter converts the higher energy level used by the pilot device to a lower level compatible with static logic components.

The static switch represents logic gates or static switches that are capable of driving other static switches either singly or as multiple units. The number of static switches used is determined by the complexity of the control required of the system.

The amplifier or power switch is a static switch capable of switching higher levels of power. The purpose of the power switch is to increase the output power level sufficiently to drive output devices such as relays, solenoids, and contactors.

The output device operates that which the system has been designed to control. It could be a starter for a motor, a solenoid for providing mechanical movement or a relay for energizing a bell or an alarm.

The rest of this chapter will relate to how transistors are designed to furnish the five basic logic functions NOT, OR, AND, Memory, and Delay. The basic NOR element will also be presented because of certain advantages that this gate offers.

A very brief explanation might be appropriate here to indicate how a transistor functions as a switch. For use as a switching device the transistor is generally used in the common emitter configuration. Figure 2 shows a basic transistor switch.

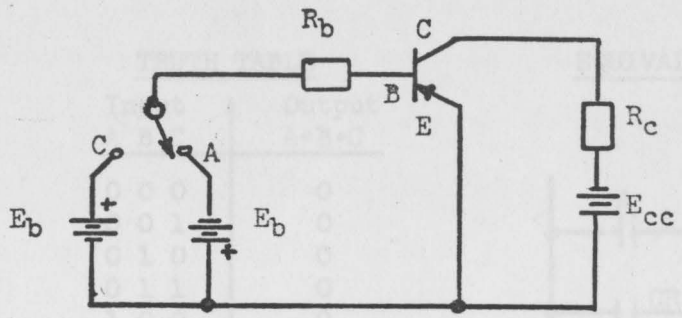


FIG. 2.--BASIC TRANSISTOR SWITCH

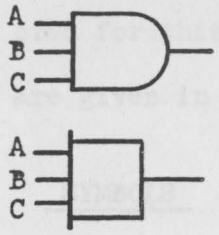
The control of current between the collector and emitter of the transistor is controlled by the base bias. If the base is made more negative then the emitter, the emitter junction is biased in the forward direction and current flows across the emitter junction to the collector. It requires only a small current in the base to control a larger current flowing through the collector-emitter path. When the switch is in position C the transistor is held in cutoff, because the base emitter junction is biased in a reverse direction, and no current flows from emitter to collector. Thus, we might say the emitter to collector switch is open. As the current applied to the base becomes negative enough saturation results and there is an extremely low impedance between collector and emitter. So if the switch is moved from C to A and back to C the collector to emitter path rapidly switches from a very high impedance state to a very low impedance state and back to the high impedance state. This is the basic operation of the transistor as a switch.

The "AND" Function

The AND logic function is accomplished by a device which produces an output only when every input is energized. Symbols encountered for this function, the truth table, and the equivalent relay circuit are

given in Figure 3.

SYMBOLS



TRUTH TABLE

Input A B C	Output A•B•C
0 0 0	0
0 0 1	0
0 1 0	0
0 1 1	0
1 0 0	0
1 0 1	0
1 1 1	1

EQUIVALENT RELAY CIRCUIT

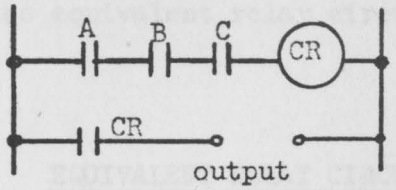


FIG. 3.--THE "AND" FUNCTION

Figure 4 shows a three input AND. When all three inputs have a ten volt signal applied, a positive ten volt output will be produced. If any of the inputs do not have a positive ten volt signal, a negative voltage will appear at the base of transistor T1 causing it to conduct. This in turn prevents transistor T2 from conducting and no output voltage will be present. All inputs must be present to obtain an output.

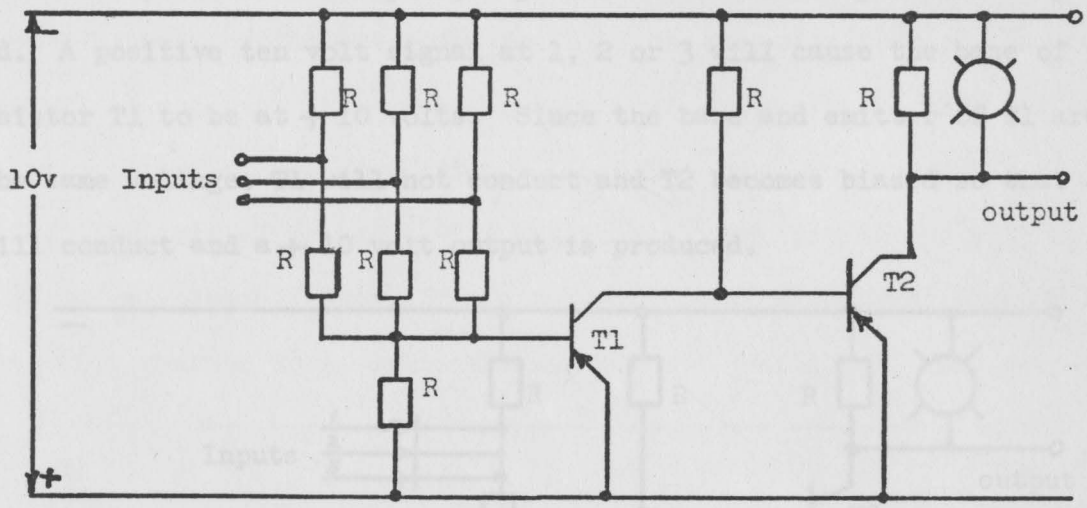
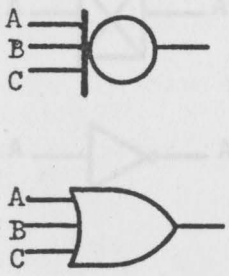


FIG. 4.--THE "AND" CIRCUIT

The "OR" Function

The OR logic function is accomplished by a device which produces an output when one or more of the inputs are energized. Symbols encountered for this function, the truth table, and the equivalent relay circuit are given in Figure 5.

SYMBOLS



TRUTH TABLE

Input A B C	Output A+B+C
0 0 0	0
0 0 1	1
0 1 0	1
0 1 1	1
1 0 0	1
1 0 1	1
1 1 0	1
1 1 1	1

EQUIVALENT RELAY CIRCUIT

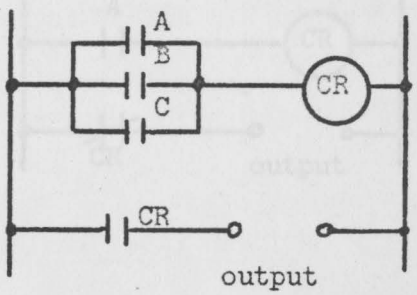


FIG. 5.--THE "OR" FUNCTION

Figure 6 shows a three input OR. When a positive ten volts is applied to any one of the inputs, a positive ten volt output will be produced. A positive ten volt signal at 1, 2 or 3 will cause the base of transistor T1 to be at + 10 volts. Since the base and emitter of T1 are at the same voltage, T1 will not conduct and T2 becomes biased so that it will conduct and a + 10 volt output is produced.

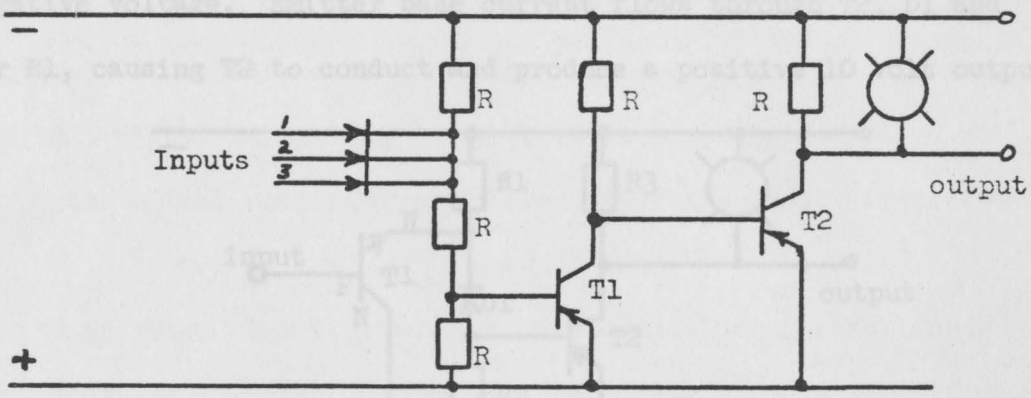


FIG. 6.--THE "OR" CIRCUIT

The "NOT" (Inverter) Function

The NOT (Inverter) function is accomplished by a device which produces an output only when the input is not energized. Symbols encountered for this function, the truth table, and the equivalent relay circuit are given in Figure 7.

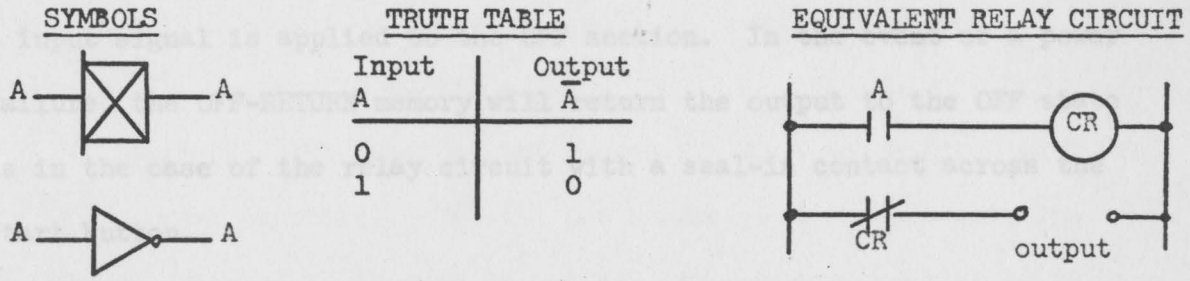


FIG. 7.--THE "NOT" FUNCTION

Figure 8 shows a typical NOT element circuit. A positive ten volt signal at the input will produce no output. When there is no positive ten volt input, there will be a positive ten volt output. If the input is at positive ten volts, current will flow through transistor T1 from base to emitter through resistor R1 to the negative side of the line, causing T1 to conduct. This makes the base of transistor T2 more positive, preventing it from conducting so that no output is produced. No positive input signal means T1 will not conduct and its emitter will be at a negative voltage. Emitter base current flows through T2, D1 and resistor R1, causing T2 to conduct and produce a positive 10 volt output.

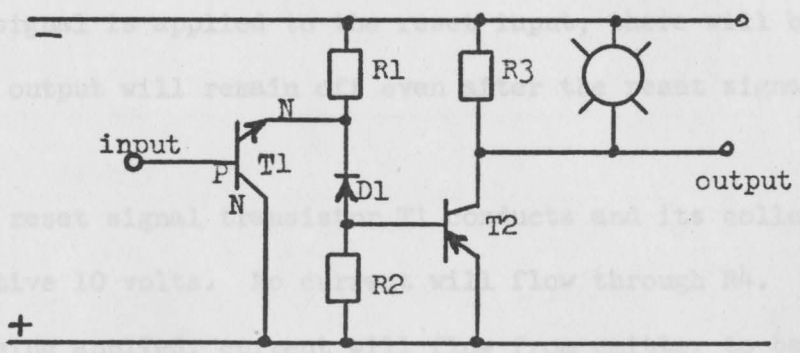
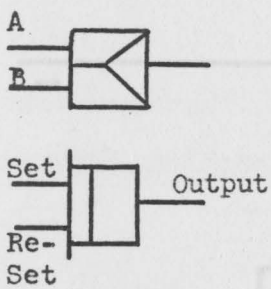


FIG. 8.--THE "NOT" CIRCUIT

The OFF-RETURN (Set-Reset) Memory

The OFF-RETURN function is accomplished by a device which returns the condition of output corresponding to the input last energized, except upon interruption of power, it returns to the off condition. As in the case of a seal-in relay circuit, a momentary signal to the A section will turn the unit on and the output will continue indefinitely until a B input signal is applied to the OFF section. In the event of a power failure, the OFF-RETURN memory will return the output to the OFF state as in the case of the relay circuit with a seal-in contact across the start button.

SYMBOLS



EQUIVALENT RELAY CIRCUIT

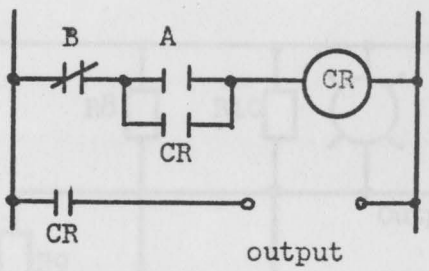


FIG. 9.--THE OFF-RETURN MEMORY FUNCTION

Figure 10 shows a set-reset memory circuit. If the set input receives a momentary + 10 volt signal, a +10 volts will be produced at the output and will remain even after the input set signal is removed. If a + 10 volt signal is applied to the reset input, there will be no output, and the output will remain off even after the reset signal is removed.

With no reset signal transistor T1 conducts and its collector will be at positive 10 volts. No current will flow through R4. If no set signal is being applied, current will flow from emitter to base of

transistor T2, through diode D1, and resistors R9 and R10, causing transistor T2 to conduct. Transistor T3 will not conduct and the output will be zero.

When a + 10 volt set signal is applied, no current can flow through diode D1, base current of transistor T2 stops and T2 cuts off. Transistor T3 conducts and a + 10 volts output is produced. Removal of the set signal causes no change since T3 and resistor R9 provide a + 10 volts to D1, keeping T2 turned off.

Applying the reset signal causes the base and emitter of T1 to be at the same potential. T1 will not conduct and current will flow from emitter to base of T2 through R4 and R1. T2 conducts preventing T3 from conducting and the positive 10 volt output goes to zero.

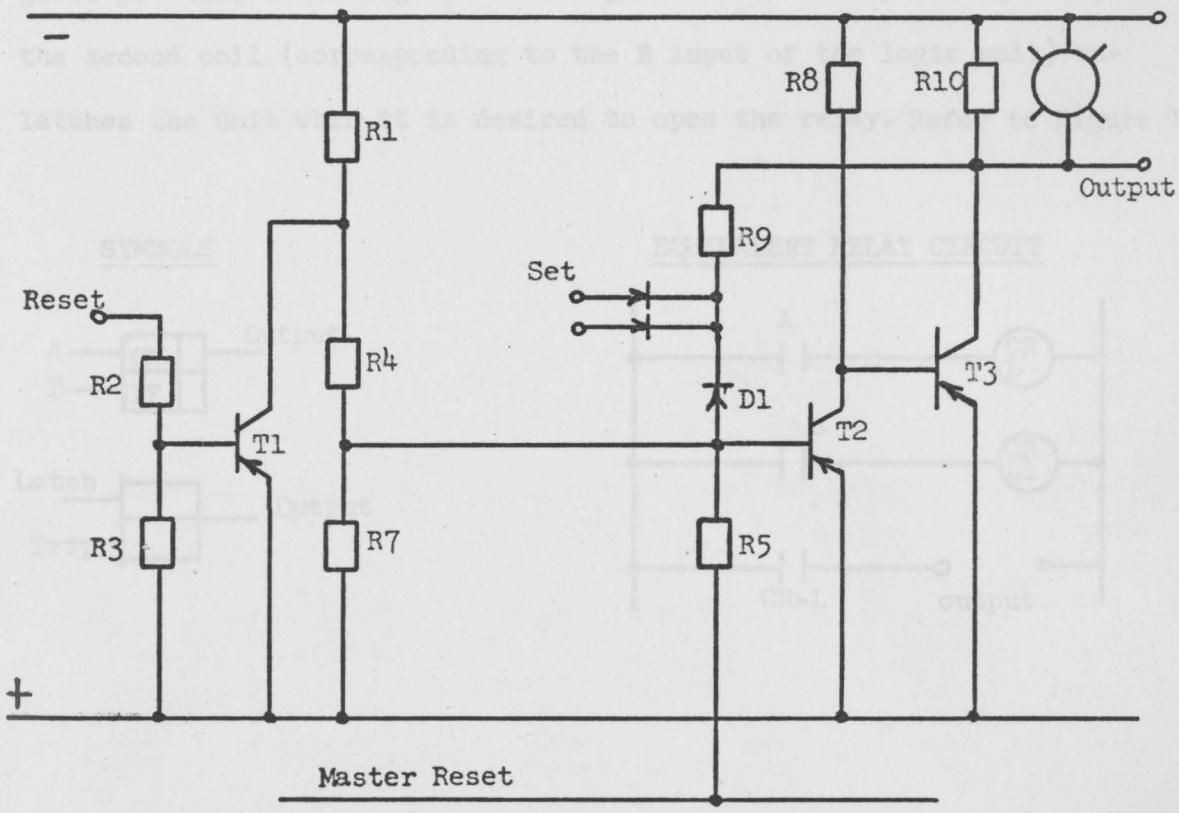


Fig. 10.--THE OFF-RETURN MEMORY CIRCUIT

The Retentive Memory

The retentive memory is accomplished by a device which retains the condition of output corresponding to the input last energized. The retentive memory always remembers the state which last existed after the restoration of power following a power failure. It is turned on and off exactly as is the off-return memory unit but in addition, when power returns after an outage, the circuit will be restored to the ON state if that was its original condition or to the OFF state if that was its original condition.

In relay circuitry retentive memory is accomplished by a device has two coils, one of them picks up the relay (equivalent to the A input of the logic unit) after which a mechanical latch holds it in the energized position following the de-energization of the operating coil, and the second coil (corresponding to the B input of the logic unit) unlatches the unit when it is desired to open the relay. Refer to Figure 11.

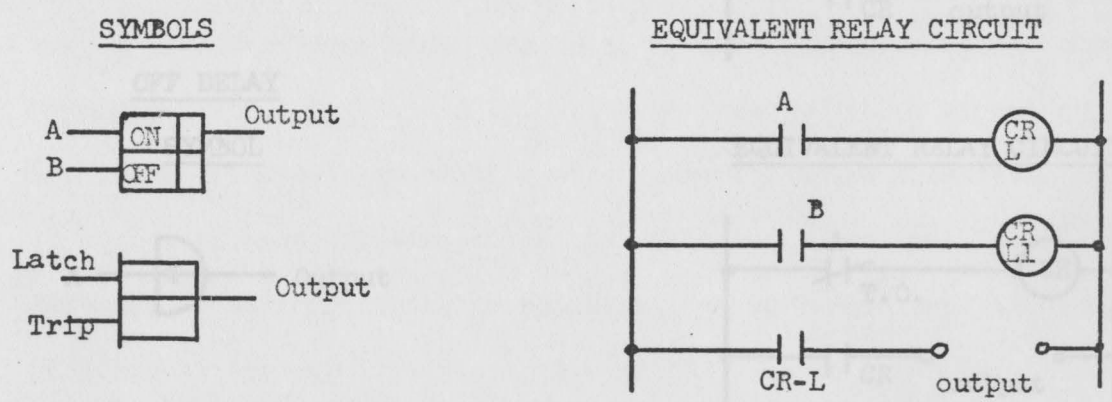


FIG. 11.--THE RETENTIVE MEMORY FUNCTION

The Delay Function

The delay function is accomplished by a device that produces an output after a definite intentional time delay after its input is energized (time delay energizing), or else whose output is de-energized following a definite intentional time delay after its input is de-energized (time delay de-energizing).

Delay components perform the same functions as timers in conventional relay circuits. The two general types are ON delay (output produced following a definite intentional time delay after input is energized), and OFF delay (output removed following a definite intentional time delay after input is de-energized). Refer to Figure 12.

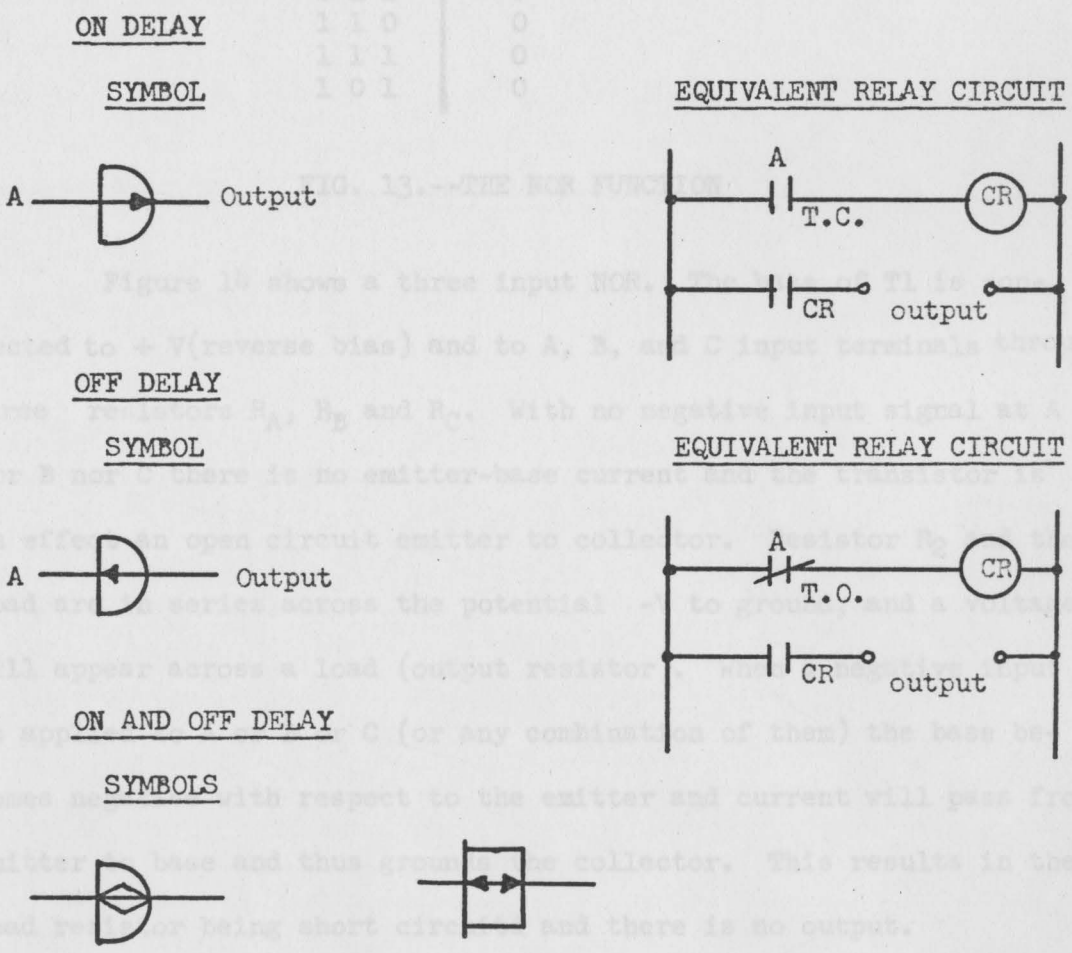
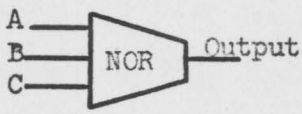


FIG. 12.--THE DELAY FUNCTION

The NOR Function

The NOR function is accomplished by a circuit that combines the OR and NOT functions together. This is called NOR logic since we get an output if neither A NOR B NOR C is present. The NOR circuit would become a simple NOT if only one input were used. This device can be used to handle the AND, OR, NOT and memory functions.

SYMBOL



TRUTH TABLE

A	B	C	Output
0	0	0	1
0	0	1	0
0	1	0	0
1	0	0	0
0	1	1	0
1	1	0	0
1	1	1	0
1	0	1	0

COMPARES TO

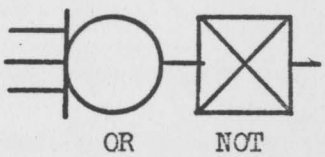


FIG. 13.--THE NOR FUNCTION

Figure 14 shows a three input NOR. The base of T1 is connected to + V(reverse bias) and to A, B, and C input terminals through three resistors R_A, R_B and R_C. With no negative input signal at A nor B nor C there is no emitter-base current and the transistor is in effect an open circuit emitter to collector. Resistor R_2 and the load are in series across the potential -V to ground, and a voltage will appear across a load (output resistor). When a negative input is applied to A or B or C (or any combination of them) the base becomes negative with respect to the emitter and current will pass from emitter to base and thus grounds the collector. This results in the load resistor being short circuitd and there is no output.

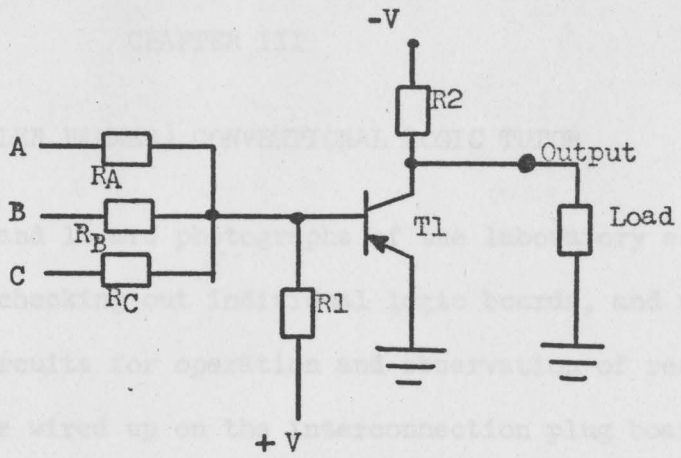


FIG. 14.--THE NOR CIRCUIT

CHAPTER III

DSL (CUTLER HAMMER) CONVENTIONAL LOGIC TUTOR

Figures 15 and 16 are photographs of the laboratory equipment to be used in checking out individual logic boards, and wiring up various logic circuits for operation and observation of results. All circuits will be wired up on the interconnection plug board. Note the four selector switches and three push buttons along the left side, the four indicating lights along the right side, the on-off switch at the lower right, the bucket that can accommodate up to six logic boards at a time, and the interconnection plug board where all wiring will be done.

The power supply provides 48v, 24v and 10v filtered direct current which is available on the interconnection plug board as marked on the corresponding buses. Depending on what components are used, one, two or three different voltages may be used in the static switching control. These voltages are related as indicated in Figure 17.

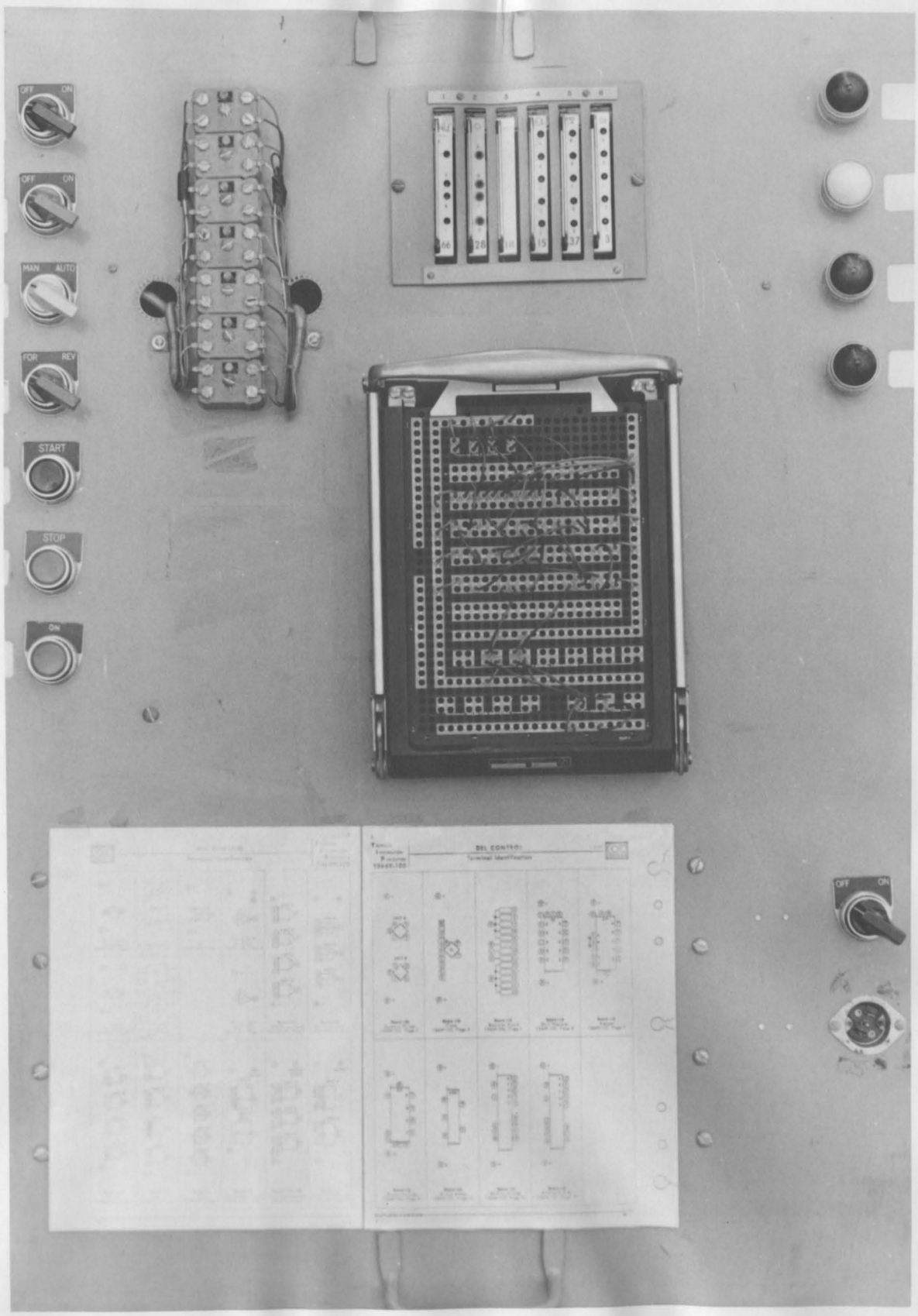


FIG. 15.--LOGIC TUTOR (DSL)

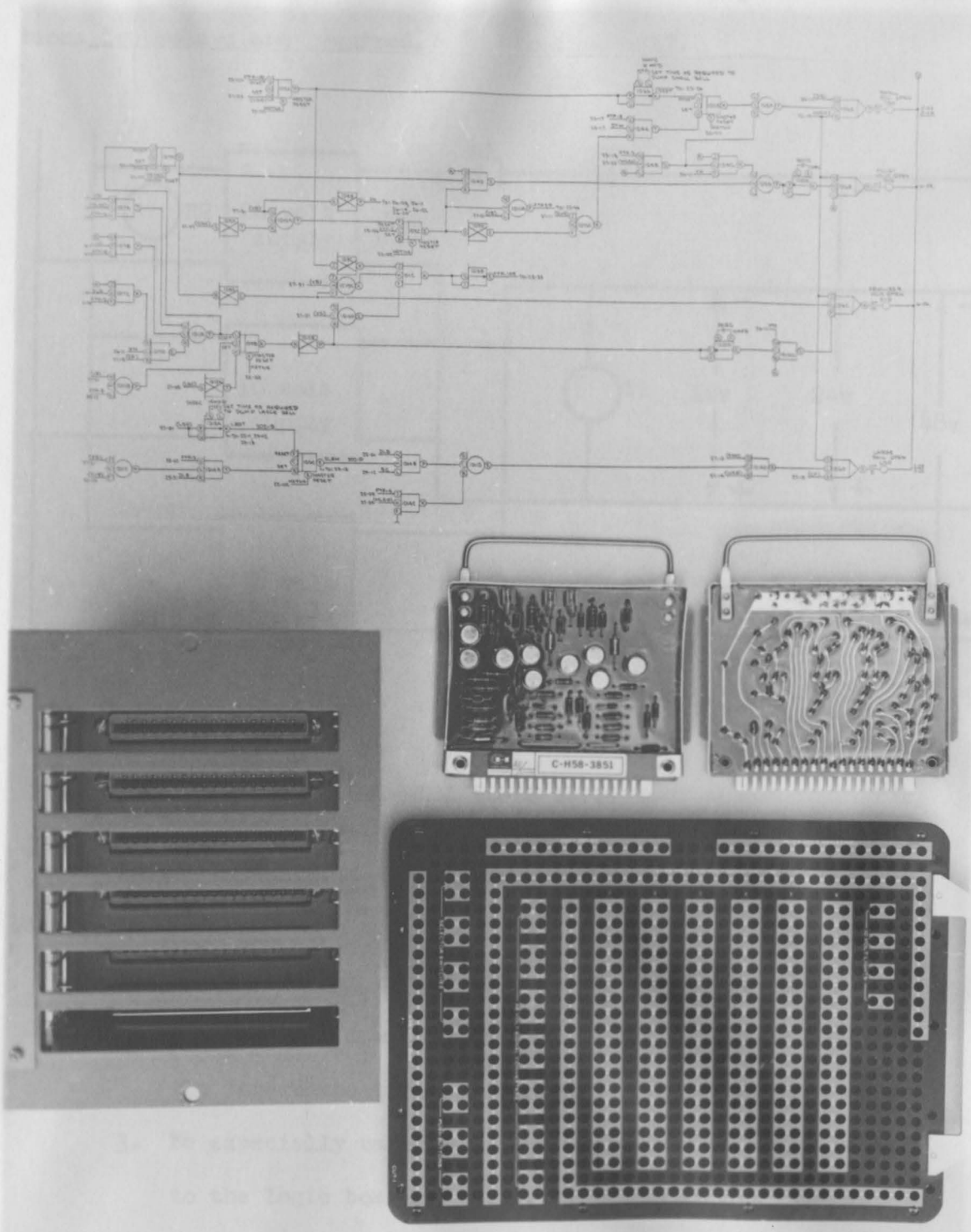


FIG. 16.--DSL CIRCUIT BOARD AND INTERCONNECTION BOARD

Because of the interfacing between voltages accomplished by the 24v power and the signal converter, it is important that the 10 volt DC is first on and last off. To insure this in power loss situations two relays are required. Refer to figure 17.

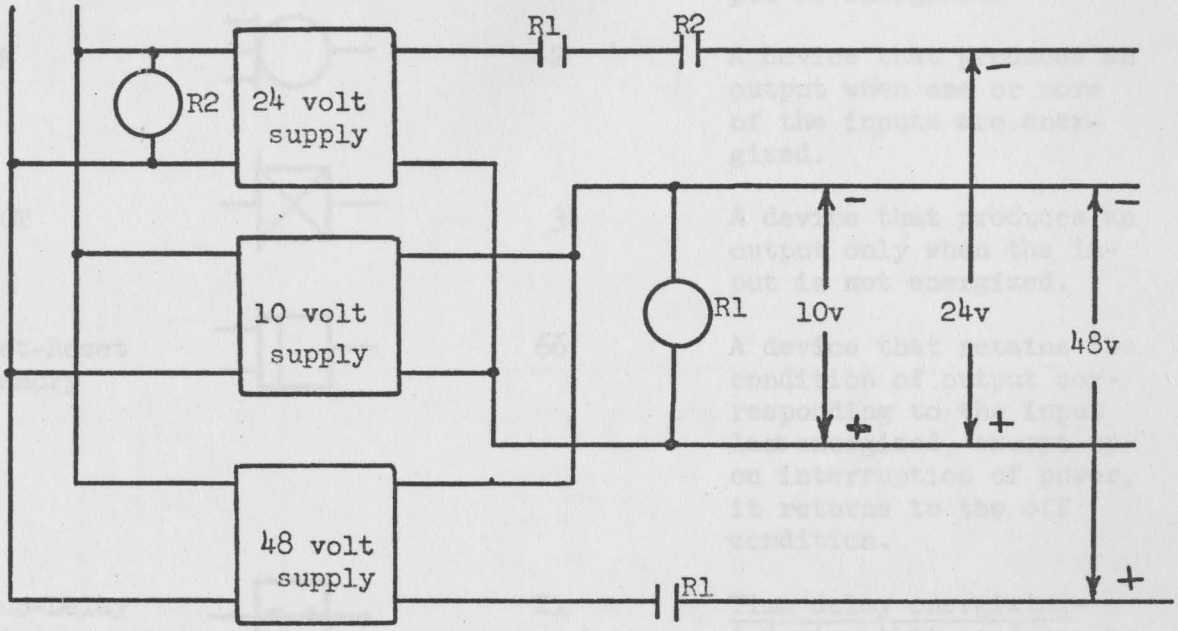


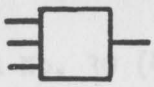
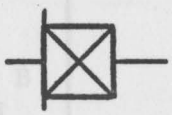
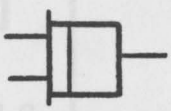
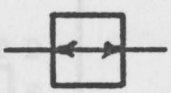
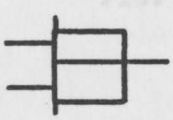
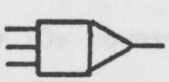
FIG. 17.--DSL POWER SUPPLY

In the experiments that follow, certain precautions must be observed.

1. Never pull out or insert boards while power is on.
2. Turn power off when making or breaking connections on the interconnection plug board.
3. Be especially careful not to apply 24 or 48 volt power to the logic boards.
4. If at all in doubt about the circuitry, have an instructor check it out before applying power.

TABLE 2

CONVENTIONAL LOGIC SYMBOLS AND DEFINITIONS

Function	Symbol	Board Number	Definition
AND		30	A device that produces an output only when every input is energized.
OR		2	A device that produces an output when one or more of the inputs are energized.
NOT		3	A device that produces an output only when the input is not energized.
Set-Reset Memory		66	A device that retains the condition of output corresponding to the input last energized, except upon interruption of power, it returns to the off condition.
Duo-Delay Timer		21	Time delay energizing- A device that produces an output following a definite intentional time delay after its input is energized. Time delay de-energizing- A device whose output is de-energized following a definite intentional time delay, after its input is de-energized.
Retentive Memory		46	A device that retains the condition of output corresponding to the input last energized.
10v Power AND		32	An AND gate in which the inputs control a local source of power to produce an output enlarged relative to the input.
24v Power AND		36	

Experiment 1 (The AND Function)

Object:

To study the AND function and check out the DSL AND board.

Given:

1. Board No. 30 (4 unit AND)

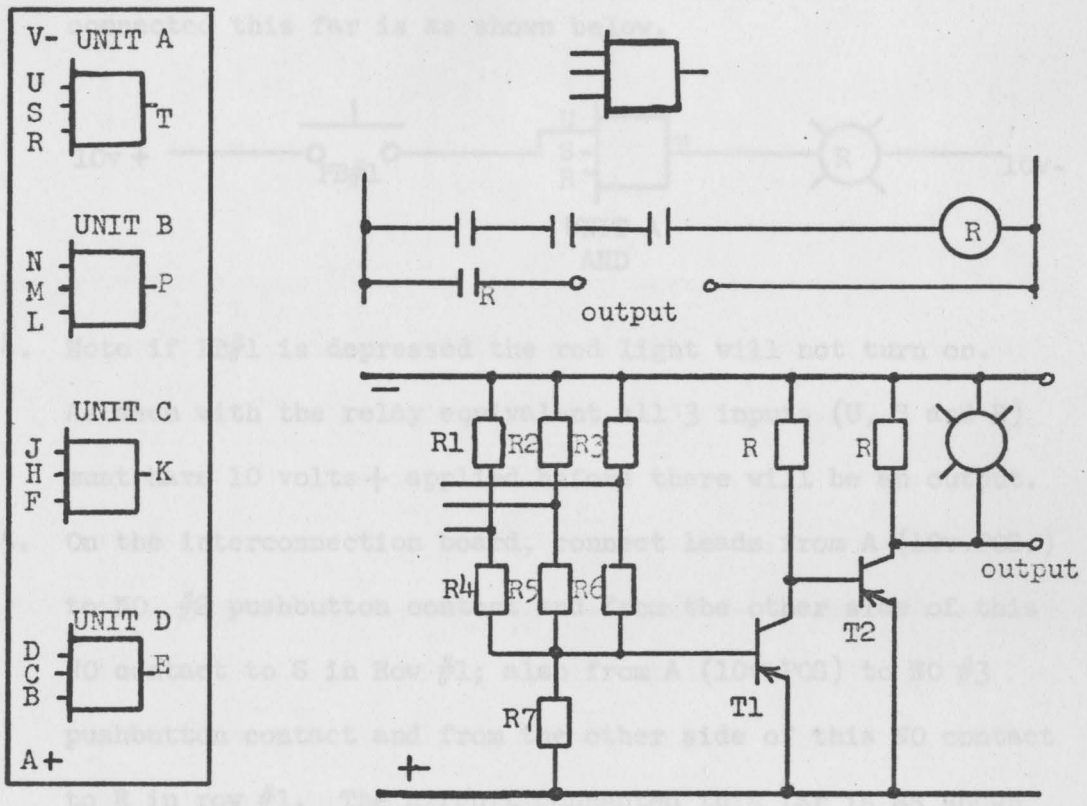
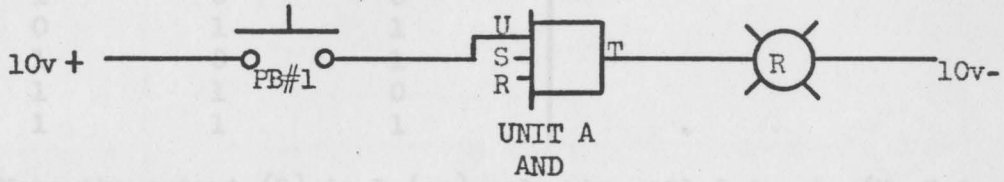


FIG. 18.--THE DSL AND BOARD

Procedure:

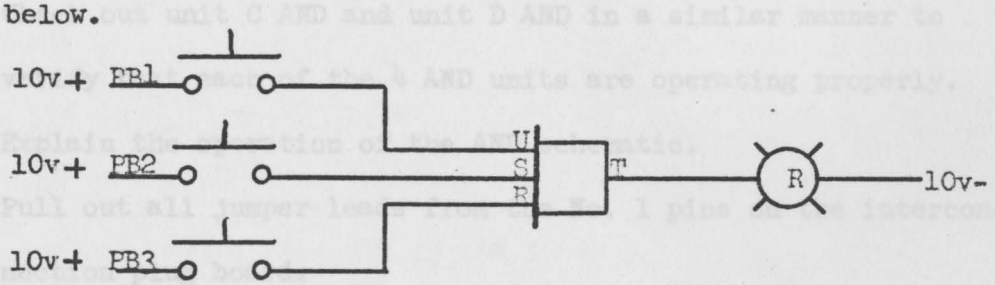
1. Insert Board #30 (4 unit AND) into bucket slot #1.
2. Apply 10v power to this board by jumpering from A (10v pos.) bus to letter A in the #1 row of pins on the interconnection patch board and from the V (10v NEG) bus to letter V in the #1 row of pins on the interconnection board.

3. On the interconnection board connect leads from A (+ 10v) to normally open #1 pushbutton contact; from the other side of the the NO pushbutton contact to U in Row #1 (first input of unit A AND): from T in Row #1 to the red light, and from the other side of the red light to 10v NEG. bus. The circuit connected this far is as shown below.



4. Note if PB#1 is depressed the red light will not turn on. As seen with the relay equivalent all 3 inputs (U, S and R) must have 10 volts + applied before there will be an output.

5. On the interconnection board, connect leads from A (10v POS.) to NO #2 pushbutton contact and from the other side of this NO contact to S in Row #1; also from A (10v POS) to NO #3 pushbutton contact and from the other side of this NO contact to R in row #1. The circuit connected this far is as shown below.



6. Complete the truth table by examining each of the possible combinations of depressing the 3 push buttons. If the red

light is on, put a 1 in the R column, and if the light is off, put a 0 in the R column for each of the 8 possible combinations for pushing the 3 buttons.

PB1	PB2	PB3	R
0	0	0	
0	0	1	
0	1	0	
1	0	0	
0	1	1	
1	0	1	
1	1	0	
1	1	1	

7. Note the output (R) is 1 (on) only when all 3 inputs (U, S & R) are 1 (energized). This constitutes the AND function that says when all three inputs have a + 10 volts applied a + 10v output will be produced.
8. Transfer the input and output leads from unit A to unit B. That is in row #1 of the interconnection board move U to N, S to M, R to L and T to P. Check out unit B "AND" by verifying that there will only be an output (red light on) when all three pushbuttons are depressed.
9. Check out unit C AND and unit D AND in a similar manner to verify that each of the 4 AND units are operating properly.
10. Explain the operation of the AND schematic.
11. Pull out all jumper leads from the No. 1 pins on the interconnection plug board.

Experiment 2 (The OR Function)

Object:

To study the OR function and check out the DSL OR board.

Given:

1. Board No. 2 (4 unit OR)

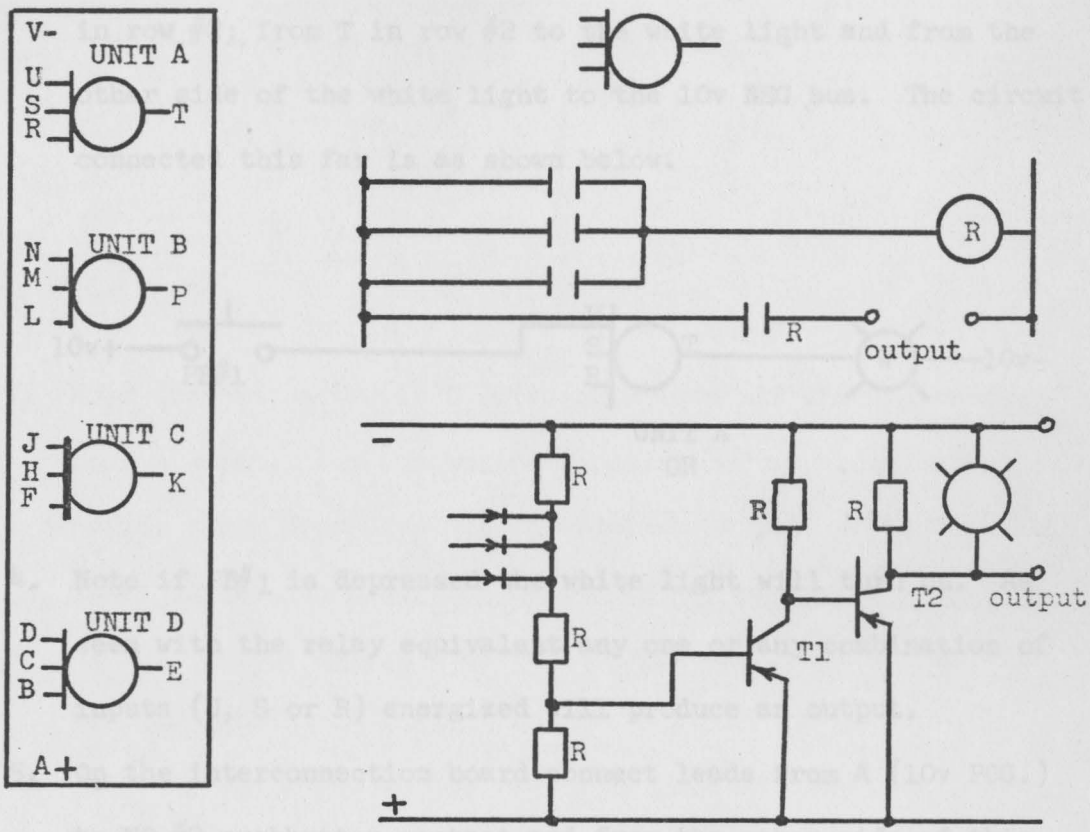


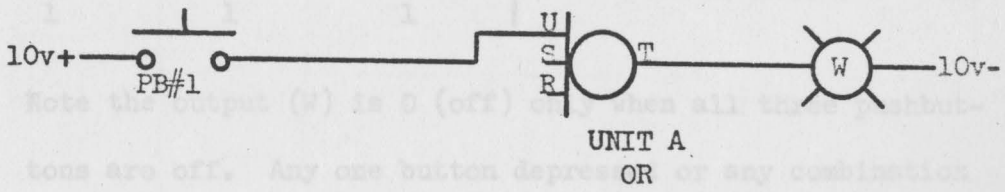
FIG. 19.--THE DSL OR BOARD

Procedure:

1. Insert Board #2 (4 unit OR) into bucket slot #2.
2. Apply 10v power to this board by jumpering from A (10v POS.) bus to letter A in the #2 row of pins on the interconnection

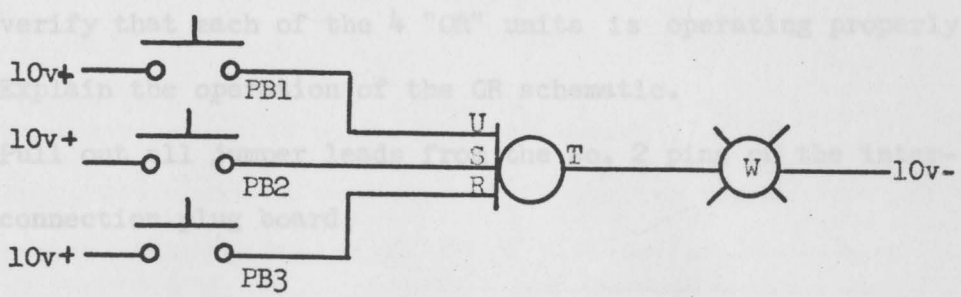
patch board and from the V (10v NEG.) bus to letter V in the #2 row of pins on the interconnection board.

3. On the interconnection board, connect leads from A (10v POS.) to normally open #1 pushbutton contact; from the other side of the NO #1 pushbutton contact to U (first input of unit A OR) in row #2; from T in row #2 to the white light and from the other side of the white light to the 10v NEG bus. The circuit connected this far is as shown below.



4. Note if PB#1 is depressed the white light will turn on. As seen with the relay equivalent any one or any combination of inputs (U, S or R) energized will produce an output.

5. On the interconnection board connect leads from A (10v POS.) to NO #2 pushbutton contact and from the other side of this NO contact to S in row #2; also from A (10v POS.) to NO #3 pushbutton contact and from the other side of this NO contact to R in row #2. The circuit connected this far is as shown below.



6. Complete the truth table by examining each of the possible combinations of depressing the 3 push buttons. If the white light is on put a 1 in the W column, and if the light is off put a 0 in the W column for each of the 8 possible combinations for pushing the 3 buttons.

PB1	PB2	PB3	W
0	0	0	
0	0	1	
0	1	0	
1	0	0	
0	1	1	
1	0	1	
1	1	0	
1	1	1	

7. Note the output (W) is 0 (off) only when all three pushbuttons are off. Any one button depressed or any combination of the three depressed will produce an output. This consititutes the OR function that says when any one or any combination of inputs have a + 10 volts applied a + 10v output will be produced.
8. Transfer the input and output leads from unit A to unit B. That is in row #2 of the interconnection board move U to N, S to M, R to L and T to P. Check out unit B "OR" by verifying that there will be an output if any one or any combination of inputs are energized.
9. Check out unit C "OR" and unit D "OR" in a similar manner to verify that each of the 4 "OR" units is operating properly.
10. Explain the operation of the OR schematic.
11. Pull out all jumper leads from the No. 2 pins on the interconnection plug board.

Experiment 3 (The NOT Function)

Object:

To study the NOT function and check out the DSL NOT board.

Given:

1. Board No. 3 (5 unit NOT)

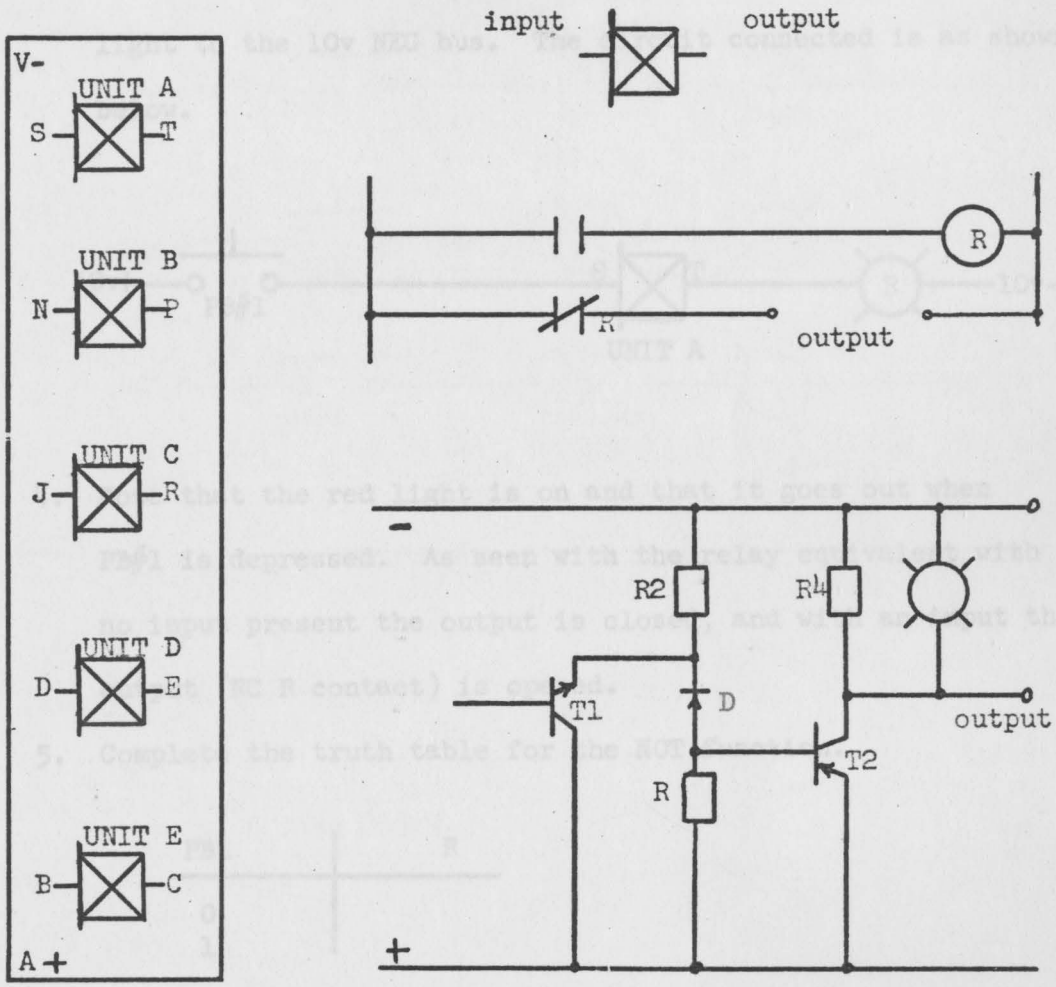


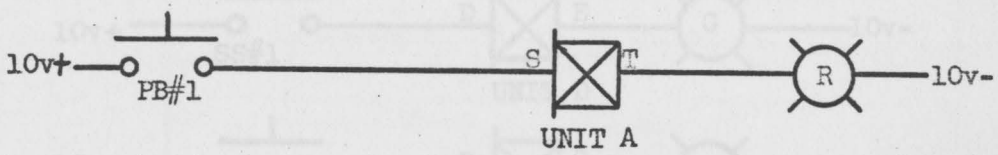
FIG. 20.--THE DSL NOT BOARD

Procedure:

1. Insert Board #3 (5 unit NOT) into bucket slot #3.
2. Apply 10v power to this board by jumpering from A (10v POS) bus to letter A in the #3 row of pins on the interconnection

patch board, and from the V (10v NEG) bus to letter V in the #3 row of pins on the interconnection board.

3. On the interconnection board, connect leads from A (10v POS) to normally open #1 pushbutton contact; from the other side of the NO #1 pushbutton contact to S in row #3; from T in row #3 to the red light, and from the other side of the red light to the 10v NEG bus. The circuit connected is as shown below.



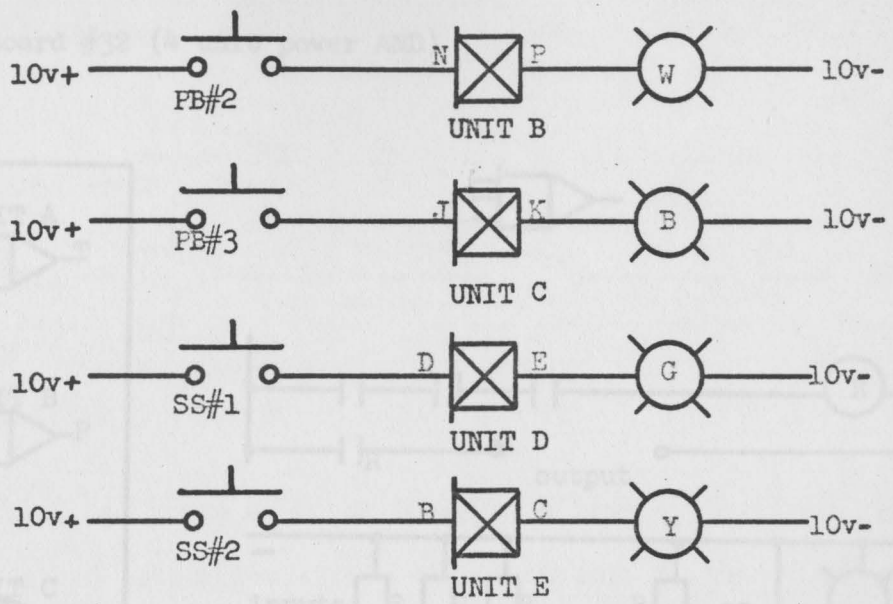
4. Note that the red light is on and that it goes out when PB#1 is depressed. As seen with the relay equivalent with no input present the output is closed, and with an input the output (NC R contact) is opened.

5. Complete the truth table for the NOT function.

PB1	R
0	
1	

6. Note that with the NOT function there is an output when no input is present and there is no output when the input is present.

7. Set up the following circuits to check out each of the other NOT units on the NOT board.



8. Explain the operation of the NOT schematic.

9. Pull out all jumper leads from the No. 3 pins on the inter-connection plug board.

Experiment 4 (The 10v Power AND)

Object:

To check out the DSL 10volt power AND board.

Given:

1. Board #32 (4 unit power AND)

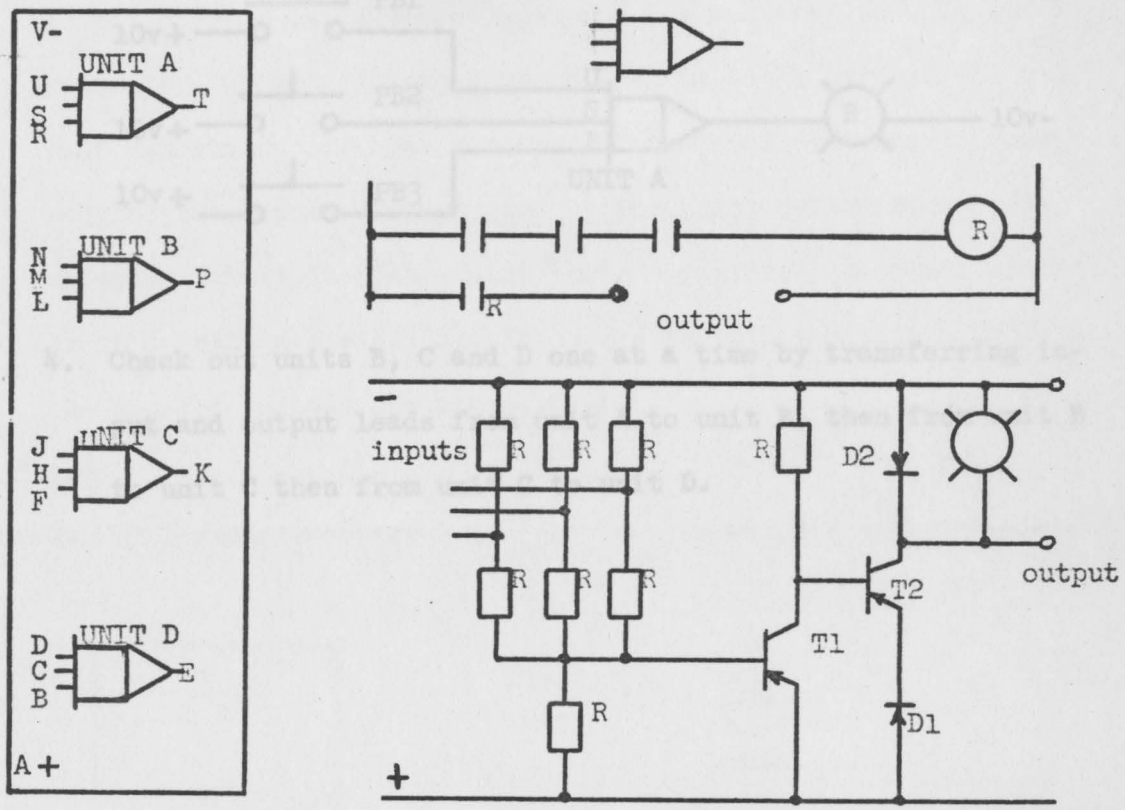


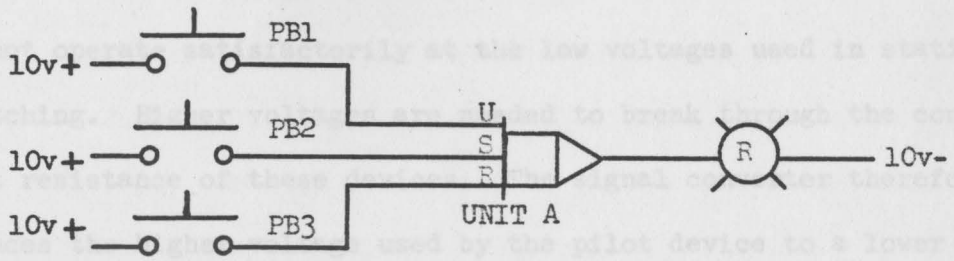
FIG. 21.--THE DSL POWER AND BOARD

Procedure:

1. Insert Board #32 (4 unit power AND) into bucket slot #5.
2. Apply 10v power to this board by jumpering from A bus to let-

ter A in the #5 row of the interconnection patch board, and from V bus to letter V in the #5 row on the interconnection board.

3. Set up the following circuit to check out unit A power AND.



4. Check out units B, C and D one at a time by transferring input and output leads from unit A to unit B, then from unit B to unit C then from unit C to unit D.

Experiment 5 (D.C. Signal Converter)

Object:

To check out and apply the d.c. signal converter.

Information:

The signal converter is necessary in most practical applications because pilot devices, such as push buttons and limit switches, do not operate satisfactorily at the low voltages used in static switching. Higher voltages are needed to break through the contact resistance of these devices. The signal converter therefore reduces the higher voltage used by the pilot device to a lower voltage compatible with static logic circuitry. A signal converter is a voltage divider and it lowers the pilot device voltage to the desired voltage for logic units.

Given:

1. DC Signal Converter

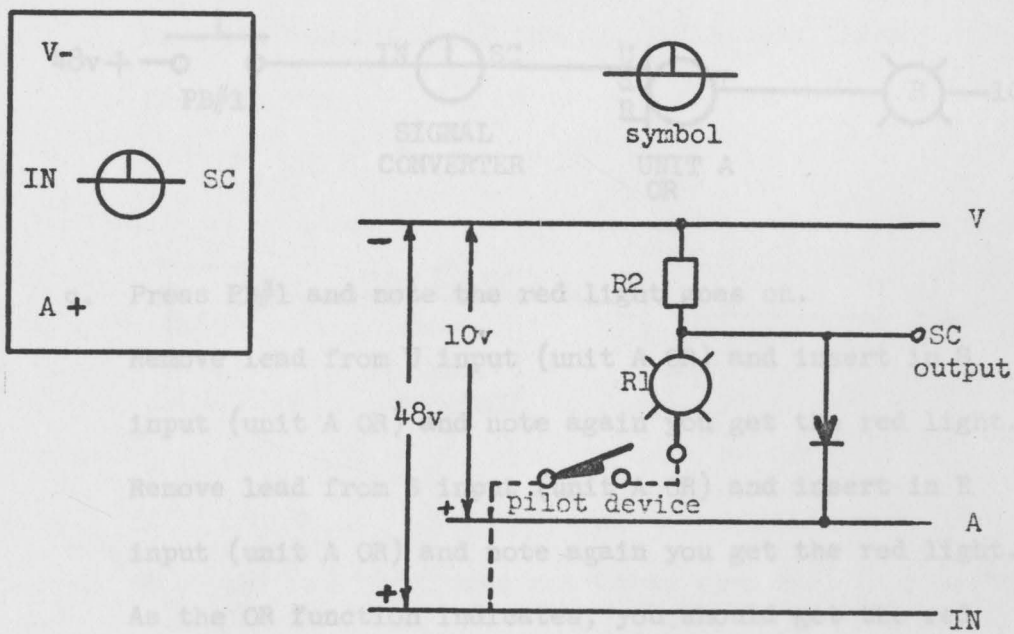


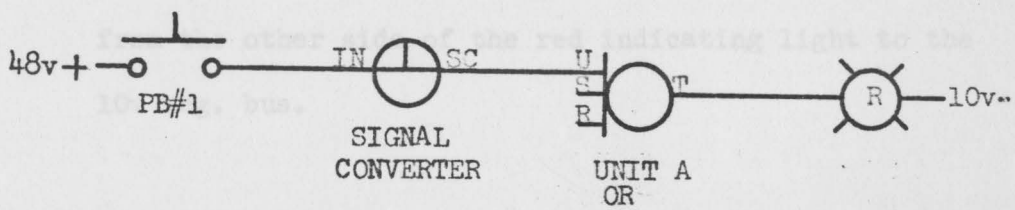
FIG. 22.--THE DSL D.C. SIGNAL CONVERTER

Procedure:

1. Wire up the A unit of the OR board and an indicating light from the output of a signal converter. To do this see that the OR board is in bucket slot #2 and wire as follows:

   a. Apply 10v power to the OR board by jumpering from A bus and V bus to A and V respectively on #2 row of the interconnection plug board.

   b. Jumper from 48v + bus to the normally open contact on PB#1, from the other side of PB#1 to the in terminal of the signal converter. Jumper from A bus and V bus to A and V respectively on the signal converter. Jumper from SC (signal converter output) to U (input of unit A OR). Jumper from T (output or unit A OR) to the red indicating light and from the other side of the red indicating light to the 10v neg. bus.



   c. Press PB#1 and note the red light goes on. Remove lead from U input (unit A OR) and insert in S input (unit A OR) and note again you get the red light. Remove lead from S input (unit A OR) and insert in R input (unit A OR) and note again you get the red light. As the OR function indicates, you should get the red light if U or S or R or any combination of them is en-

ergized.

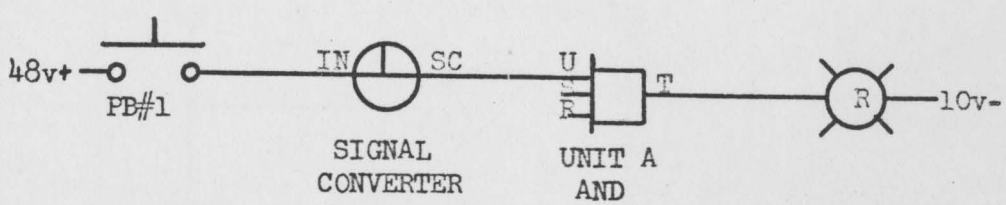
d. Remove all jumpers from the interconnection board.

2. Wire up the A unit of the AND board and an indicating light from the output of a signal converter. To do this see that the AND board is in bucket slot #1 and wire as follows:

a. Apply 10v power to the AND board by jumpering from A bus and V bus to A and V respectively on #1 row of the interconnection plug board.

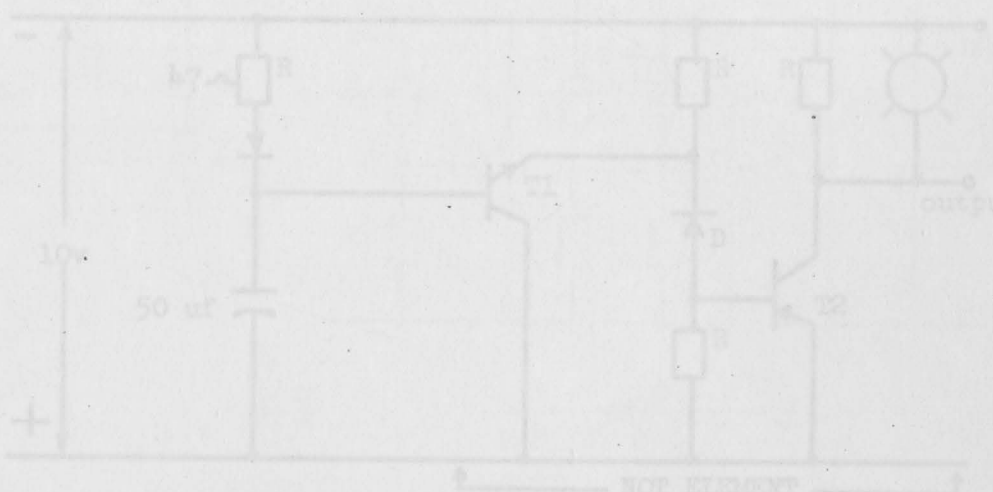
b. Apply 10v power to the signal converter by jumpering from A bus and V bus to A and V respectively for the signal converter on the interconnection plug board.

c. Jumper from the 48v + bus to the N.O. contact on PB#1, from the other side of PB#1 to the in terminal of the signal converter. Jumper from SC (signal converter output) to U (input of unit A AND). Jumper from T (output of unit A AND) to the red indicating light and from the other side of the red indicating light to the 10v neg. bus.



d. Note the red light does not go on when PB#1 is pressed since unused inputs of any AND units must have 10volts +

applied to them. Jumper from A (10v+ bus) to both S and R inputs of the unit A AND. Now when PB#1 is pressed, the red light goes on. Since U, S and R inputs are energized (10 volts + applied) the red light (output) lights.



Experiment 6 (Set-Reset Memory)

Object:

To study Set-Reset Memory and check out the DSL Set-Reset Memory board.

Information:

The term reset means returning a switch to a predetermined state. Example resetting a set reset memory to the no output condition. When the 10 volt power is first turned on, the transistors in the system start turning on. In elements such as ANDS, ORS, and NOTS the inputs originating from limit switches and pushbuttons insure that the proper transistors end up conducting. Memory type circuits, those that pick up on a short signal and latch in, however cannot have their input states predictable without a resetting action. For this reason a master reset terminal is provided that resets all elements on the board. The master reset terminal should be held negative to reset and then positive to permit normal operation.

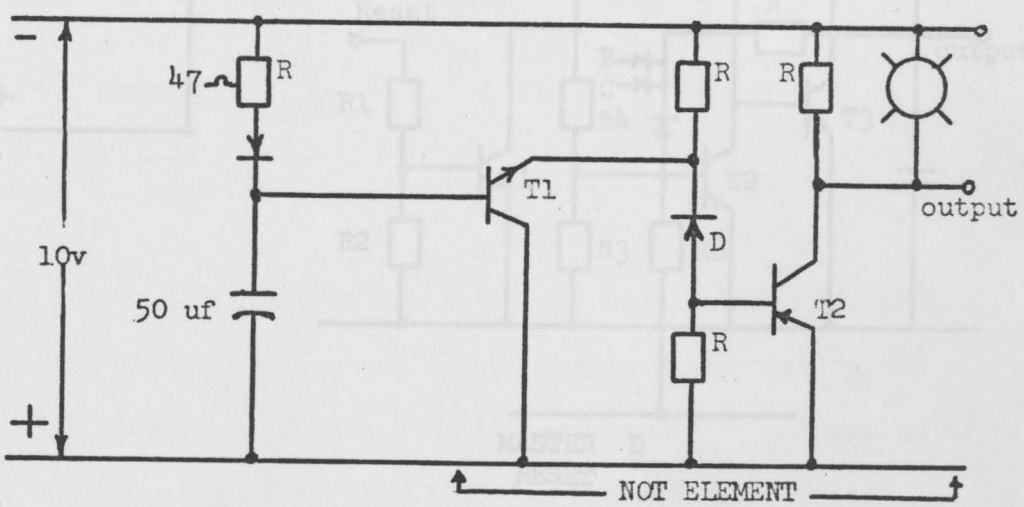


FIG. 23.--THE RESET GATE

This reset gate plus a set-reset memory can be used to provide under voltage protection.

Given:

1. Board No. 66 (3 unit set-reset memory)
2. Board No. 3 (5 unit NOT)
3. Reset resistor-capacitor network

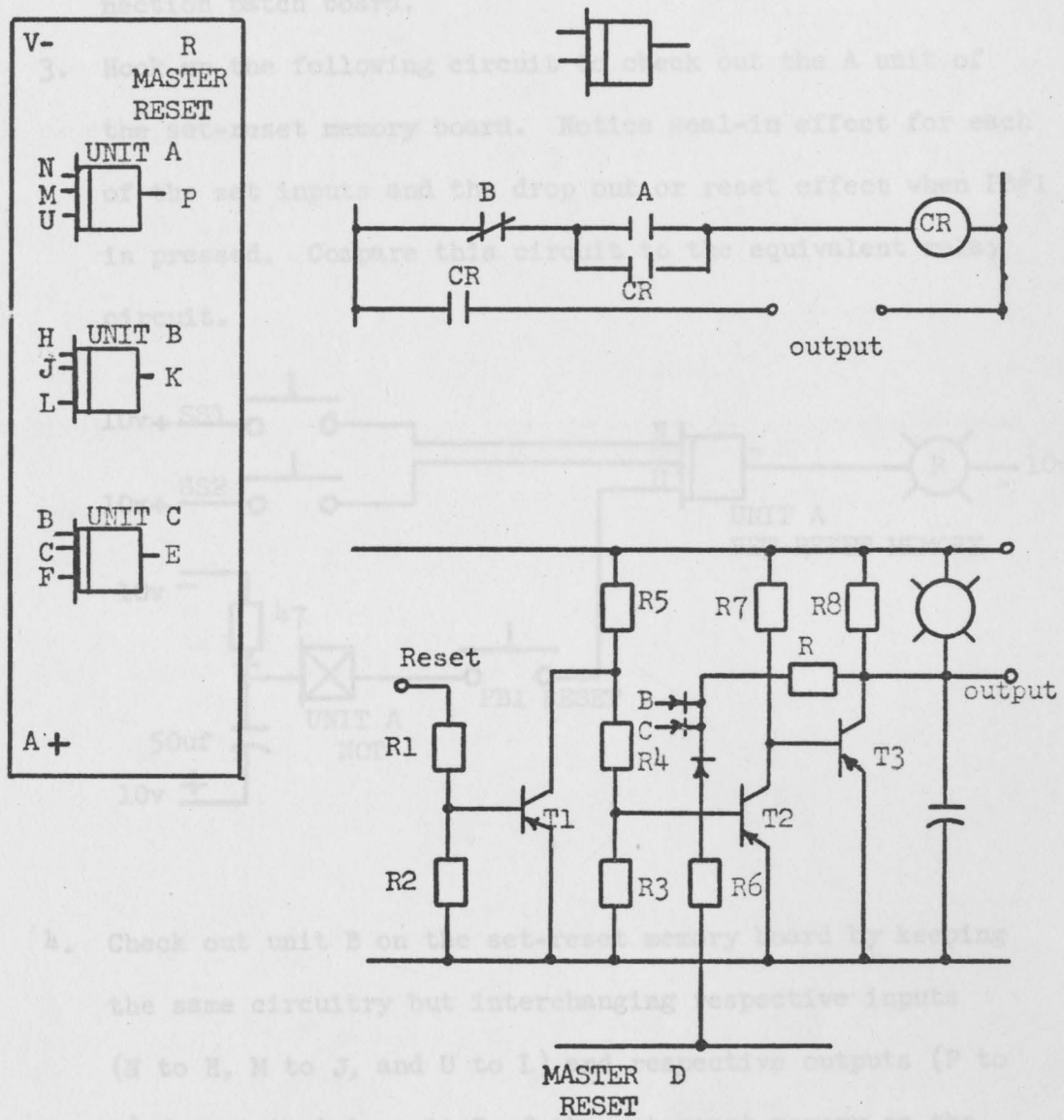
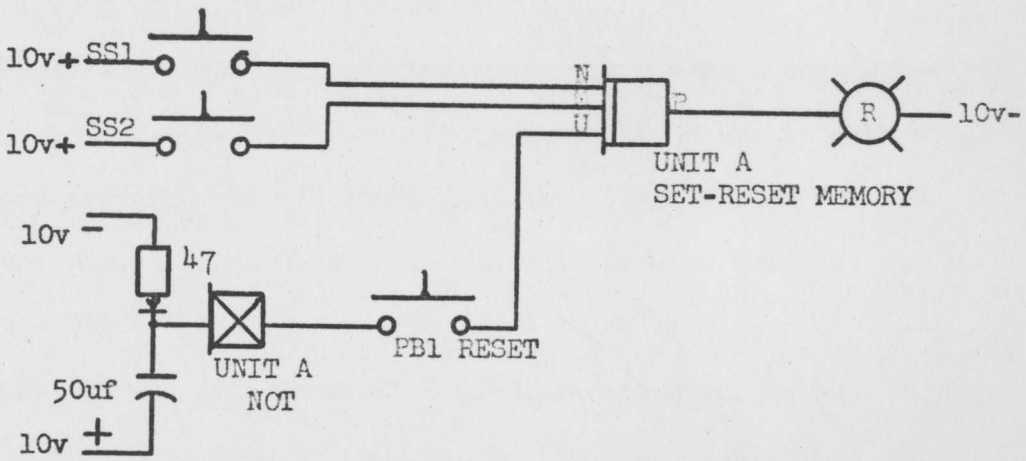


FIG. 24.--THE DSL SET-RESET MEMORY BOARD

Procedure:

1. Insert Board #66 (3 unit Set-Reset Memory) into bucket slot #4. Insert Board #3 (4 unit NOT) into bucket slot #5.
2. Apply 10v power to board #66 by jumpering A bus and V bus to respective letters in the #4 row on the interconnection patch board. Apply 10v power to board #3 by jumpering A bus and V bus to respective letters in the #5 row on the interconnection patch board.
3. Hook up the following circuit to check out the A unit of the set-reset memory board. Notice seal-in effect for each of the set inputs and the drop out or reset effect when PB#1 is pressed. Compare this circuit to the equivalent relay circuit.



4. Check out unit B on the set-reset memory board by keeping the same circuitry but interchanging respective inputs (N to H, M to J, and U to L) and respective outputs (P to K) from unit A to unit B of the set reset memory on the interconnection plug board.

5. Check out unit C on the set-reset memory board by keeping the same circuitry but interchanging respective inputs (H to B, J to C, and L to F) and respective outputs (K to E) from unit B to unit C of the the set reset memory on the interconnection plug board.

Experiment 7 (Interconnecting DSL Gates)

Object:

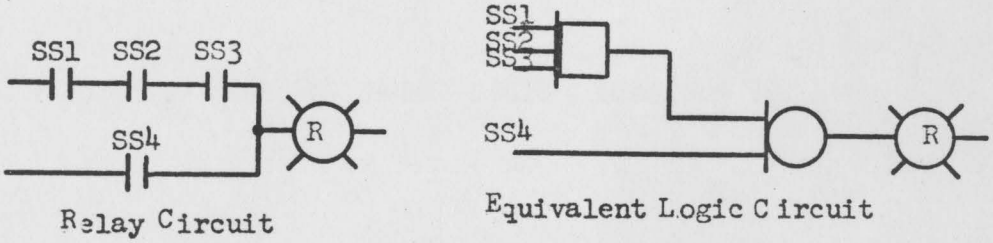
To become better acquainted with interconnections between logic gates and to be better able to compare relay circuitry with its equivalent in DSL logic circuitry.

Given:

1. Board #30 (4 unit AND)
2. Board #2 (4 unit OR)
3. Board #3 (5 unit NOT)
4. Board #32 (4 unit 10v power AND)
5. 4 signal converters

Procedure:

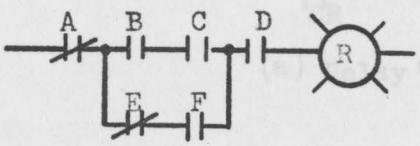
1. Plug in logic boards, 30, 2, 3, and 32 into bucket slots 1, 2, 3 and 4 respectively.
2. Apply 10v power for each board and the 4 signal converters by jumpering from the 10v + and from the 10v — bus to each board and converter on the interconnection plug board. NOTE: Do not remove these power feed connections when told to remove jumpers.
3. Compare the relay and DSL logic circuits given below. Wire up the logic circuit and compare its operation to the relay circuit. Remove jumpers.



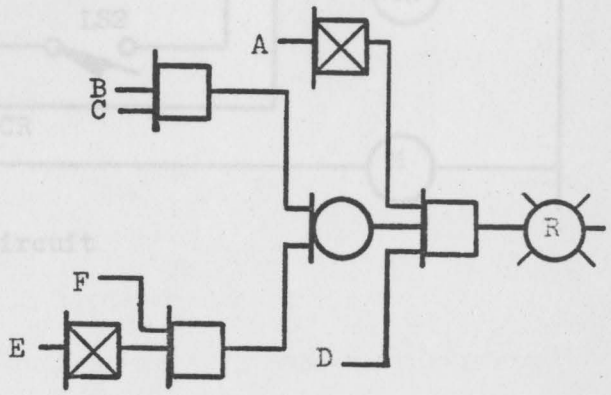
Relay Circuit

Equivalent Logic Circuit

4. Compare the relay equivalent circuit and the DSL logic circuits given below. Wire up the logic circuit and compare its operation to the relay circuit. Use SS1, SS2, SS3, SS4, PB1 and PB2 for A B C D E and F respectively. Remove jumpers.



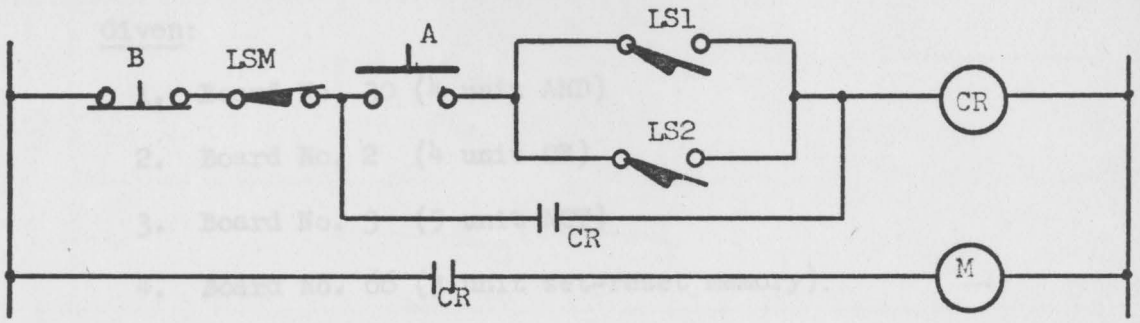
Relay Circuit



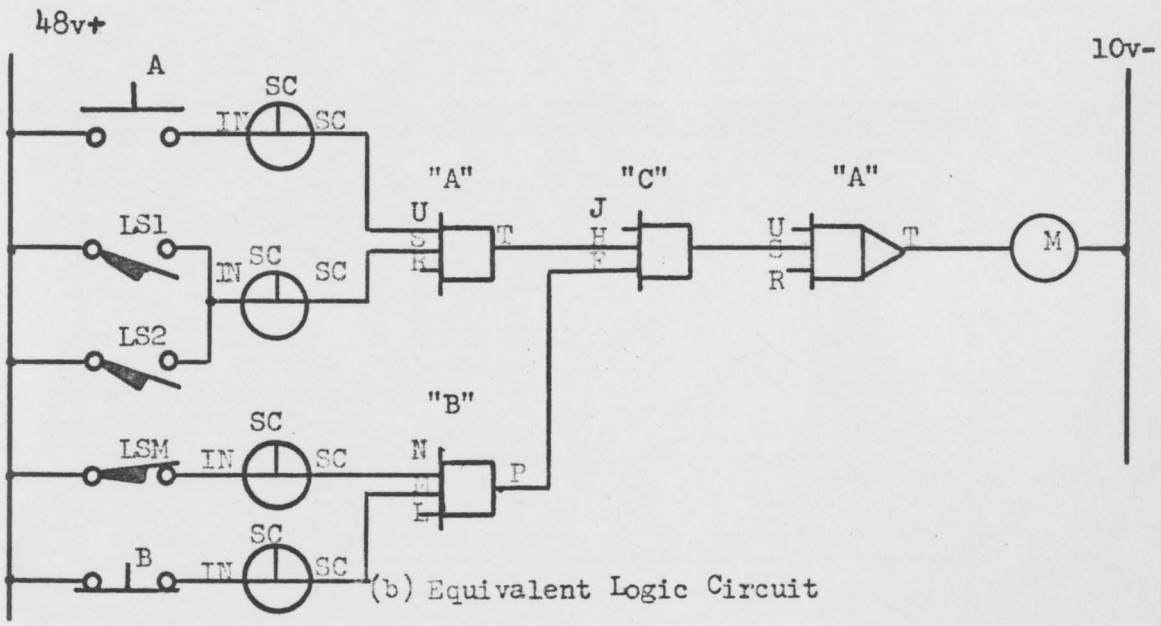
Equivalent Logic Circuit

5. Compare the relay circuit and the equivalent conventional logic circuit. Wire up the logic circuit and compare its operation to the relay circuit. Refer to Figure 25.

Caution: Have instructor check out the circuit before turning on the power. It is very important that you don't apply 48 volts to any logic gates. The 48v + bus should go through the selector switches and pushbuttons and only to the in terminal of the signal converters. Remember that any unused inputs of AND gates must be connected to 10v + bus.



(a) Relay Circuit



(b) Equivalent Logic Circuit

FIG. 25.--RELAY AND STATIC LOGIC COMPARISON NO. 1

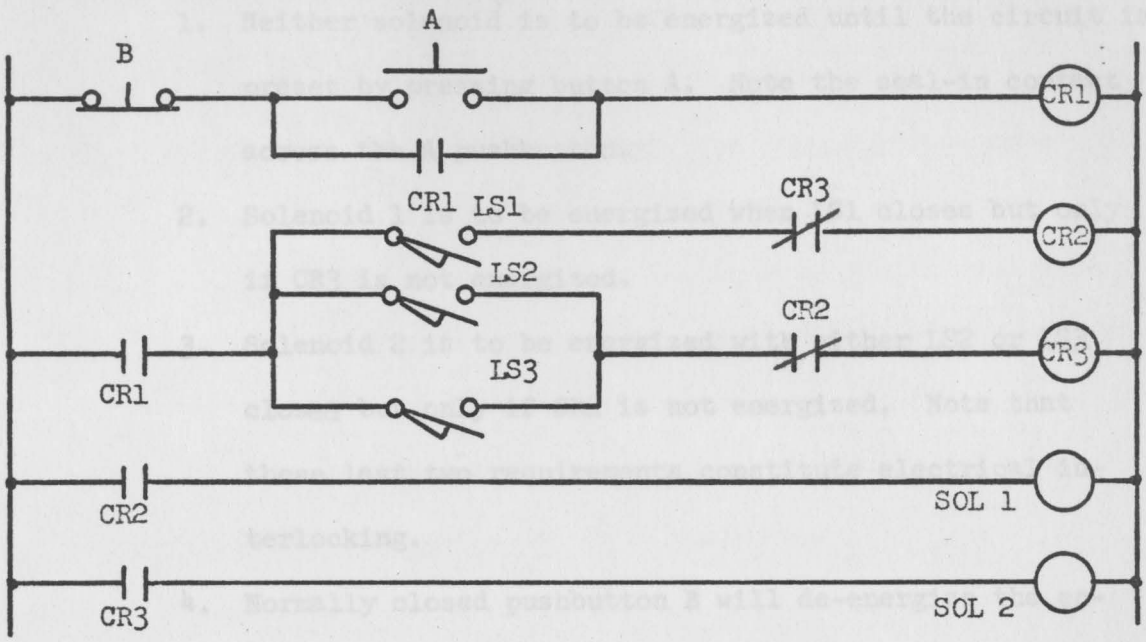
Experiment 8 (A DSL Logic Circuit)

Object:

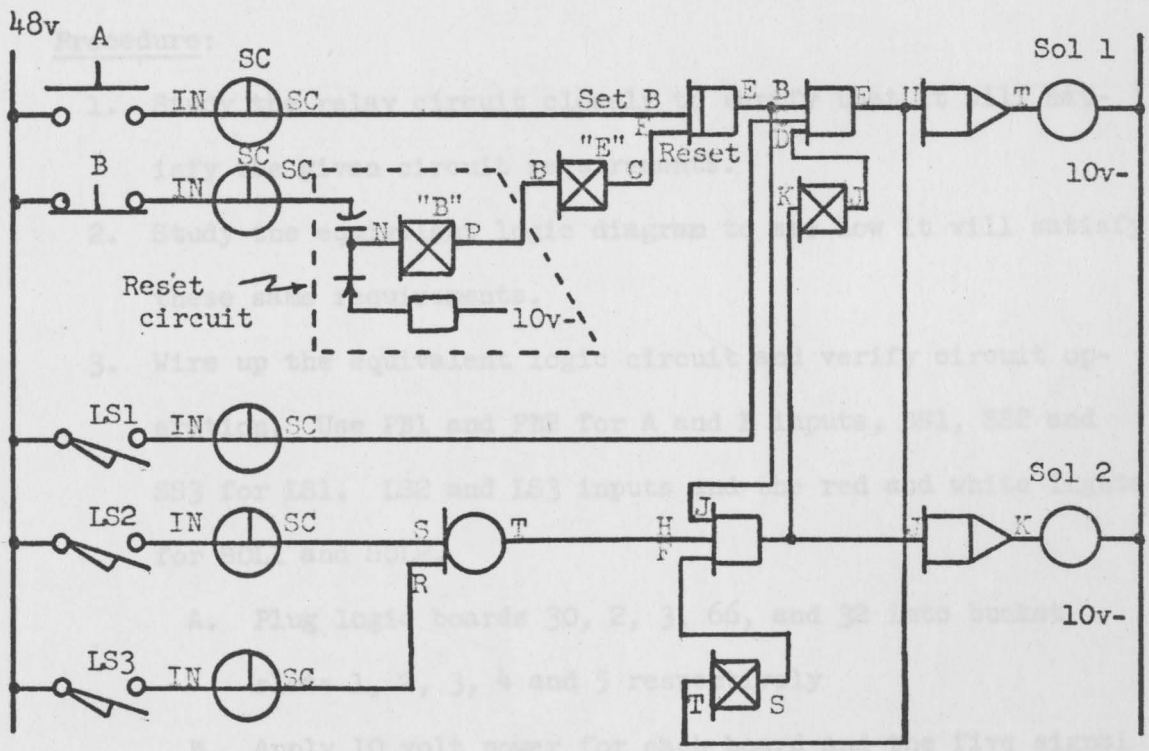
This experiment will give a comparison of relay circuitry and equivalent DSL logic circuitry.

Given:

1. Board No. 30 (4 unit AND)
2. Board No. 2 (4 unit OR)
3. Board No. 3 (5 unit NOT)
4. Board No. 66 (3 unit set-reset memory)
5. Board No. 32 (4 unit 10v power AND)
6. Relay circuit and circuit requirements
7. Corresponding logic circuit to satisfy same requirements. Refer to Figure 26.



(a) Relay Circuit



(b) Equivalent Logic Circuit

FIG. 26.--RELAY AND STATIC LOGIC COMPARISON NO. 2

Circuit requirements

1. Neither solenoid is to be energized until the circuit is preset by pressing button A. Note the seal-in contact across the A pushbutton.
2. Solenoid 1 is to be energized when LS1 closes but only if CR3 is not energized.
3. Solenoid 2 is to be energized with either LS2 or LS3 closed but only if CR2 is not energized. Note that these last two requirements constitute electrical interlocking.
4. Normally closed pushbutton B will de-energize the entire circuit and before any relays or solenoids can be energized A button will have to be depressed.

Procedure:

1. Study the relay circuit closely to verify that it will satisfy the given circuit requirements.
2. Study the equivalent logic diagram to see how it will satisfy these same requirements.
3. Wire up the equivalent logic circuit and verify circuit operation. Use PB1 and PB2 for A and B inputs, SS1, SS2 and SS3 for LS1. LS2 and LS3 inputs and the red and white lights for SOL1 and SOL2.
   A. Plug logic boards 30, 2, 3, 66, and 32 into bucket slots 1, 2, 3, 4 and 5 respectively
   B. Apply 10 volt power for each board and the five signal converters by jumpering from the 10v+ and from the 10v- bus to each board or converter on the interconnection

plug board.

C. Wire from the 48v+ bus through the selector switches and push buttons to the signal converters. Note: This is the only place the 48v + bus should be connected. It is very important that 48 volts are not applied to any logic gates. Follow the diagram closely and wire up the rest of the circuit. Note also that any unused AND gate inputs must be connected to the 10v + bus. Be sure the instructor checks your circuit before you apply power.

CHAPTER IV

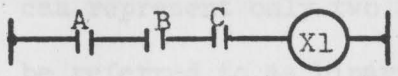
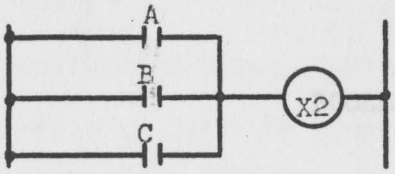
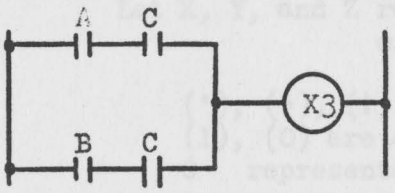
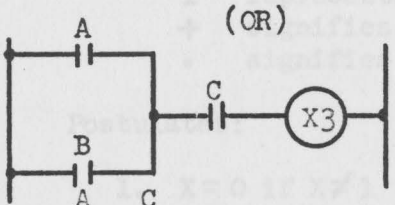
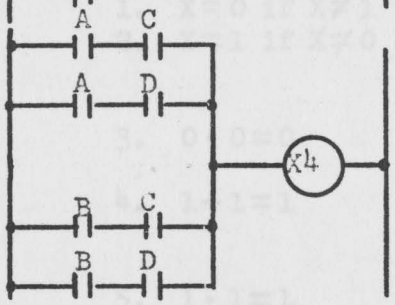
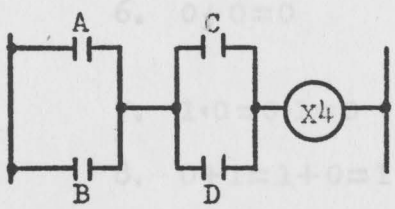
ADDITIONAL THEORY

Boolean Algebra

Any given contact circuit can be represented by an equation or in word form. Having any one of the three the other two can be obtained at will. The following table illustrates this for switching variables A, B, C, . . . and relays X1, X2, X3, . . .

TABLE 3

THE BOOLEAN STRUCTURE

Circuit Form	Equation Form	Word Form
	X1 = A·B·C	X1 will be energized if A AND B AND C are closed.
	X2 = A+B+C	X2 will be energized if A OR B OR C is closed
	X3 = AC + BC	X3 will be energized if A AND C are closed OR if B AND C are closed
(OR)	(OR)	(OR)
	X3 = (A+B) C	X3 will be energized if A OR B AND C are closed
	X4 = AC+AD+BC+BD	X4 will be energized if A AND C, OR A AND D, OR B AND C, OR B AND D are closed.
(OR)	(OR)	(OR)
	X4 = (A+B) (C+D)	X4 will be energized if A OR B, and C OR D are closed

Some of the basic definitions, postulates and theorems of Boolean Algebra are summarized in Tables 4 and 5.[1]

The switching variables are two valued in the sense that they can represent only two states of operation. For this reason they can be referred to as binary variables.

TABLE 4

BOOLEAN DEFINITIONS AND POSTULATES

Definitions:

Let X, Y, and Z represent circuit variables such as switches or relay contacts

(′), (•), (+) are prime, dot, and plus operators
(1), (0) are digits representing states of inputs or outputs
0 represents an open circuit
1 represents a closed circuit
+ signifies a parallel connection
• signifies a series connection

Postulates:

1.	$X=0$ if $X\neq 1$	Shows that switching variables are actually binary variables and that at any given time either $X=0$ or $X=1$.
2.	$X=1$ if $X\neq 0$	
3.	$0\cdot 0=0$	An open circuit in series with an open circuit is an open circuit.
4.	$1+1=1$	A closed circuit in parallel with a closed circuit is a closed circuit.
5.	$1\cdot 1=1$	A closed circuit in series with a closed circuit is a closed circuit.
6.	$0+0=0$	An open circuit in parallel with an open circuit is an open circuit.
7.	$1\cdot 0=0\cdot 1=0$	A closed circuit in series with an open circuit in either order is an open circuit.
8.	$0+1=1+0=1$	An open circuit in parallel with a closed circuit in either order is a closed circuit.
9.	$0'=1$	The opposite of the 0 state is the 1 state.
10.	$1'=0$	The opposite of the 1 state is the 0 state.

[1]Claude E. Shannon, "A Symbolic Analysis of Relay and Switching Circuits." AIEE Transactions. 1938. Vol.57, p. 713.

It should be noted that duality relationships exist between postulates 3 and 4, between 5 and 6, and between 7 and 8. That is if each 1 digit in postulate 4 is changed to a 0 digit and the (+) operator is changed to the (•) operator we obtain postulate 3 and likewise if every 0 digit in postulate 3 is changed to a 1 digit and the (•) operator is changed to (+) operator we obtain postulate 4. Postulates 9 and 10 introduce negation or complementation. We can refer to 0 as the complement of 1 or we can refer to 1 as the complement of 0.

TABLE 5

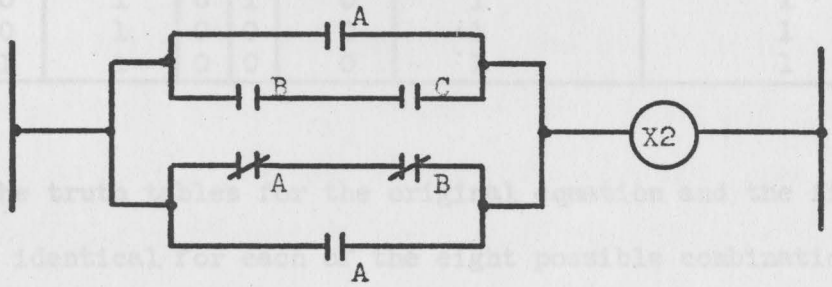
BOOLEAN THEOREMS

1.	$X+Y=Y+X$	
2.	$X \cdot Y=Y \cdot X$	
3.	$X+(Y+Z)=(X+Y)+Z=X+Y+Z$	Associative Laws - parenthesis may be omitted in a sum or product of several terms.
4.	$X \cdot (Y \cdot Z)=(X \cdot Y) \cdot Z=X \cdot Y \cdot Z$	
5.	$X \cdot (Y+Z)=X \cdot Y+X \cdot Z$	Distributive laws - can multiply out products and factor sums.
6.	$X+(Y \cdot Z)=(X+Y)(X+Z)$	
7.	$1 \cdot X=X$	
8.	$0+X=X$	
9.	$1+X=1$	
10.	$0 \cdot X=0$	
11.	$X+X'=1$	
12.	$X \cdot X'=0$	
13.	$X+X=X$	
14.	$X \cdot X=X$	
15.	$(X)'=X'$	
16.	$(X')'=X$	
17.	$X+XY=X$	
18.	$X \cdot (X+Y)=X$	
19.	$(X+Y')\ Y=XY$	
20.	$XY'+Y=X+Y$	
21.	$(X+Y)\ (Y+Z)(Z+X')=(X+Y)(Z+X')$	
22.	$XY+YZ+ZX'=XY+ZX'$	
23.	$(X+Y+Z+\ldots)'=X'Y'Z' \ldots.$	
24.	$(X \cdot Y \cdot Z \cdot \ldots)'=X'+Y'+Z'+\ldots$	
25.	$(X+Y)\ (X'+Z)=XZ+X'Y$	

Some time should be spent to visualize each of the postulates and theorems in terms of contact circuitry to try to justify each equality. Each of the paired duality relationships in tables 4 and 5 should also be studied to better understand the duality concept.

The following example illustrates the application of theorems in simplifying or reducing the algebraic equations. The (') prime signifies a normally closed contact and is similar to the NOT function of the previous chapter. Thus —|| B' = —//— B .

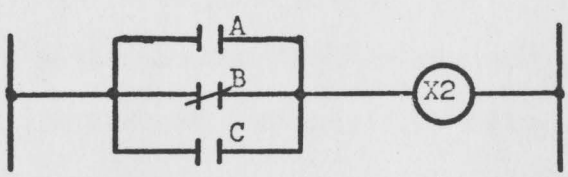
B' might also be represented by $\bar{B}$ meaning NOT B.



Algebraic Representation and Reduction:

$X2 = [A+(B\cdot C)] + [(A'\cdot B') + A]$	
$X2 = [A+(B\cdot C)] + [(A+A')\ (A+B')]$	By Theorem 6
$X2 = [A+(B\cdot C)] + [(1)\ (A+B')]$	By Theorem 11
$X2 = [A+(B\cdot C)] + [A+B']$	By Theorem 7
$X2 = A+B\cdot C+A+B'$	By Theorems 3 & 4
$X2 = A+B\cdot C+B'$	By Theorem 13
$X2 = A+(B'+B)\ (B'+C)$	By Theorem 6
$X2 = A+(1)\ (B'+C)$	By Theorem 11
$X2 = A+B'+C$	By Theorem 7

Resulting Equivalent Circuit:



Proof of Equivalence:

Inputs A B C	B•C	A+(B•C)	A'	B'	A'• B'	A+ (A'• B')	Original Equation	Final Equation
0 0 0	0	0	1	1	1	1	1	1
0 0 1	0	0	1	1	1	1	1	1
0 1 0	0	0	1	0	0	0	0	0
0 1 1	0	1	1	0	0	0	1	1
1 0 0	0	1	0	1	0	1	1	1
1 0 1	0	1	0	1	0	1	1	1
1 1 0	0	1	0	0	0	1	1	1
1 1 1	1	1	0	0	0	1	1	1

The truth tables for the original equation and the final equation are identical for each of the eight possible combinations of inputs assuring the equivalence of the two circuits.

Some working knowledge of truth tables can be gained by setting up truth tables for each side of the equality sign for some of the Theorems stated in Table 5. It should be noted that there are 2^N possible combinations of N input variables. In the above circuit simplification there are 3 input variables (A, B and C), thus the truth table had to consider 2^3 or 8 possible combinations of these three variables.

Conversions Between Conventional (Non-Inverting) and Inverting Logic

A brief circuit comparison between the non-inverting and the inverting type logic will now be made and we will complete this chapter with practice in making conversions between gates of various logic types.

Consider the circuit in Figure 27 that illustrates the non-inverting type logic. Transistor T2 will re-invert the output signal from the first transistor (T1) thereby restoring similarity with the input signal. Since the output signal looks like the input signal the circuit is called non-inverting logic.

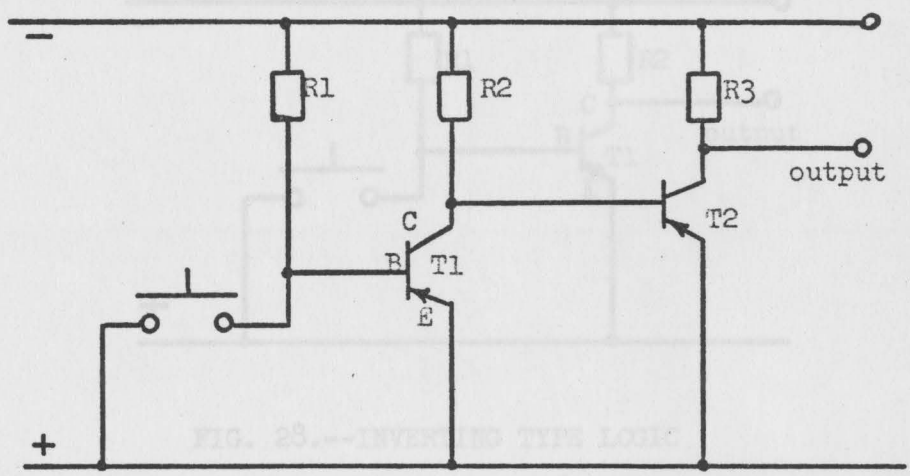


FIG. 27.--NON-INVERTING LOGIC CIRCUIT

With the push button open transistor T1 is forward biased and base current flows from the + bus through T1 (E to B) and through R1 to the − bus. T1 while conducting acts like a closed switch (E to C). With T1 conducting the base of T2 is at the same potential as the emitter and T2 will not conduct. T2 acts like an open switch (E to C) and there will be no output signal across R3.

When the push button is closed T1 does not conduct and acts like an open circuit (E to C) since its base and emitter are at the same potential. This places a negative voltage on the base of T2 through R2, forward biasing T2 causing it to conduct. T2 will draw base current and act like a short circuit (closed switch E to C) and 10 volts will appear across output load resistor R3.

Thus with the non-inverting circuit with no input (PB open) there is no output (0 volts across R3). When there is an input (PB closed) there is an output (10 volts across R3). Figure 28 illustrates the inverting type logic.

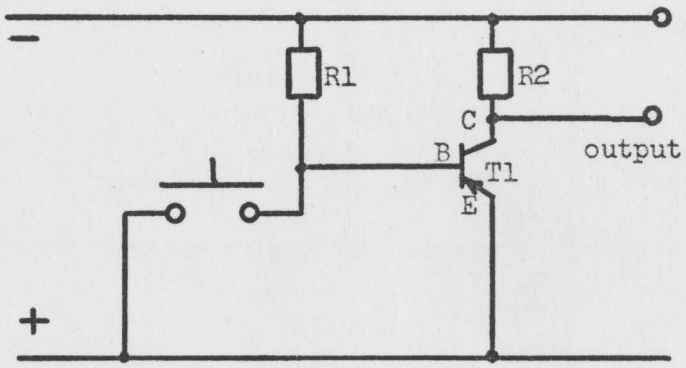


FIG. 28.--INVERTING TYPE LOGIC

With the push button open T1 is forward biased and base current flows from the + bus through T1 (E to B) and through R1 to the negative bus. When T1 conducts it acts like a short circuit (closed switch) E to C and 10 volts appears across output resistor R2.

With the push button closed T1 cannot conduct since the base and emitter are at the same potential. T1 acts like an open switch E to C and no voltage appears across output resistor R2.

Thus with the inverting circuit with no input (PB open) there is an output (10 volts across R2). With an input (PB closed) there is no output (0 volts across R2).

Conversions Between Conventional and Inverting Logic

Since the major suppliers of electrical equipment might utilize either or both types of logic systems, it becomes important to be able to convert circuitry from one system to another. Also, since required logic gates might have to be constructed from other available logic gates, it becomes important to be able to convert from one gate to another.

Figure 29 presents a simplified method for converting from one logic gate to another by adding inverters to inputs and/or output.

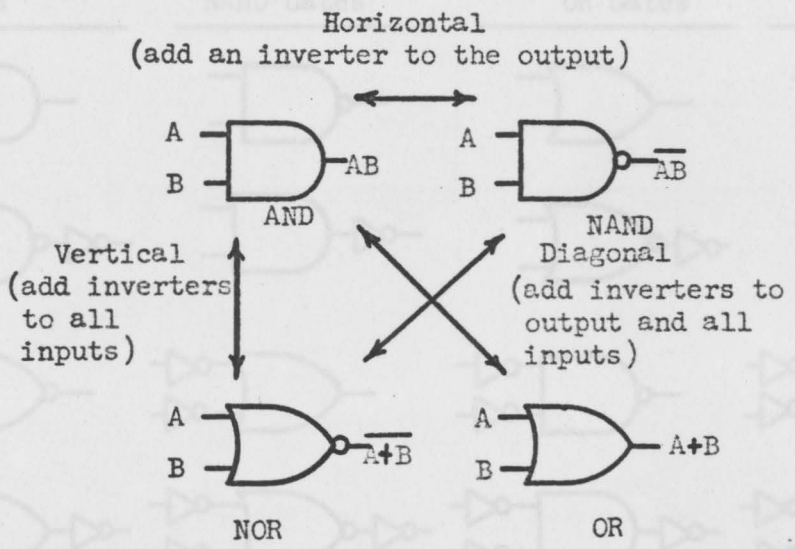


FIG. 29.--GATE CONVERSION METHOD[2]

It should be noted that small circles encountered in the outputs or inputs of inverting logic symbols signify inverters. This can be noticed in the NAND and the NOR gates in Figure 29. We can say that the NAND is an AND with an inverter in its output. We can also say

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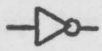
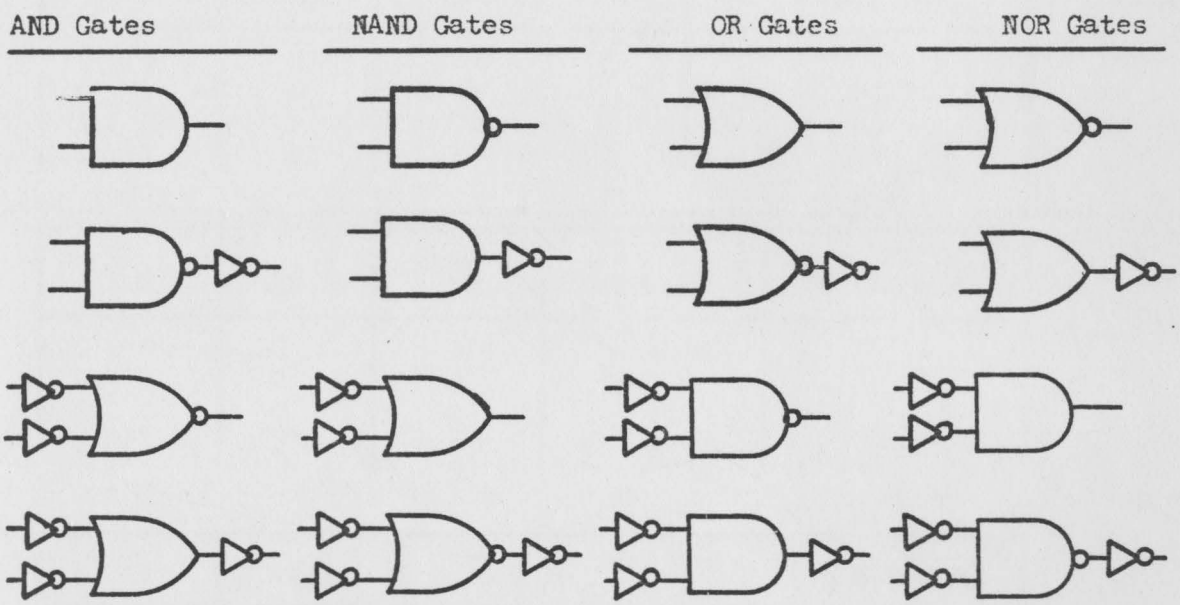
[2]Technical Staff, Practical Applications of Digital Integrated Circuits (Northfield, Ohio: General Electronics Associates, Inc., 1972),

that the NOR is an OR with an inverter in its output. The symbol  also represents an inverter. Placing inverters in series with the input leads of an OR make it act like a NAND, and placing inverters in series with the input leads of an AND makes it act like a NOR gate. Two inverters in series cancel each other and may be eliminated.

To better understand the given conversion method verify each entry in Table 6.

TABLE 6

GATE CONVERSIONS



The final aim of this chapter is to present the exclusive OR and utilize it to compare conventional (non-inverting) circuitry and inverting circuitry. More will be said about the exclusive OR in the next chapter. The exclusive OR will produce a 1 if only one of its inputs (an odd number) is 1 but not if both inputs (an even number)

are 1. Consider this function in Table 7 which is a truth table summary for the gates we have studied.

TABLE 7

GATE TRUTH TABLE SUMMARY

Inputs A	Inputs B	AND	OR	NAND	NOR	Exclusive OR
0	0	0	0	1	1	0
0	1	0	1	1	0	1
1	0	0	1	1	0	1
1	1	1	1	0	0	0

Four ways that the exclusive OR can be represented algebraically as seen by the equivalence of the column with the asterisk (*) are $(A+B)(\overline{AB})$, $A\bar{B}+\bar{A}B$, $\overline{AB+\bar{A}\bar{B}}$, and $(A+B)(\bar{A}+\bar{B})$.

TABLE 8

EXCLUSIVE OR TRUTH TABLES

A	B	A+B	AB	$\overline{AB}$	$(A+B)(\overline{AB})$ *
0	0	0	0	1	0
0	1	1	0	1	1
1	0	1	0	1	1
1	1	1	1	0	0

A	B	$A\bar{B}$	$\bar{A}B$	$A\bar{B}+\bar{A}B$ *
0	0	0	0	0
0	1	0	1	1
1	0	1	0	1
1	1	0	0	0

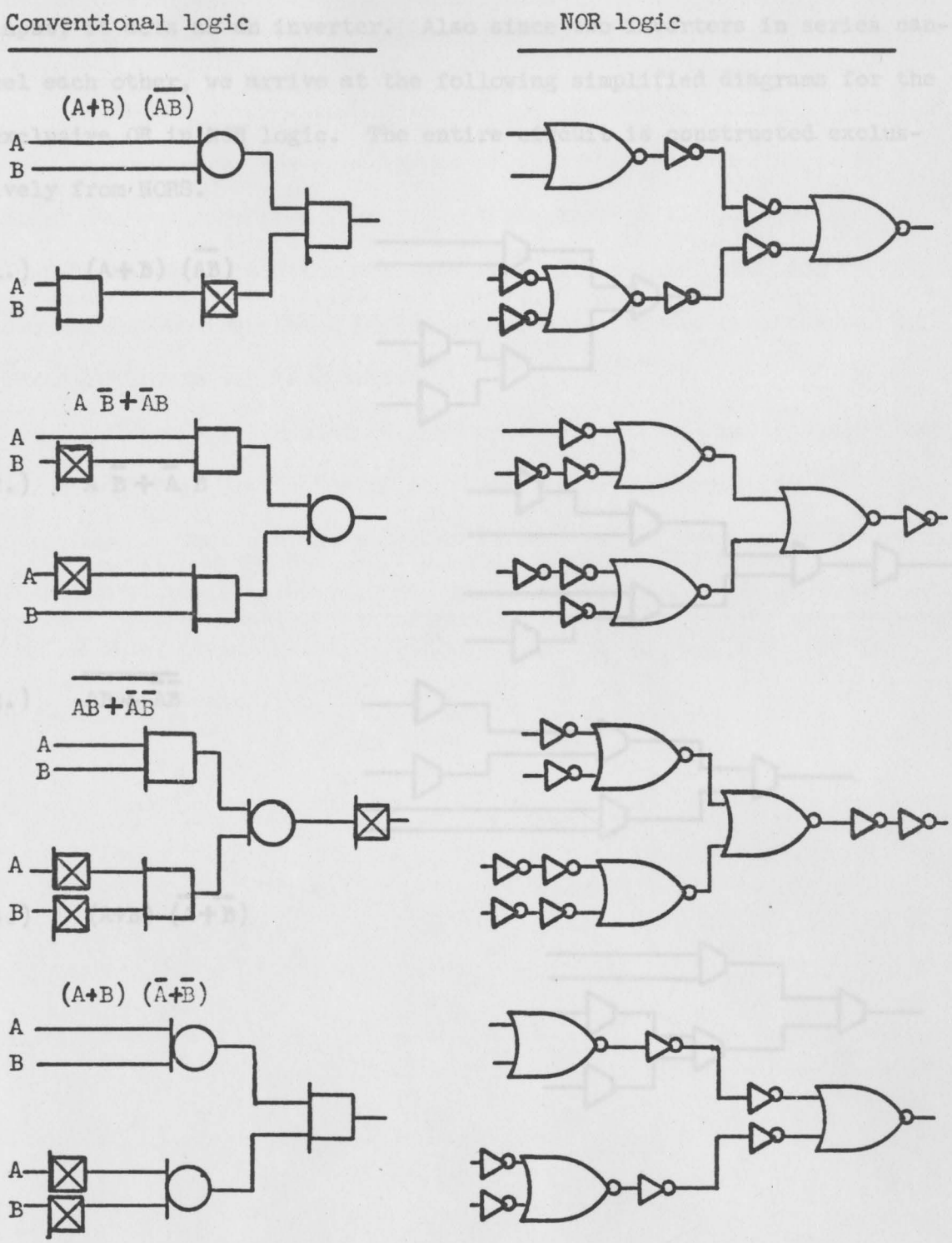
A	B	AB	$\bar{\bar{A}}\bar{\bar{B}}$	$AB+\bar{\bar{A}}\bar{\bar{B}}$	$\overline{AB+\bar{\bar{A}}\bar{\bar{B}}}$ *
0	0	0	1	1	0
0	1	0	0	0	1
1	0	0	0	0	1
1	1	1	0	1	0

A	B	A+B	$\bar{A}+\bar{B}$	$(A+B)(\bar{A}+\bar{B})$ *
0	0	0	1	0
0	1	1	1	1
1	0	1	1	1
1	1	1	0	0

The conventional logic diagrams have been drawn in Table 9 for each of these equivalent exclusive OR forms, as well as an equivalent inverting logic diagram using only NOR elements and inverters.

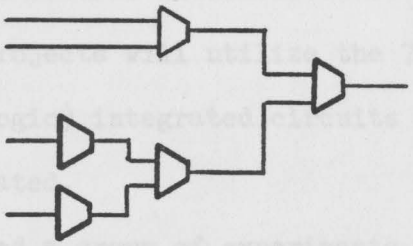
TABLE 9

EXCLUSIVE OR DIAGRAMS

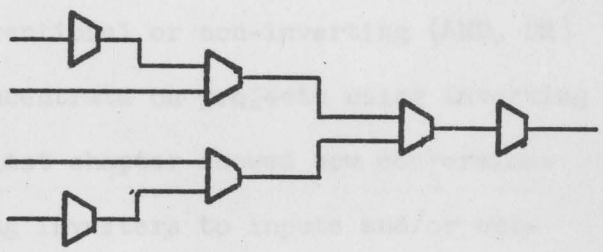


In NOR logic as used with Westinghouse (Prodac) that will be covered in Chapter VI, the symbol  is used to represent a NOR. If the inputs of a NOR are shorted together to make a single input, it acts as an inverter. Also since two inverters in series cancel each other, we arrive at the following simplified diagrams for the exclusive OR in NOR logic. The entire circuit is constructed exclusively from NORS.

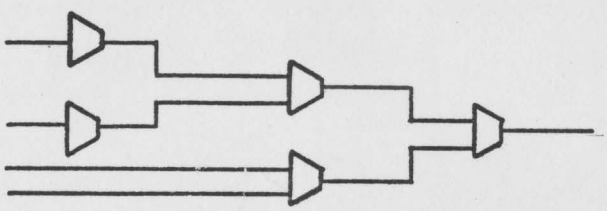
1.) $(A+B)\,(\overline{AB})$



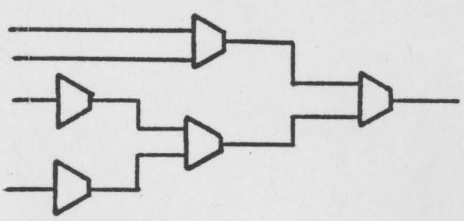
2.) $A\,\overline{B} + \overline{A}\,B$



3.) $\overline{\overline{AB} + \overline{\overline{AB}}}$



4.) $(A+B)\,(\overline{A}+\overline{B})$



CHAPTER V

TTL (TEXAS INSTRUMENTS) INVERTING LOGIC TUTOR

Figure 30 is a photograph of the laboratory equipment to be used in completing the experiments of this chapter. The Digi-Kit Midel 200 was purchased from General Electronics Associates, Inc., Northfield, Ohio, and the projects will utilize the 7400 line of TTL (Transistor to Transistor Logic) integrated circuits manufactured by Texas Instruments, Incorporated.

Chapter III contained a group of experiments using Cutler Hammer DSL (Direct Static Logic) conventional or non-inverting (AND, OR) type logic. This chapter will concentrate on projects using inverting (NAND, NOR) logic hardware. The last chapter showed how conversions can be made between gates by adding inverters to inputs and/or outputs of other gates.

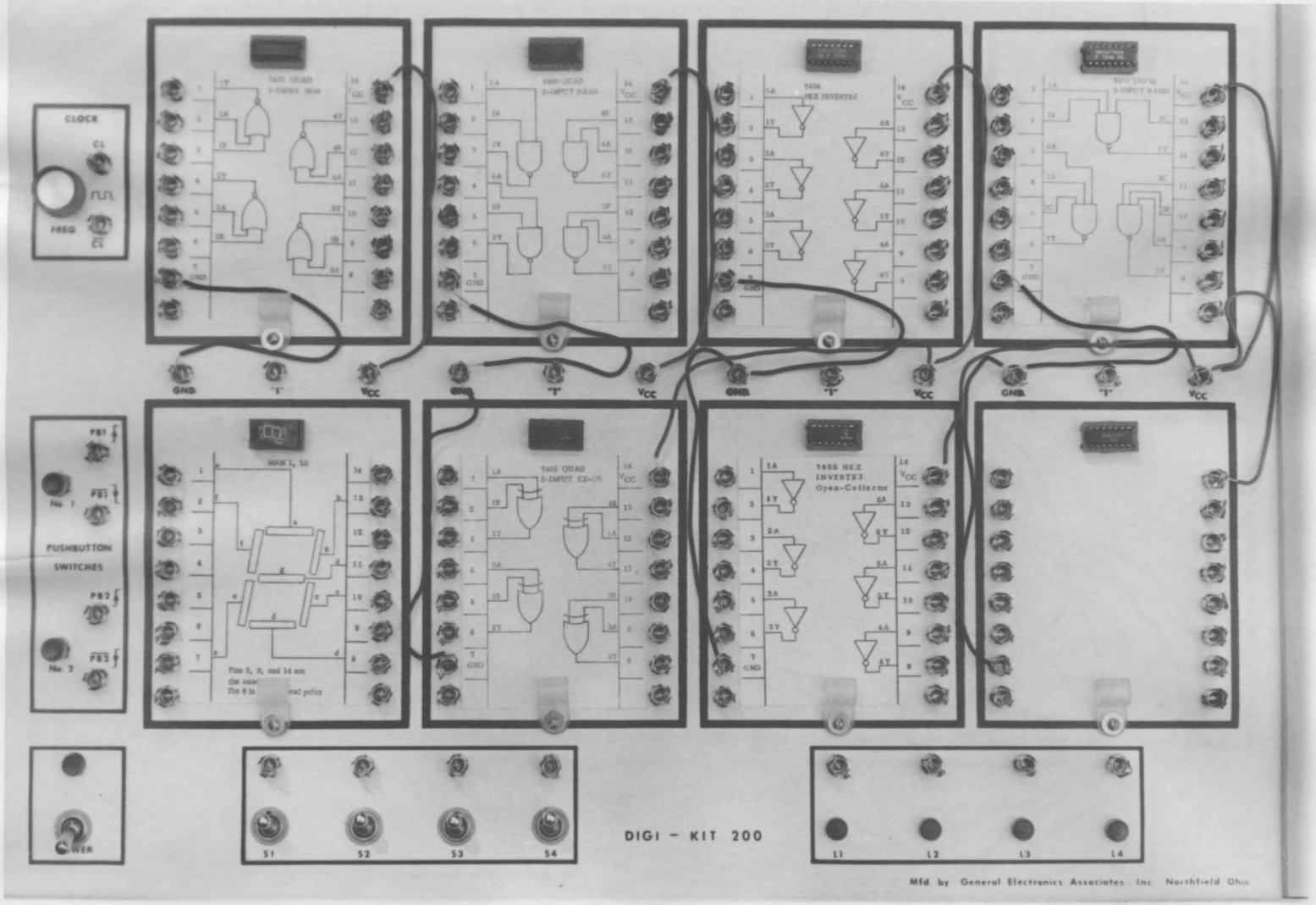


FIG. 30.--TTL DIGI-KIT TUTOR

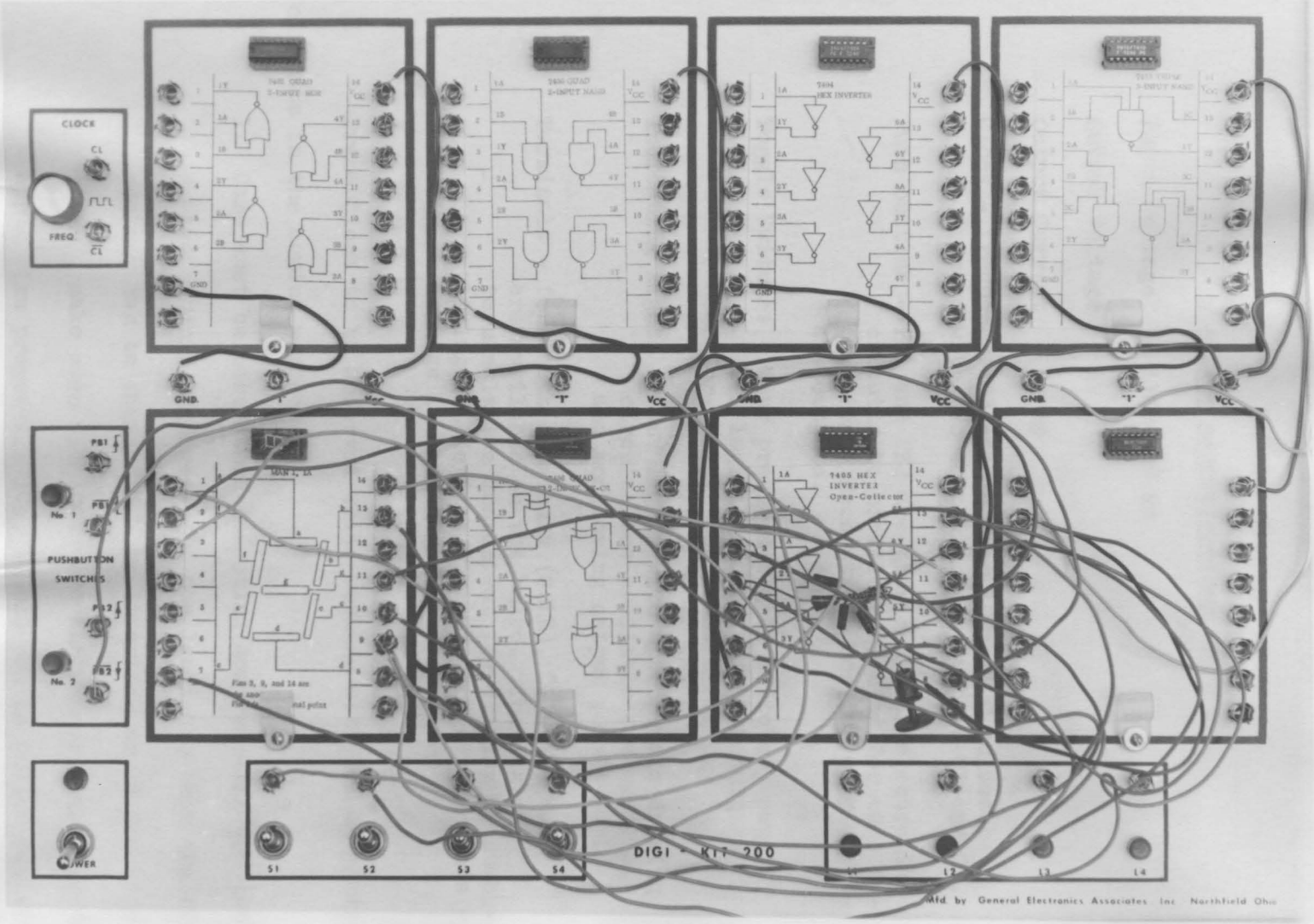


FIG. 31.--TTL DIGI-KIT TUTOR WIRED

Pertinent Digi-Kit specifications are summarized below, as are a few precautions and pointers that need to be kept in mind while experimenting with this equipment.

TABLE 10

DIGI-KIT SPECIFICATIONS

Input Voltage - 110v 60 Hz

Output Voltage - 5v

Output Current - 1 amp

Clock - frequency adjustable from 10 to 200 pulses per second with two complementary outputs CL and $\overline{CL}$.

Push buttons - PB1 and PB2 are prewired with electronic circuits to provide one pulse for each depression. Each switch has two complementary outputs.

Toggle Switches - four prewired toggle switches, supply TTL logical 1 and logical 0 outputs for gating functions.

Indicating lights - four lights with appropriate driving circuits are available for testing, and monitoring output points.

Terminals - four sets of ground (GND), "1", and Vcc are available on the board. The logical "1" terminals are convenient for driving or stabilizing TTL devices without damage since this voltage is limited to a safe value.

Precautions to be observed while working with TTL integrated circuits in the coming projects.

1. Care must be taken when inserting and removing the integrated circuit packages. If the leads are bent the IC sockets can be damaged. When inserting an IC into its socket, make sure all leads are aligned properly and then apply firm pressure. ICs should not be pulled out with

your fingers. Use an extractor or a small screwdriver and be careful.

2. A small etched marking on top of the IC or small notch at one end indicates the location of pin #1. If the IC is held with the notch to the left and the pin tips pointing downward, #1 pin will be toward you to the left. Pin #1 goes into the socket corner that is rounded off. In our case the notched IC end goes to the far left of the socket.
3. There are paper overlay cards that are placed directly below the IC and between terminals. These cards identify the various inputs and outputs of the IC.
4. The IC cards are provided with 5v power by connecting ground terminal of the IC to the ground bus and Vcc terminal of the IC to Vcc bus. These must be connected for each IC package. Position these power feed leads so that they will stay in place and do not need to be disconnected in going from one experiment to the next.
5. If at all in doubt about the circuitry, have an instructor check it out before applying power. Be sure to turn power off when making or breaking connections.

Experiment 1 (The Basic Logic Gates)

Object:

This experiment is to familiarize you with the tutor that will be used in the coming experiments and to review the basic logic gates.

Given:

1. Digi-Kit 200 and jumper leads.
2. Quad 2 input NOR (7402) and associated overlay
3. Quad 2 input NAND (7400) and associated overlay
4. Hex Inverter (7404) and associated overlay
5. Table of 5 basic gates

Procedure:

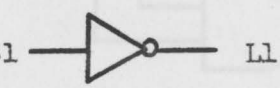
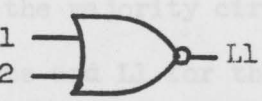
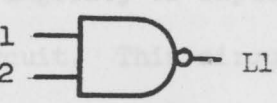
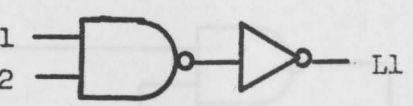
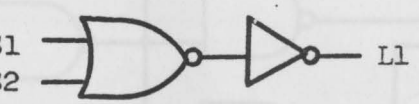
1. Jumper from S1 toggle switch to L1, from S2 to L2, from S3 to L3 and from S4 to L4. As each of the respective toggle switches is closed, observe lights. Remove jumpers.
2. Jumper from each of the four "1" terminals to the four indicating lights and verify "1" terminal outputs. Remove jumpers.
3. Jumper from PB1, $\overline{PB1}$, PB2, and $\overline{PB2}$ to L1, L2, L3, and L4 respectively. Notice that the two indicating lights supplied from $\overline{PB1}$ and $\overline{PB2}$ are on similating normally closed contacts on the pushbuttons. Depress PB1 and note that L1 goes on as L2 goes off. Depress PB2 and note that L3 goes on and L4 goes out. The outputs of each push button has complimentary outputs. Outputs PB1 and PB2 will deliver a positive going pulse when their respective buttons are depressed, and conversely outputs $\overline{PB1}$ and $\overline{PB2}$ will deliver a negative going pulse when their respective buttons are depressed. Remove

jumpers.

4. Jumper from clock terminal CL to L1 and from clock terminal CL to L2. Adjust frequency for lowest value and note complimentary. The clock serves as a pulse generator to provide a series of pulses for driving counters, shift registers, and other sequential circuits. Note the effect as the frequency is increased. Remove jumpers.
5. Wire up and verify the operation of each of the five basic gates given in Table No. 11, and complete the truth tables for the output (L1) of each of these five basic gates.

TABLE 11

BASIC GATES WITH TTL

Gate	IC No.	Circuit	Truth Tables
Inverter	7404		S1 | L1 0 1
NOR	7402		S1 S2 | L1 0 0 0 1 1 0 1 1
NAND	7400		S1 S2 | L1 0 0 0 1 1 0 1 1
AND	7400 7404		S1 S2 | L1 0 0 0 1 1 0 1 1
OR	7402 7404		S1 S2 | L1 0 0 0 1 1 0 1 1

Experiment 2 (Interconnecting Logic Gates)

Object:

Practice interconnecting various integrated circuits will be accomplished in this experiment by wiring up three special circuits and verifying their operation.

Given:

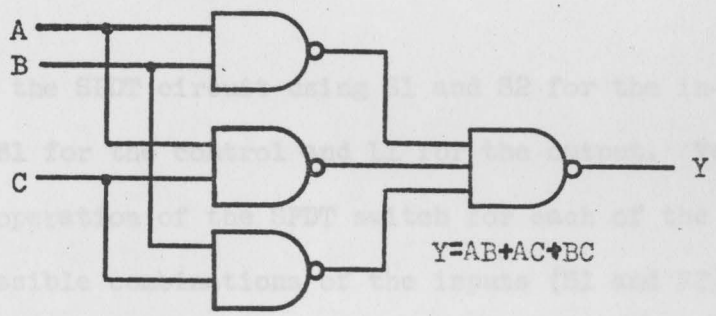
Quad 2 input NAND

Triple 3 input NAND

Hex inverter

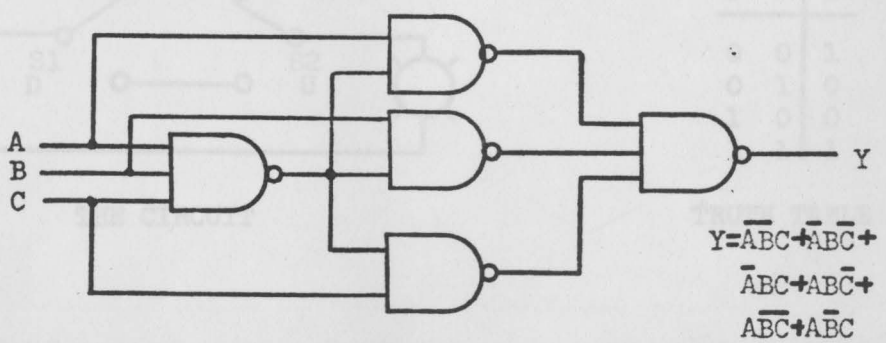
Procedure:

1. The majority circuit. This circuit will produce a state of one in the output when a majority of inputs are present.



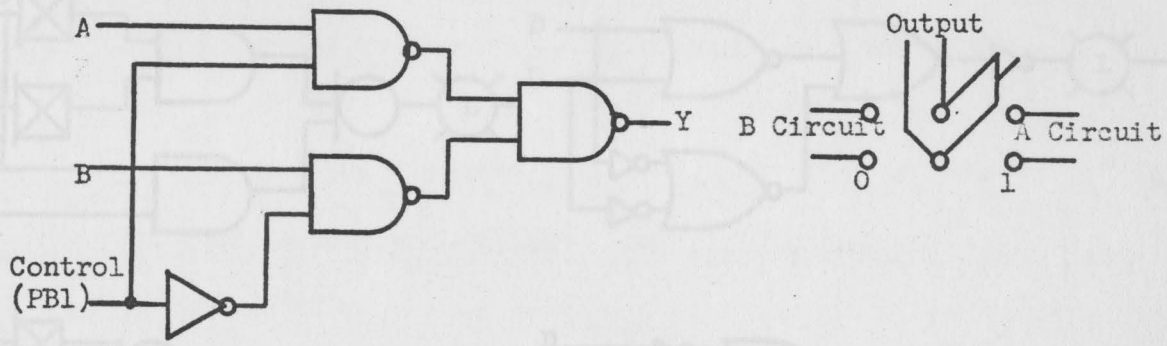
A. Wire up the majority circuit using S1, S2, and S3 for the inputs and L1 for the output. Verify the output and the majority of inputs idea. Remove jumpers.

2. The Dissent Circuit. This circuit will be in state one if all inputs do not agree (are not identical).



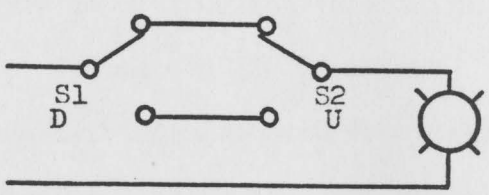
A. Wire up the dissent circuit using S1, S2, and S3 for the inputs and L1 for the output. Verify the output and the dissent idea. Remove jumpers.

3. The SPDT switch. When the control input is one, Y will assume the same state as A. When the control input is 0, Y will assume the same state as B.



A. Wire up the SPDT circuit using S1 and S2 for the inputs, PB1 for the control and L1 for the output. Verify the operation of the SPDT switch for each of the four possible combinations of the inputs (S1 and S2). Remove jumpers.

4. The three way switch to control hall lights by two switches one upstairs and one downstairs. By throwing either switch we wish to be able to change the light from "off" to "on" or from "on" to "off".



THE CIRCUIT

D	U	L
0	0	1
0	1	0
1	0	0
1	1	1

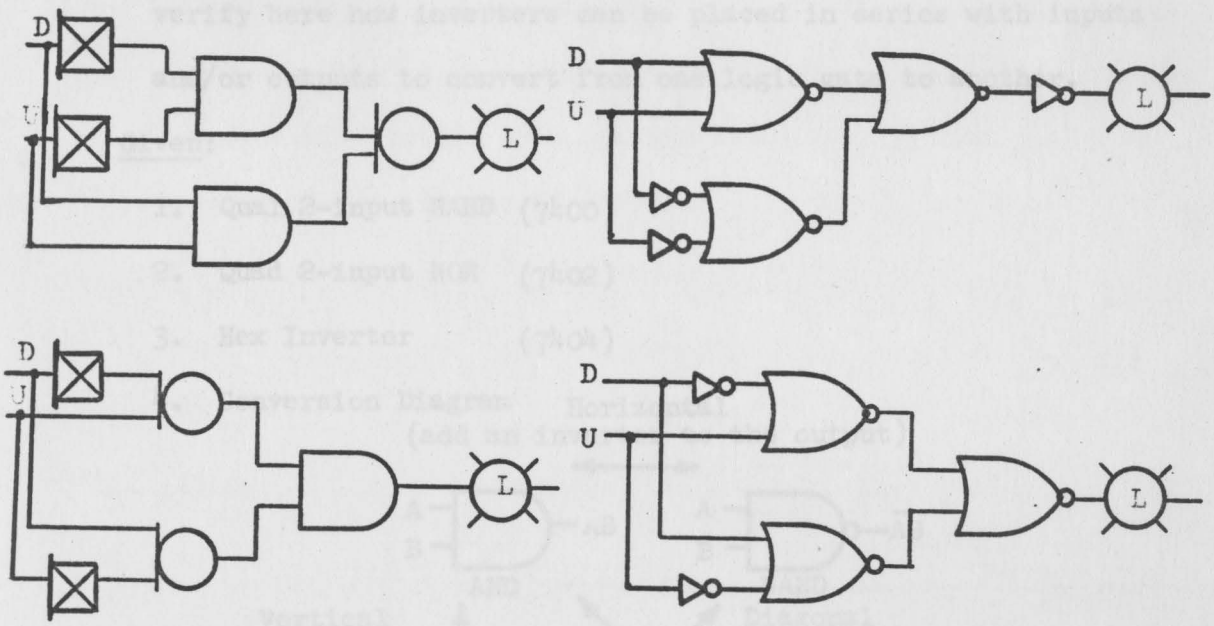
TRUTH TABLE

Two equations can be derived from the truth table.

$$(\bar{D} \cdot \bar{U}) + (D \cdot U) = L$$

$$(\bar{D} + U) \cdot (D + \bar{U}) = L$$

Conventional logic diagrams and inverting logic diagrams for these two equations are given below.



A. Wire up these two circuits using NOR gates and verify the truth table. Note these circuits are exclusive NOR circuits and will be further looked at in experiment 4.

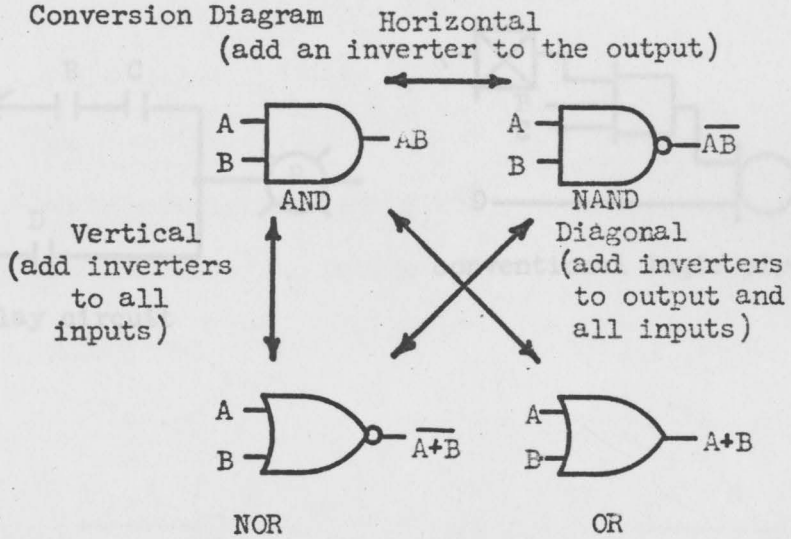
Experiment 3 (Conversions of Logic Gates)

Object:

Conversions between various logic gates is important for a proper understanding of the operation of the basic gates and for substitution purposes to get a desired gate from others available. We verify here how inverters can be placed in series with inputs and/or outputs to convert from one logic gate to another.

Given:

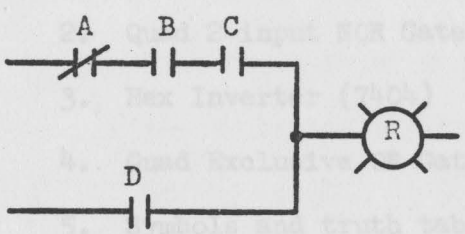
1. Qual 2-input NAND (7400)
2. Quad 2-input NOR (7402)
3. Hex Inverter (7404)
4. Conversion Diagram



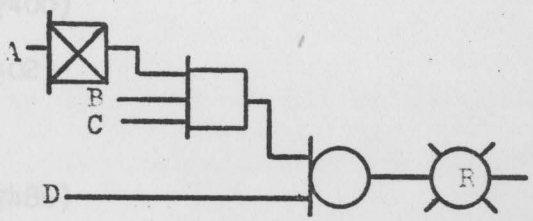
Procedure:

1. Construct an AND gate from a NAND gate using the given conversion diagram and verify its truth table. Use S1 and S2 for inputs and L1 for output. Remove jumpers.
2. Construct an AND gate from a NOR gate using the given conversion diagram and verify its truth table (proper output for all possible input combinations). Remove jumpers.

3. Construct an OR gate from a NAND gate and verify its truth table. Remove jumpers.
4. Construct an OR gate from a NOR gate and verify its truth table. Remove jumpers.
5. Given the following relay circuit and conventional logic circuit, convert the conventional logic to inverting logic employing three input NANDS and inverters. Wire up this circuit and verify results by comparing its output to what would be expected from the relay circuit.



relay circuit



conventional logic circuit

Experiment 4 (Exclusive OR and Exclusive NOR)

Object:

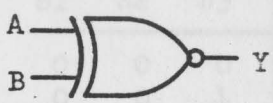
The exclusive OR and the exclusive NOR circuits will be wired up and their operation verified in this experiment. An important feature about the exclusive OR circuits is that they will respond only to an odd number of 1's applied to the input. The exclusive OR will produce a 1 if only one of its inputs (an odd number) is 1 but not if both inputs (an even number) are 1. The exclusive NOR circuit is called a comparator circuit gate or an odd parity circuit.

Given:

1. Quad 2-input NAND Gate (7400)
2. Quad 2-input NOR Gate (7402)
3. Hex Inverter (7404)
4. Quad Exclusive OR Gate (7486)
5. Symbols and truth tables

A	B	Y
0	0	0
0	1	1
1	0	1
1	1	0

Exclusive OR



A	B	Y
0	0	1
0	1	0
1	0	0
1	1	1

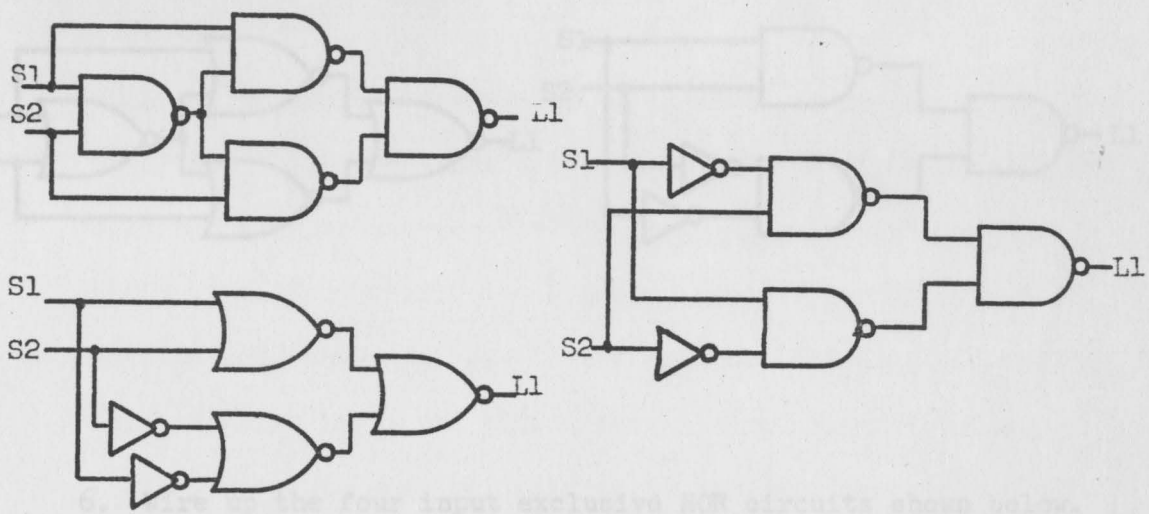
Exclusive NOR

Procedure:

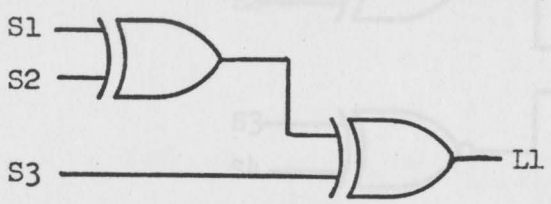
1. Wire up the exclusive OR gate using S1 and S2 as inputs and L1 as an output. Verify the truth table for all possible com-

binations of inputs. Remove jumpers.

2. Wire up each of the following exclusive OR circuits constructed from NANDS, NORS and inverters. Verify truth table for each circuit. Remove jumpers



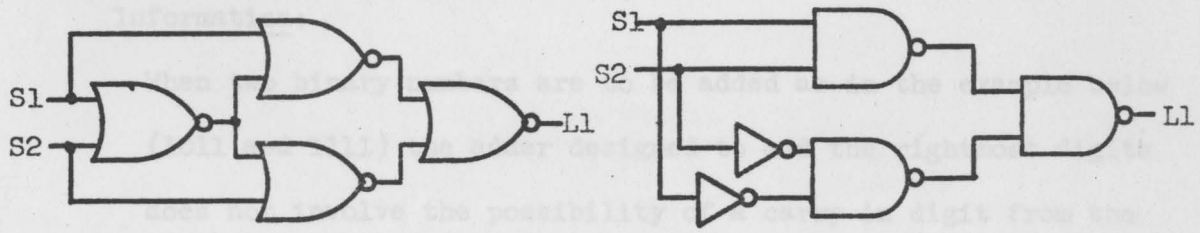
3. Wire the 3 input exclusive OR verify results and complete the truth table given for each combination of inputs. Remove jumpers.



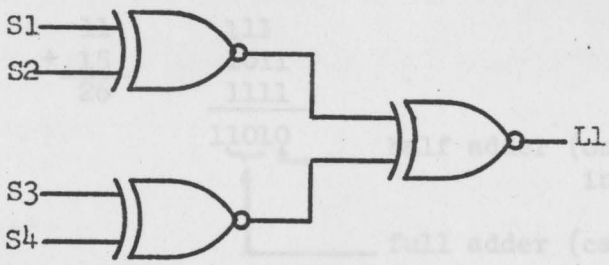
S1	S2	S3	L1
0	0	0	
0	0	1	
0	1	0	
1	0	0	
1	1	0	
1	0	1	
0	1	1	
1	1	1	

4. Using exclusive OR gates and inverters make an exclusive NOR gate. Use S1 and S2 as inputs and L1 as an output. Verify the truth table for all possible combinations of inputs. Remove jumpers.

5. Wire up the follcwing exclusive NOR circuits constructed from NANDS,NORS and inverters. Verify truth table for each circuit. Remove jumpers.



6. Wire up the four input exclusive NOR circuits shown below. This is called an odd bit parity detector. Verify output. Remove jumpers.



Experiment 5 (Half Adder and Full Adder)

Object:

The half adder and the full adder will be studied, wired up and operation verified in this experiment.

Information:

When two binary numbers are to be added as in the example below (1011 and 1111) the adder designed to add the rightmost digits does not involve the possibility of a carry-in digit from the right, therefore a half adder having simpler circuitry can be used to add these digits. As the columns of digits are added from right to left, the adders for all columns except the rightmost column must be designed to handle a carry-out digit. In these cases a full adder with more involved circuitry needs to be used.

Decimal	Binary
11	1011
+ 15	1111
26	11010

half adder (only carry-out involved)

full adder (carry-in and carry-out involved)

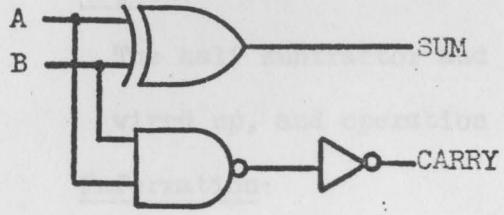
Given:

1. Quad Exclusive OR gate (7486)
2. Quad 2-input NAND gate (7400)
3. Hex Inverter (7404)

Procedure:

1. Wire up the half adder circuit shown and verify the truth table. Use S1 and S2 for inputs (A and B) and L1 and L2 for

outputs (S and Co).



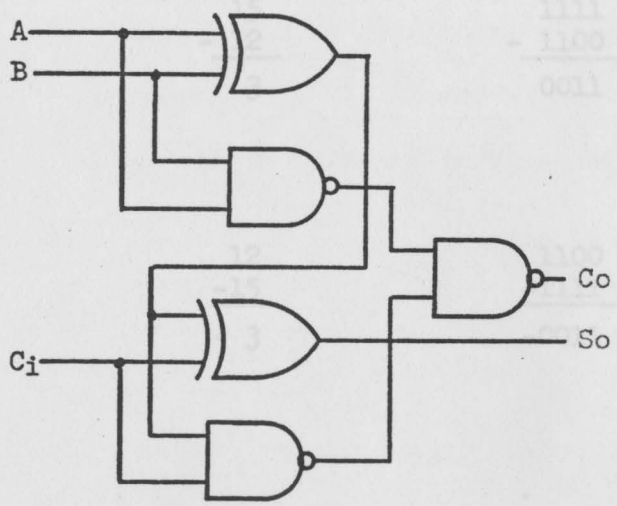
$S=\bar{A}B+A\bar{B}=A\oplus B$

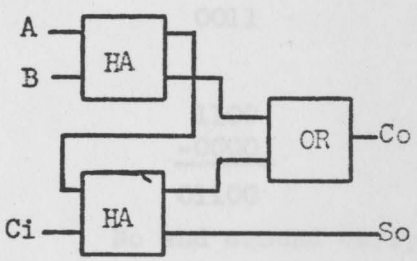
$Co=AB$

A B	Sum	Carry Out
0 0	0	0
0 1	1	0
1 1	0	1
1 0	1	0

Co A
B
S

2. Wire up a second half adder circuit and combine outputs through an OR gate to make the full adder circuit shown below. Use S1, S2 and S3 for inputs (A, B and Ci) and L1 and L2 for outputs (Sum and Carry out). Note half adder inverters were eliminated as were the inverters in OR gate inputs since two inverters in series cancel each other. Recall that an OR gate is a NAND gate with inverters in all inputs.





Experiment 6 (Half Subtractor and Full Subtractor

Object:

The half subtractor and the full subtractor will be studied, wired up, and operation verified in this experiment.

Information:

When two binary numbers are to be subtracted as in the examples below (1111 and 1100) the subtractor designed to subtract the rightmost digits does not involve the possibility of a borrow-in digit for digits to the right, therefore a half subtractor having simpler circuitry can be used to subtract these digits. As the columns of digits are subtracted from right to left the subtractors for all columns except the rightmost column must be designed to handle the possibility of a borrow-in digit for the column to its right and/or a borrow-out digit from the column to its left. In these cases a full subtractor with more involved circuitry needs to be used.

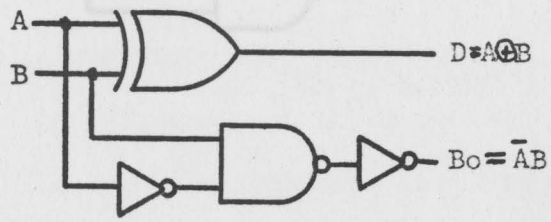
Decimal	Binary (Regular)	Binary (Compliment Method)
15	1111	1111
- 12	- 1100	- 0011
3	0011	10010
		1
		0011
12	1100	1100
-15	-1111	-0000
- 3	-0011	01100
		No end around carry
		∴ negate and complement to get -0011 answer.

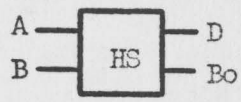
Given:

1. Quad Exclusive OR gate (7486)
2. Quad 2-input NAND gate (7400)
3. Hex Inverter (7404)

Procedure:

1. Wire up the half subtractor circuit shown below and verify the truth table. Use S1 and S2 for inputs (A and B) and L1 and L2 for outputs D (difference) and Bo (Borrow-out).

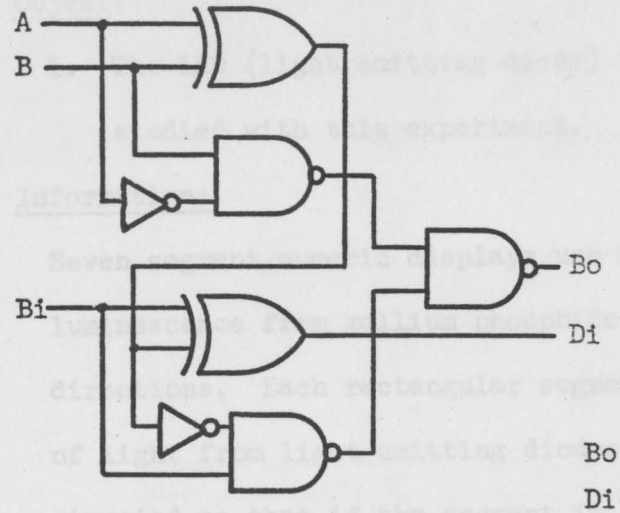


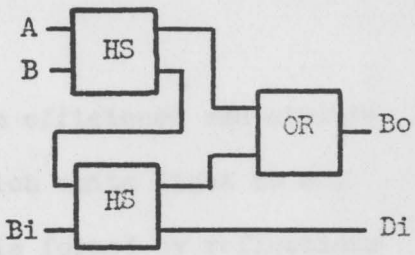


D=A$\bar{B}$+$\bar{A}$B = A⊕B
Bo=$\bar{A}$B

A	B	D	B_o
0	0	0	0
0	1	1	1
1	1	0	0
1	0	1	0

2. Wire up a second half subtractor circuit and combine outputs through an OR gate to make the full subtractor circuit shown below. Use S1, S2 and S3 for inputs (A, B and Bi) and L1 and L2 for outputs (borrow out and difference).





$Bo = \bar{A}B + \overline{(A \oplus B)}\ Bi$

$Di = A \oplus B \oplus Bi$

A	B	Bi	Bo	Di
0	0	0	0	0
0	0	1	1	1
0	1	0	1	1
0	1	1	1	0
1	0	0	0	1
1	0	1	0	0
1	1	0	0	0
1	1	1	1	1

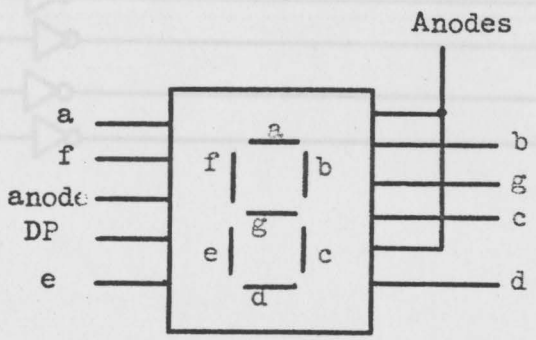
Experiment 7 (The Seven Segment Numeric Display)

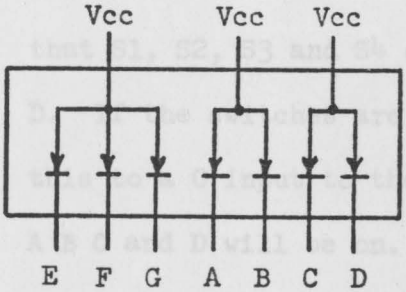
Object:

1. The LED (light emitting diode) 7 segment readout will be studied with this experiment.

Information:

Seven segment numeric displays use high efficiency red electroluminescence from gallium phosphide which emits light in all directions. Each rectangular segment is formed by reflections of light from light emitting diodes. The MAN-1 array is constructed so that if the segment is logical 1, the segment will be off, and when the segment is logical 0 (grounded) it should be on. The open collector inverter is used since it is capable of sinking sufficient current to prevent damage to the TTL units. The MAN-1 readout is shown below.





a b c d e f g	Display
0 0 0 0 0 0 1	0
1 0 0 1 1 1 1	1
0 0 1 0 0 1 0	2
0 0 0 0 1 1 0	3
1 0 0 1 1 0 0	4
0 1 0 0 1 0 0	5
1 1 0 0 0 0 0	6
0 0 0 1 1 1 1	7
0 0 0 0 0 0 0	8
0 0 0 1 1 0 0	9

Given:

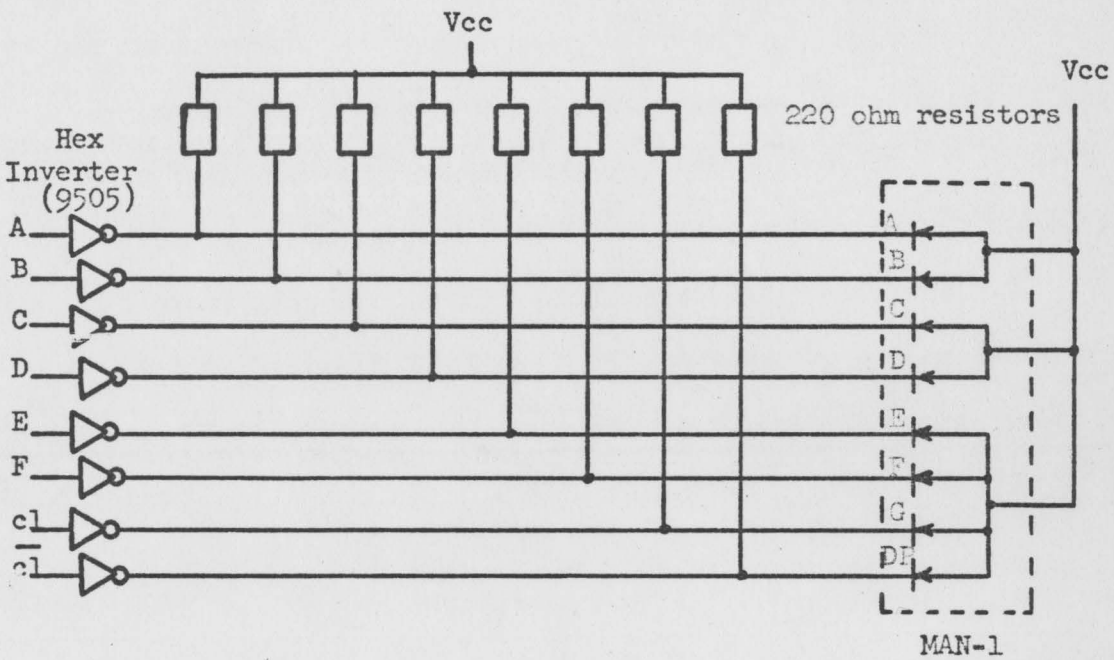
7 - 220 ohm resistors

1 - 7 segment MAN-1 display

2 - Open Collector Hex Inverters (7505)

Procedure:

1. Wire up the MAN-1 circuit given below. Use S1, S2, S3, S4, PB1, and PB2 for ABCDE and F.



2. Check the circuit for control of the MAN-1 segments. Note that S1, S2, S3 and S4 control segment sections A, B, C and D. If the switches are on (1 output), the inverter changes this to a 0 input to the MAN-1 segment and the MAN-1 segments A B C and D will be on. PB1 and PB2 outputs when push buttons are not depressed will be a logical 1. These feed th-

rough the inverters and place logical 0 signals on Man-1 segments E and F will be on. With G and DP (decimal point) connected to the clock outputs you should get a pulsing light on these two elements.

3. Verify the truth table for each of the numbers from 0 to 9.

CHAPTER VI

PRODAC (WESTINGHOUSE) NOR LOGIC

In Chapter II the NOR function was covered as one of the Basic Building Blocks for logic circuits. Figure 13 gave the symbol, the truth table, and the OR-NOT analogy. Figure 14 showed the schematic of the NOR element.

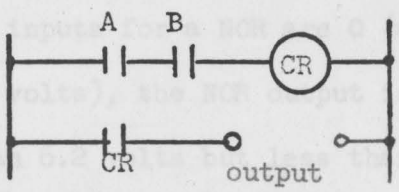
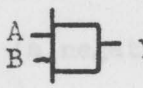
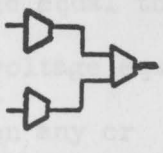
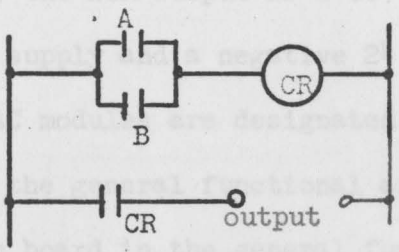
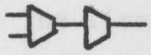
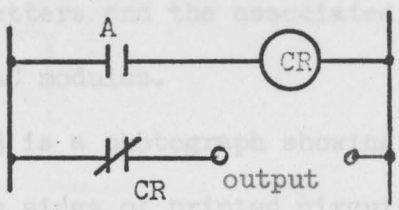
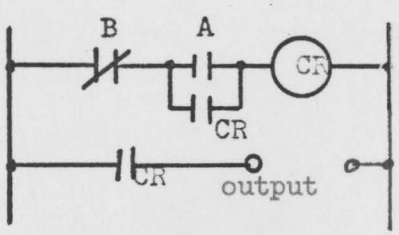
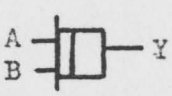
In Chapter IV a conversion technique was given to enable any of the basic logic gates to be converted to the NOR gate.

With this background Prodac circuitry utilizing NOR elements and the versatility of the NOR element are better understood.

The basic logic functions, and how they are accomplished with relay circuitry, conventional logic, and NOR logic are summarized in Table 12.

TABLE 12

NOR LOGIC GATES.

FUNCTION	RELAY CIRCUIT	CONVENTIONAL LOGIC	NOR LOGIC
AND		 Y=A•B	
OR		 Y=A+B	
NOT		 Y=$\bar{A}$	
OFF-RETURN MEMORY		 Y=(A+Y) $\bar{B}$	

PRODAC (Programmed Digital Automatic Control) systems incorporate printed circuit boards called modules on which are mounted a number of 3 input and/or 6 input NOR elements and other components. These modules plug into a cage that can accommodate sixteen modules.

Figure 32 shows the schematic diagrams and the NOR element terminal identification for the 3 input NOR and the 6 input NOR. The load is connected between ground and the output.

When all inputs for a NOR are 0 (a negative voltage equal to or less than 0.2 volts), the NOR output is 1 (a negative voltage equal to or greater than 6.2 volts but less than 39 volts). When any or all inputs are 1, the NOR output is a 0. The NOR element requires a positive 24 volt supply and a negative 24 volt supply.

All PRODAC modules are designated by two letters. The first letter describes the general functional area, the second letter specifies the specific board in the general functional area. Appendix A lists the code letters and the associated general functional area for the various PRODAC modules.

Figure 33 is a photograph showing some PRODAC circuitry, NOR elements and both sides of printed circuit modules.

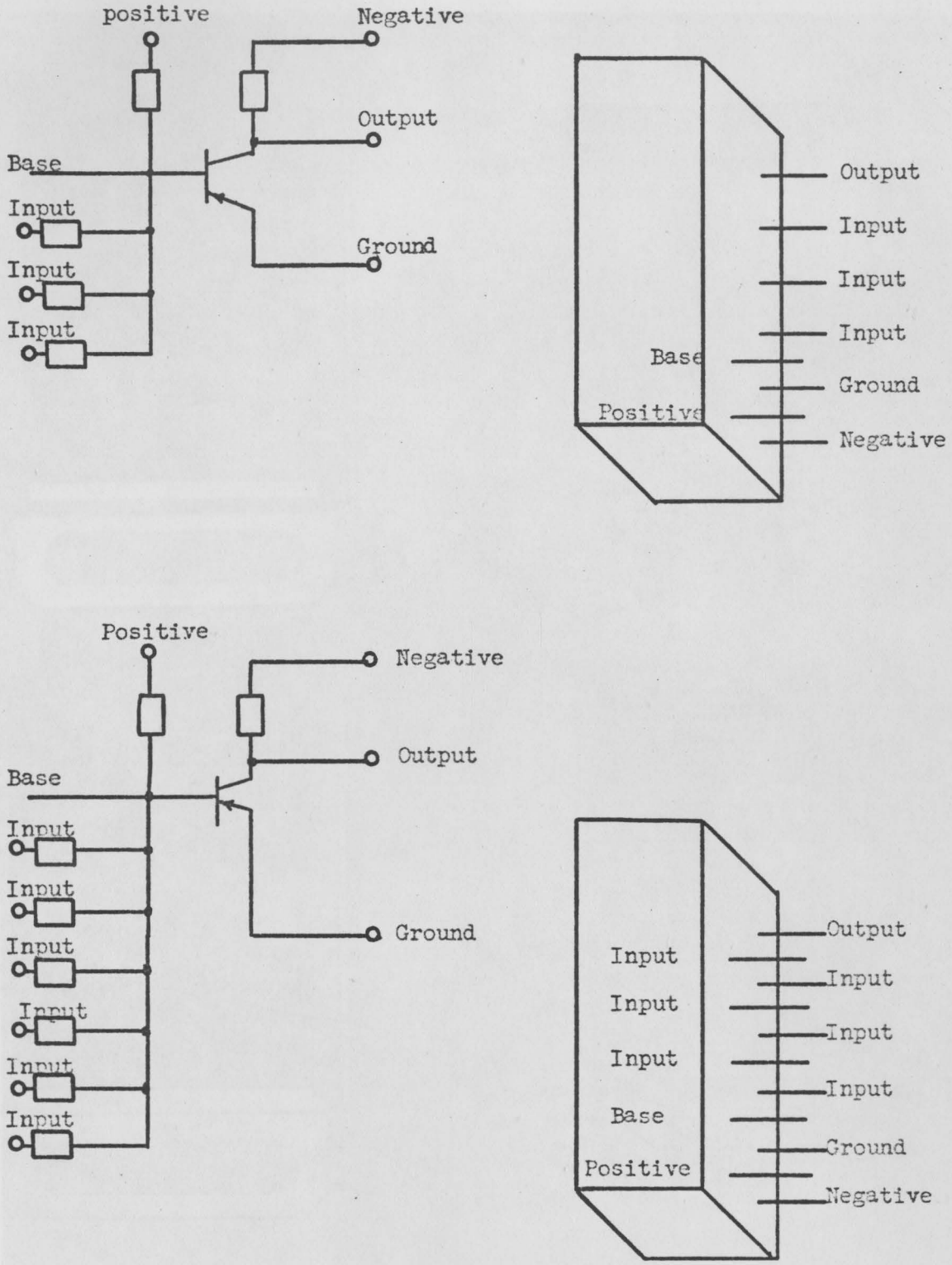


FIG. 32.--NOR ELEMENTS

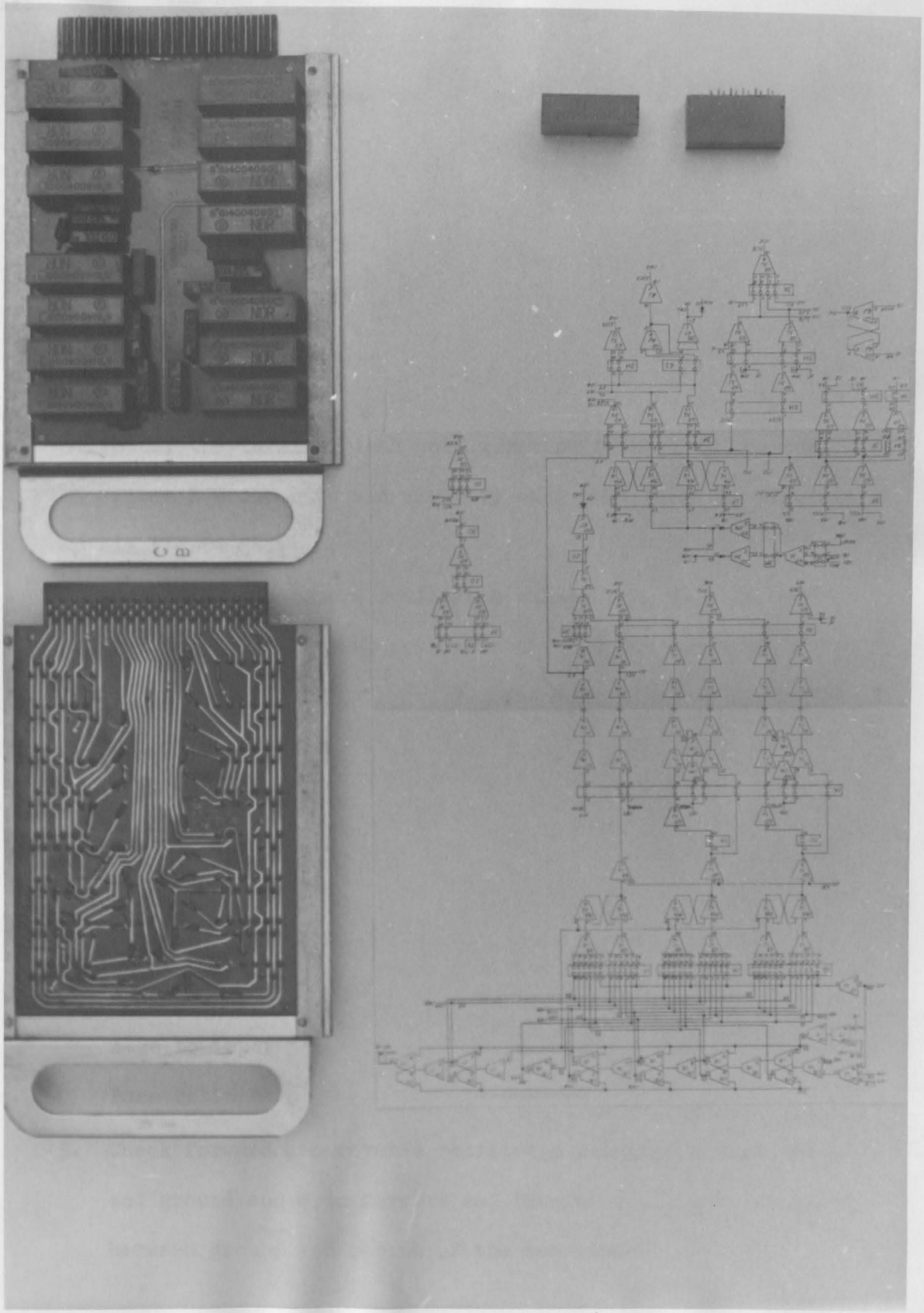


FIG. 33.--PRODAC MODULES AND NOR ELEMENTS

Project 1 (The NOR Element)

Object:

To study and verify operation of the 3 input and the 6 input NOR elements.

Given:

1 - 3 input NOR element

1 - 6 input NOR element

1 - VOM multimeter

Procedure:

1. Study the terminal lead configuration of each of the two given NOR elements and identify each lead from the drawings in Figure 34.
2. Determine and record resistance values read on multitester between the following points on the two NOR elements.

	3 input NOR	6 input NOR
Output to negative		
Base to positive		
Base to input 1		
Base to input 2		
Base to input 3		
Base to input 4	———	
Base to input 5	———	
Base to input 6	———	

3. Check forward and reverse resistance readings between base and ground and also forward and reverse resistance readings between ground and output of the transistor.

Project 2 (NOR Modules)

Object:

Trace out printed circuitry on DB and CB PRODAC modules and compare with Westinghouse related drawings.

Given:

1. PRODAC DB module and related drawing 217A075
2. PRODAC CB module and related drawing 217A070

Procedure:

1. Identify each component on the PRODAC DB module with its related symbol on drawing 217A075.
2. Trace out the circuitry of the DB module from each of the pin connections and verify connections indicated on the drawing.
3. Identify each component on the PRODAC CB module with its related symbol on Westinghouse drawing number 217A070.
4. Trace out the circuitry of the CB module from each of the pin connections and verify connections indicated on the drawing.

Project 3 (NOR Logic Circuits)

Object:

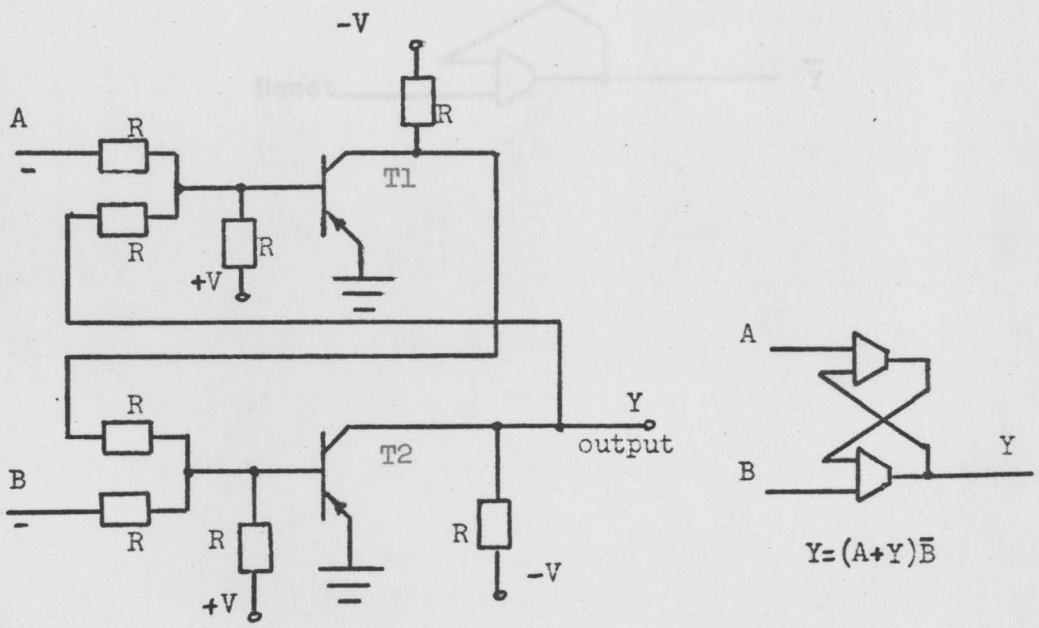
To understand memory circuit operation.

Information:

The bi-stable memory concept is important in circuits involving seal-in, under voltage, counting, and other applications having memory type requirements.

Given:

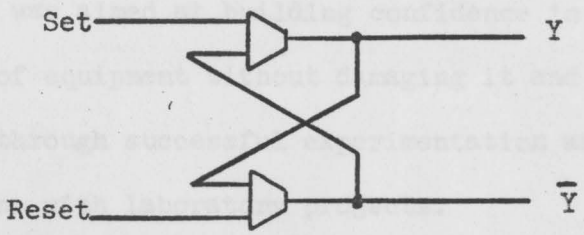
OFF-RETURN memory circuit and related NOR symbol



Procedure:

1. Explain the operation of the given NOR memory schematic.
2. Verify the equation $Y = (A+Y)\,\bar{B}$ given for the memory symbol output.

3. Study the bi-stable symbol below with this description. No input produces an output from one NOR and no output from the other, depending on which input last carried a signal. Inputs to both NOR's gives zero output from both. A momentary signal applied to the proper input is all that is required to reverse the outputs.



CHAPTER VII

SUMMARY

The purpose of this thesis was to develop a practical approach whereby electrical maintenance technicians and apprentices could through a "hands on approach" be able to understand and work with digital circuits and hardware.

The approach was aimed at building confidence in their ability to handle this type of equipment without damaging it and providing rewarding experiences through successful experimentation as they learn by practical applications with laboratory projects.

Each of the projects included in Chapter III on conventional logic, and Chapter V on inverting logic, were wired up and verified. Duplication in projects worked with the DSL experiments and TTL experiments were avoided to enable a broader coverage of binary circuits.

The chapter on Westinghouse (NOR) logic gives added insight into the versatility of the NOR gate, and a better understanding of logic flexibility.

For future consideration a greater number of projects involving dynamic boards such as pulsers, clocks, registers and counters would be beneficial.

Additional information including some basics of circuit synthesis including minimization techniques would give a fuller understanding of this field and enhance the practical understanding of digital circuitry gained from the previous chapters.

Taking an already designed system, understanding it, and maintaining it is understandably difficult, however, to take the requirements of a desired operation and from these requirements develop, through a logical sequence of design steps, the simplified and economical circuitry to achieve the desired system requirements is probably much more demanding.

The tutoral equipment and the projects developed to reinforce the learning of digital logic will be utilized in the future training of Youngstown Sheet and Tube electrical technicians and apprentices.

APPENDIX A

PRODAC Functional Area Code

A	Calculating Circuits
B	Machine Tool Control
C	Counters
D	Amplifiers
E	Pulsetter and Automatic Gauge Control
F	Filters
G	Gates
H	Digital to Analog Converter
I	Indicators
J	Analog to Digital Converter
K	Coding and Conversion
L	Anacon
M	Memory
N	Nordic Computer
O	Opcan Control
P	Pulse Shapers
S	Shift Registers
T	Timing
U	Universal
X	Special

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