

A HIGH-FREQUENCY TIME SHARING FREQUENCY INVERTER

by

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ABSTRACT

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Charles Alexander, Associate Professor of Electrical Engineering at Youngstown State University, who acted as my advisor on

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This thesis presents a theoretical study of the output parameters of a time sharing, naturally commutated series frequency inverter. This analysis was performed because of the student's interest in the area of time sharing frequency inverters. The field of study is timely and this work presents the basis for a practical field of application. A first approximation of the inverter is based on a short circuit load and conservation of energy principles. A Fourier analysis is performed on the circuit and a state variable analysis is then considered. The results are compared for a pure resistive load. A discussion is given concerning the output obtained by the clamping of the series capacitor voltage.

ACKNOWLEDGEMENTS

I wish to express sincerest thanks to Doctor Charles Alexander, Associate Professor of Electrical Engineering at Youngstown State University, who acted as my advisor on this thesis. His guidance, patience and counsel were greatly appreciated.

I also want to render my appreciation to Mr. George Havas of the Ajax Magnethermic Corporation who lent me his "ears".

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L Series inductance	Microhenries
C Series capacitance	Microfarads
R Load resistance	Ohms
x_1 State variable	See development
T Energy	watt-seconds
V_{dc} DC supply voltage	volts
ω Resonant frequency	radians per second
n Multiplier	See eq. (2-9)
N Harmonic number	none
N Maximum harmonic	none
f_{REP} Repetition rate	Hertz
f_o Frequency of the current pulse	Hertz
r Ratio of I_{REP}/f_o	none
I_p Peak load current	Ampere

LIST OF SYMBOLS

SYMBOL	DEFINITION	UNITS
L	Series inductance	Microhenries
C	Series capacitance	Microfarads
R	Load resistance	Ohms
x_i	State variable	See development
Υ	Energy	watt-seconds
E_{dc}	DC supply voltage	volts
ω	Resonant frequency	radians per second
n	Multiplier	See eq.(2-9)
N	Harmonic number	none
M	Maximum harmonic	none
f_{REP}	Repetition rate	Hertz
f_o	Frequency of the current pulse	Hertz
r	Ratio of f_{REP}/f_o	none
I_p	Peak load current	Amperes
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An inverter is an electronic frequency changer which converts an input frequency to a higher output frequency, as opposed to a cycloconverter which produces an output frequency lower than the input. Inverters are of two types. The first type produces an output directly from the input (AC/AC). The second type uses a DC link between the input and output alternating voltage (AC/DC/AC). The inverter discussed in this thesis is of the latter type.

Cycloconverters and inverters are two classes of frequency changers. The oldest type, the cycloconverter, was initially conceived by Hazeltine in 1923. His system allowed for free power flow to and from the load and the output to input frequency ratio could be arbitrarily chosen.

The first practical frequency changer was developed by Schenkel and Von Issendorff in the 1930's using mercury arc converters. It used phase control and was utilized to step down the line voltage frequency for use in electric trains in Europe.

The development of high speed, power transistors and thyristors (SCR's) enlarged the field of frequency changers. The 1960's saw major developments in the field

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CHAPTER I

INTRODUCTION

An inverter is an electronic frequency changer which converts an input frequency to a higher output frequency, as opposed to a cycloconverter which produces an output frequency lower than the input. Inverters are of two types. The first type produces an output directly from the input (AC/AC). The second type uses a DC link between the input and output alternating voltage (AC/DC/AC). The inverter discussed in this thesis is of the latter type.

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The development of high speed, power transistors and thyristors (SCR's) enlarged the field of frequency changers. The 1960's saw major developments in the field

of power conversion as SCR technology developed. Any future development in the frequency changer field will be linked to switching device (electric valve) technology.

A wide range of applications exist for high power and high frequency inverters utilizing silicon controlled rectifiers, henceforth to be referred to as SCR's. Typical applications include ultrasonic cleaners, induction heating power stations and large KVA DC power supplies with minimal ripple.

SCR's can be readily applied in high power applications for example, 10 kilowatt output and upward, however they are limited in high frequency uses due to the circuit commutated turnoff time (t_{off}) rating. The t_{off} parameter is defined as, "the time interval between the instant when the SCR current has decreased to zero after external switching of the SCR voltage circuit, and the instant when the SCR is capable of supporting a specified voltage waveform without turning on".¹ If the SCR fails to turn off when the current through it crosses zero the condition is referred to as a commutation failure. Such failures can cause permanent damage to the SCR.

Classes of SCR's are currently marketed with a small t_{off} parameter, however, the power handling capability of these devices decreases as the t_{off} parameter

¹Leslie R. Rice, et al, Silicon Controlled Rectifier Designers Handbook (Youngwood, Pennsylvania: Westinghouse Electric Corporation, 1970), pp3-6.

declines. Appendix A contains a brief discussion of the limitations of SCR's with regard to power handling capability and circuit commutated turnoff time. SCR devices with small t_{off} parameters are necessary in high frequency applications when standard inverter configurations are used.

The high frequency limitations can be overcome by using time sharing inverter networks. Various series time sharing inverter schemes have been proposed by Nishimura, et al. [1]

Power control can be implemented in many ways, for example, controlling the DC voltage in a DC link and controlling the repetition rate of the energizing of the SCR's.

This thesis is dedicated to determining the output characteristics of a time sharing series inverter operated at a nominal frequency of 10KHz. Power control is to be accomplished by a variation of the repetition frequency of the SCR firings. A pure resistive load will be considered.

Chapter II deals with a method of approximating the output characteristic of the proposed inverter by using energy relationships.

Chapter III deals with the Fourier analysis of the inverter with a small resistive load where the results of Chapter II are utilized.

Chapter IV is a discussion of the results of a

state variable analysis of the inverter.

Chapter V deals with the clamping of the series capacitor voltage. Several methods are discussed and a Fourier analysis and state variable analysis is presented for the most practical method.

Chapter VI is a brief discussion of the results of this thesis and proposed future work is presented.

The battery shown for E_{dc} will be considered to be ideal.

The circuit shown in Fig. 2-1 was first proposed by Nishizura, et al. [1]. The SCR's are fired one at a time in sequence, i.e., 4, 3, 2, 1. This sequence was arbitrarily chosen. All that is required is to fire the SCR's in opposite loops alternately. For the purpose of analysis the SCR's will be assumed to be perfect unidirectional switches. L_1 is to be equal to L_2 and all capacitors are of equal value. Henceforth the inductors will be designated L and the capacitors will be designated C . Notice that if SCR₁ or 3 is energized there exists a path for current flow through C_2 and C_4 . Similarly for the energizing of SCR₂ or 4. For a practical inverter this wasted reactive current component should be kept to a minimum. Thus the load resistance should be kept small with respect to the impedance in the loop opposite to the loop being activated.

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INITIAL CONSIDERATIONS

Introduction

Due to the complexity of the proposed network shown in Fig. 2-1, a reasonable means of approximating the range of output wattage and series capacitor voltage is necessary. The batteries shown for E_{dc} will be considered to be ideal.

The circuit shown in Fig. 2-1 was first proposed by Nishimura, et al. [1] The SCR's are fired one at a time in sequence, ie, 4,3,2,1. This sequence was arbitrarily chosen. All that is required is to fire the SCR's in opposite loops alternately. For the purpose of analysis the SCR's will be assumed to be perfect unidirectional switches. L_1 is to be equal to L_2 and all capacitors are of equal value. Henceforth the inductors will be designated L and the capacitors will be designated C . Notice that if SCR_1 or 3 is energized there exists a path for current flow through C_2 and C_4 . Similarly for the energizing of SCR_2 or 4. For a practical inverter this wasted reactive current component should be kept to a minimum. Thus the load resistance should be kept small with respect to the impedance in the loop opposite to the loop being activated.

Fig. 2-3. SCR_1 Energized with a Short Circuit Load.

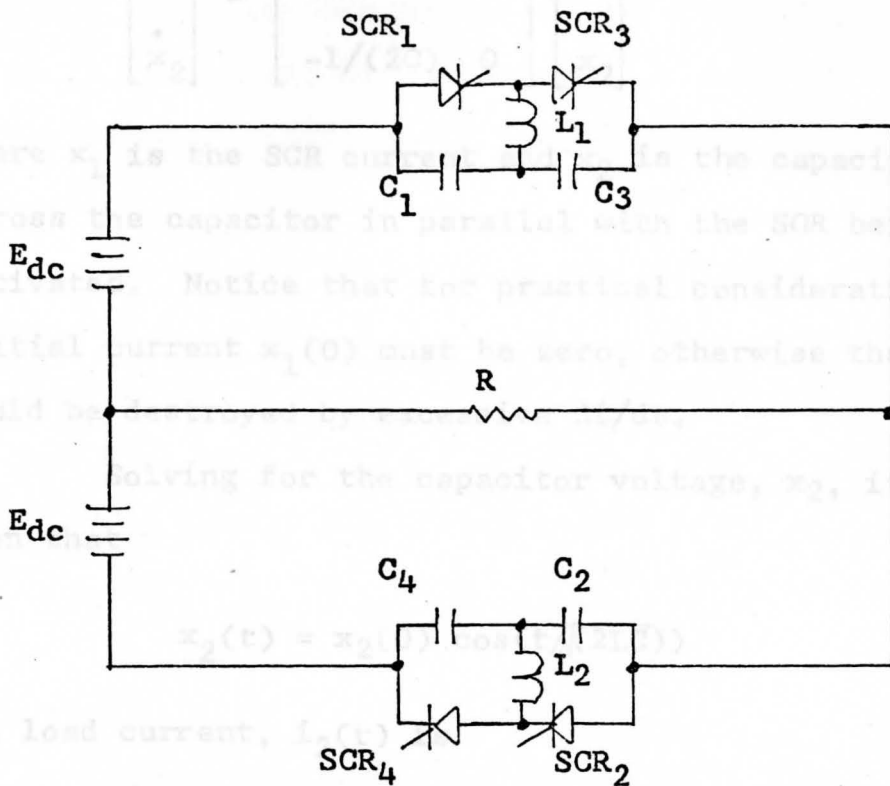


Fig. 2-1. Basic Inverter Circuit.

Short Circuit Considerations

Consider the inverter with a shorted load as shown in Fig. 2-2. The state equation for this condition is

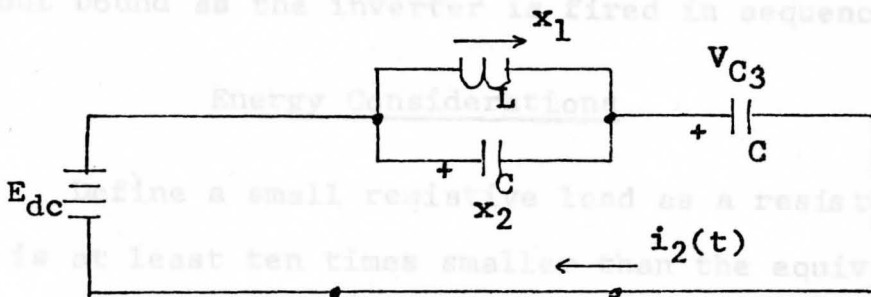


Fig. 2-2. SCR₁ Energized with a Short Circuit Load.

$$\begin{bmatrix} \dot{x}_1 \\ \dot{x}_2 \end{bmatrix} = \begin{bmatrix} 0 & 1/L \\ -1/(2C) & 0 \end{bmatrix} \begin{bmatrix} x_1 \\ x_2 \end{bmatrix} \quad (2-1)$$

Where x_1 is the SCR current and x_2 is the capacitor voltage across the capacitor in parallel with the SCR being activated. Notice that for practical considerations the initial current $x_1(0)$ must be zero, otherwise the SCR could be destroyed by excessive di/dt .

Solving for the capacitor voltage, x_2 , it is seen that

$$x_2(t) = x_2(0) \cos(t/\sqrt{2LC}) \quad (2-2)$$

The load current, $i_2(t)$ is

$$i_2(t) = x_1(t) + C\dot{x}_2(t) \quad (2-3)$$

or

$$i_2(t) = x_2(0)\sqrt{C/(2L)} \sin(\sqrt{1/(2LC)} t) \quad (2-4)$$

It is obvious that the capacitor voltages will increase without bound as the inverter is fired in sequence.

Energy Considerations

Define a small resistive load as a resistive load that is at least ten times smaller than the equivalent capacitive reactance magnitude, at the nominal frequency, in the loop not containing the the SCR being energized.

The steady state capacitor voltages can then be approximated. Under the assumed load, the current can be assumed to be the short circuit current and all energy from the source can be considered to be dissipated in the load resistance.

The energy delivered from the supply is

$$T_d = 2E_{dc}I_p/\omega \tag{2-5}$$

at $\omega t = \pi$.

The energy dissipated in the load is

$$T_l = R(I_p)^2 \pi / (2\omega) \tag{2-6}$$

at $\omega t = \pi$.

Equating and solving for I_p it is found that:

$$I_p = 4E_{dc}/(\pi R) \tag{2-7}$$

but from the short circuit analysis

$$I_p = x_2(0) \sqrt{C/(2L)} \tag{2-8}$$

Let $x_2(0)$ be equal to nE_{dc} , then solving for n it is seen that

$$n = (4/(R\pi)) \sqrt{(2L)/C} \tag{2-9}$$

The energy delivered to the load becomes

$$T_l = ((nE_{dc})^2 CR\pi) / (4L\omega) \tag{2-10}$$

and the power delivered to the load is

$$KW = 2(T_1)(\text{repetition rate})(10^{-3}) \quad (2-11)$$

Table I summarizes the output characteristic of the inverter for a five to one variation in load resistance. The values of L and C are sized to give a natural resonant frequency of approximately 10 KHz. The data presented gives the multiple by which the capacitor voltage will be increased, based on the supply voltage, the energy dissipated in the load, and the maximum expected kilowatt output.

TABLE I
OUTPUT CHARACTERISTICS FOR VARIOUS SERIES
L AND C COMPONENTS, RESISTIVE LOAD

R	L ^a	C ^b	n	T ₁ ^c	KW ^d
.130	5.32	24.	6.52	3.11	62.0
.104	5.32	24.	8.15	3.89	78.0
.078	5.32	24.	10.87	5.19	103.9
.052	5.32	24.	16.30	7.79	155.8
.026	5.32	24.	32.60	15.58	311.6
.256	10.5	12.	6.68	1.58	31.7
.212	10.5	12.	7.94	1.90	38.2
.159	10.5	12.	10.60	2.55	51.0
.106	10.5	12.	15.89	3.82	76.5
.053	10.5	12.	31.78	7.65	153.0
.530	21.1	6.	6.37	.76	15.3
.424	21.1	6.	7.96	.95	19.1
.318	21.1	6.	10.62	1.27	25.5
.212	21.1	6.	15.93	1.91	38.2
.106	21.1	6.	31.85	4.89	76.4

^aunits are microhenries

^bunits are microfarads

^cbased on E_{dc} equal to 100 volts

^dbased on 10000. Hz repetition rate

CHAPTER III

FOURIER ANALYSIS OF THE INVERTER

Introduction

Most physical systems, unfortunately, are not submitted to simple periodic excitations such as pure sine or cosine waves. It was recognized long ago that if a periodic function² could be expressed in a series such as

$$f(t) = \frac{1}{2}a_0 + \sum_{k=1}^{\infty} a_k \cos t + \sum_{k=1}^{\infty} b_k \sin t \quad (3-1)$$

then each term could be handled individually and solutions to physical problems could be readily obtained. [2] Daniel Bernoulli (1700-1782) showed that the most general solution to the vibrating string problem is in the form

$$y = \sum_{k=1}^{\infty} A_k \sin(k\pi x/l) \cos(k\pi ct/l). \quad (3-2)$$

Joseph Fourier in his monograph, "Théorie analytique de la chaleur", (1822) for the first time proved that such series converged for a large number of specific cases. [3] This was a major breakthrough in the theory of periodic analysis.

²A function is said to be periodic if \exists a constant, $2p$, $\ni f(t+2p)=f(t) \forall t$.

This Fourier analysis is based on the approximations developed in the previous chapter. The purpose of this analysis is to determine the range of frequency control that is inherent in this system. If a user of this system desires to maintain a constant power output as the load changes it would be necessary to vary the frequency of repetition to avoid tap changes in the output transformer, if one is used, or change the value of the DC supply voltage.

Analysis Details

Fig. 3-1 shows the equivalent circuit of the system for the purpose of Fourier analysis. The current pulses are shown in Fig. 3-2. Current pulse amplitude is defined by equation (2-8) and the data taken from Table I for various values of series inductance and capacitance.

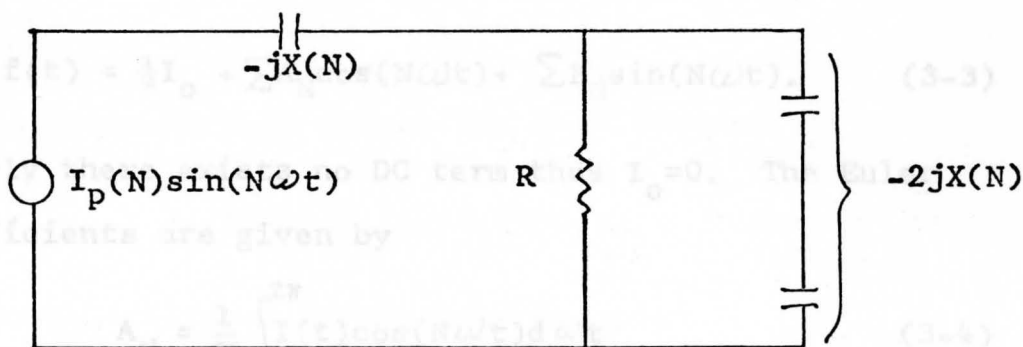


Fig. 3-1. Equivalent Circuit for Fourier Analysis.

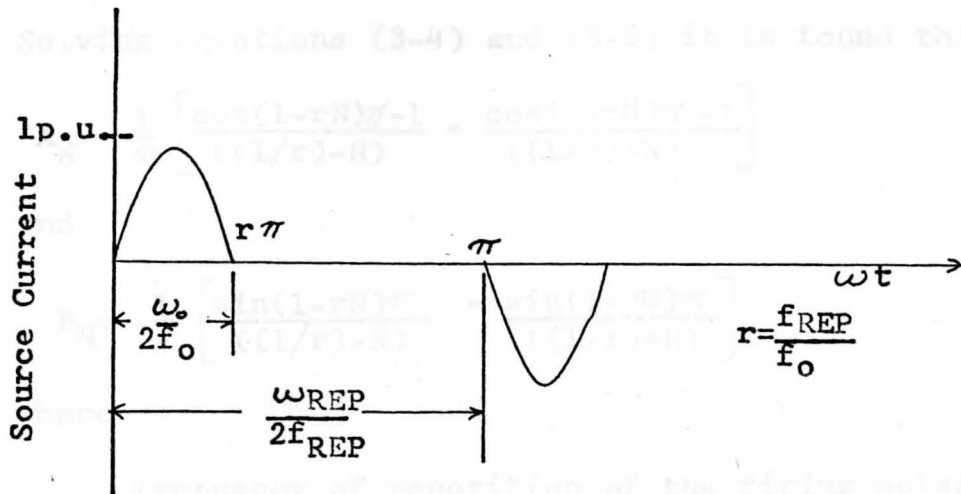


Fig. 3-2. Current Pulses for Fourier Analysis.

It is clear that the Dirichlet conditions are met, since the function has a finite number of discontinuities, and maxima and minima. The function is also bounded, i.e. a function is bounded on a set S if there exists a number M such that $f(p) \leq M$ for all $p \in S$, and of period 2π where the maxima, minima, and discontinuities occur. [2] [5]

The Fourier series can then be written.

The standard representation for the series is

$$f(t) = \frac{1}{2}I_0 + \sum A_N \cos(N\omega t) + \sum B_N \sin(N\omega t). \quad (3-3)$$

Clearly there exists no DC term thus $I_0 = 0$. The Euler coefficients are given by

$$A_N = \frac{1}{\pi} \int_0^{2\pi} I(t) \cos(N\omega t) d\omega t \quad (3-4)$$

and

$$B_N = \frac{1}{\pi} \int_0^{2\pi} I(t) \sin(N\omega t) d\omega t \quad (3-5)$$

Solving equations (3-4) and (3-5) it is found that

$$A_N = -\frac{1}{\pi} \left[\frac{\cos(1-rN)\pi - 1}{((1/r) - N)} + \frac{\cos(1+rN)\pi - 1}{((1/r) + N)} \right] \quad (3-6)$$

and

$$B_N = -\frac{1}{\pi} \left[\frac{\sin(1-rN)\pi}{((1/r) - N)} - \frac{\sin(1+rN)\pi}{((1/r) + N)} \right] \quad (3-7)$$

where

$$r = \frac{\text{frequency of repetition of the firing pulses}}{\text{current pulse equivalent frequency}} \quad (3-8)$$

and

$N = \text{harmonic number (integer)}$

The current waveform is symmetric thus the even harmonics are zero. A plot of the Euler coefficients is shown in Fig. 3-3. The harmonic magnitudes are on a one per unit basis.

The impedance as seen by the current source is

$$Z_1(N\omega) = \frac{2R}{\omega NC((R^2 + 4/((\omega NC)^2))^{1/2})} \left/ \text{Atan} \left(\frac{-2}{\omega NRC} \right) - \frac{\pi}{2} \right. \quad (3-9)$$

The harmonic voltage across the load becomes

$$V_1(N\omega) = I_p(N\omega) Z_1(N\omega) \quad (3-10)$$

The power delivered to the load becomes

$$P = \frac{V_{1rms}^2}{R} \quad (3-11)$$

where

$$V_{1_{rms}} = \left[\sum_{N=1}^M \frac{V_1(N\omega)^{**2}}{2} \right]^{\frac{1}{2}} \quad (3-12)$$

and M is the number of harmonics being considered. For this analysis the first nine harmonics were sufficient for use. [5]

Figures 3-4 through 3-10 show the results of the Fourier analysis. The smallest inductance was chosen as about five microhenries since smaller values of inductance are difficult to achieve in large KVA inverters. The capacitance was chosen to provide a series resonant frequency of 10000. Hz., and the largest value of load resistance was chosen to be ten times smaller than the excess loop reactance at 10000. Hz. The changes in the load resistance reflect a five to one load variation.

The plot of the root mean squared load voltage versus repetition rate (Fig. 3-7) clearly shows the constant current characteristic of this inverter. Combining equations (2-8) and (2-9) it is clear that

$$I_p = \frac{4E_{dc}}{\pi R} \quad (3-13)$$

and from Ohm's Law the peak load voltage becomes

$$V_{1_p} = \frac{4E_{dc}}{\pi} \quad (3-14)$$

The rest of the plots show the direct relationship of the output power to the repetition rate and the inverse relationship of output power to load resistance.

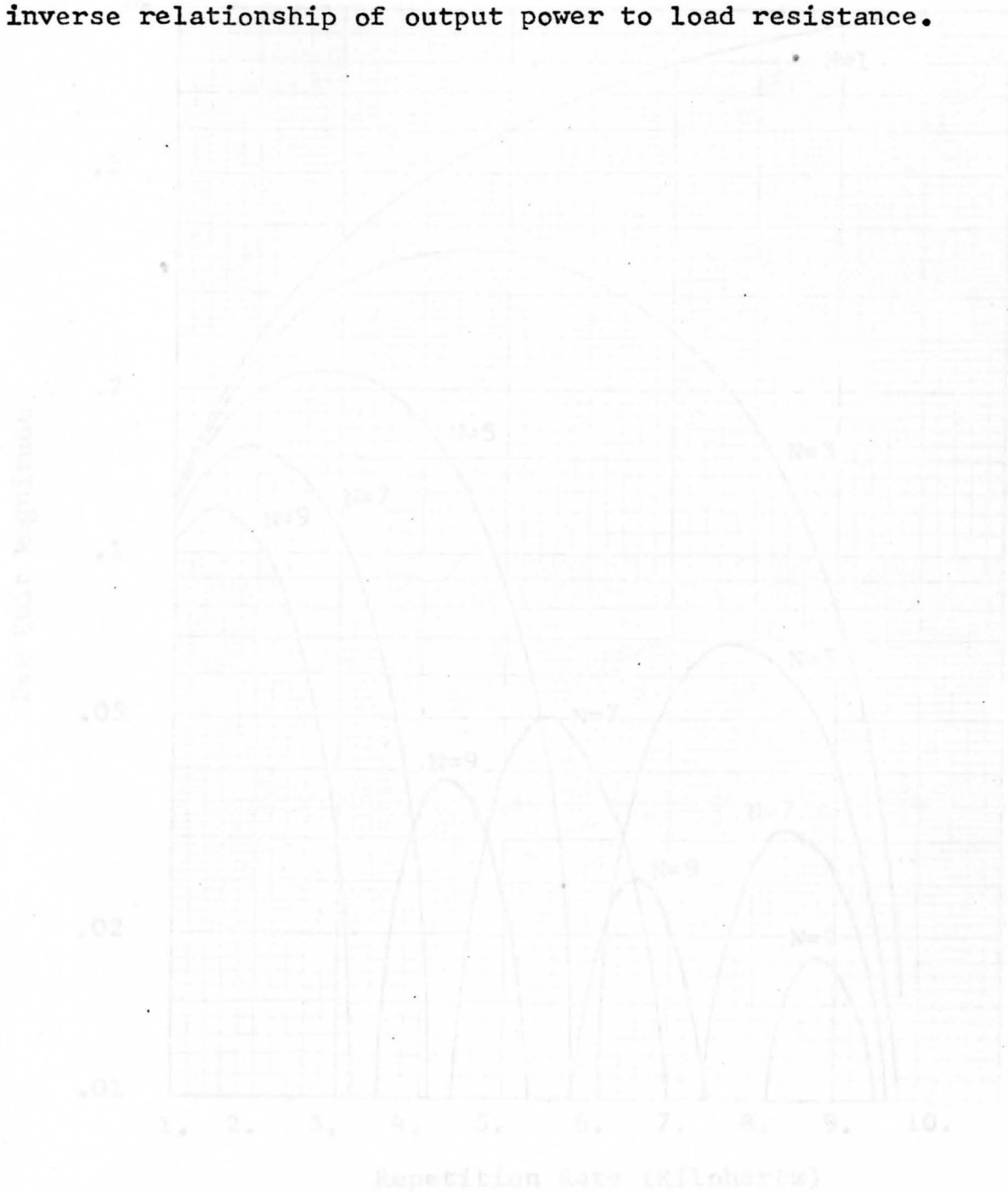


Fig. 3-3. Euler Coefficients; N is the Harmonic Number.

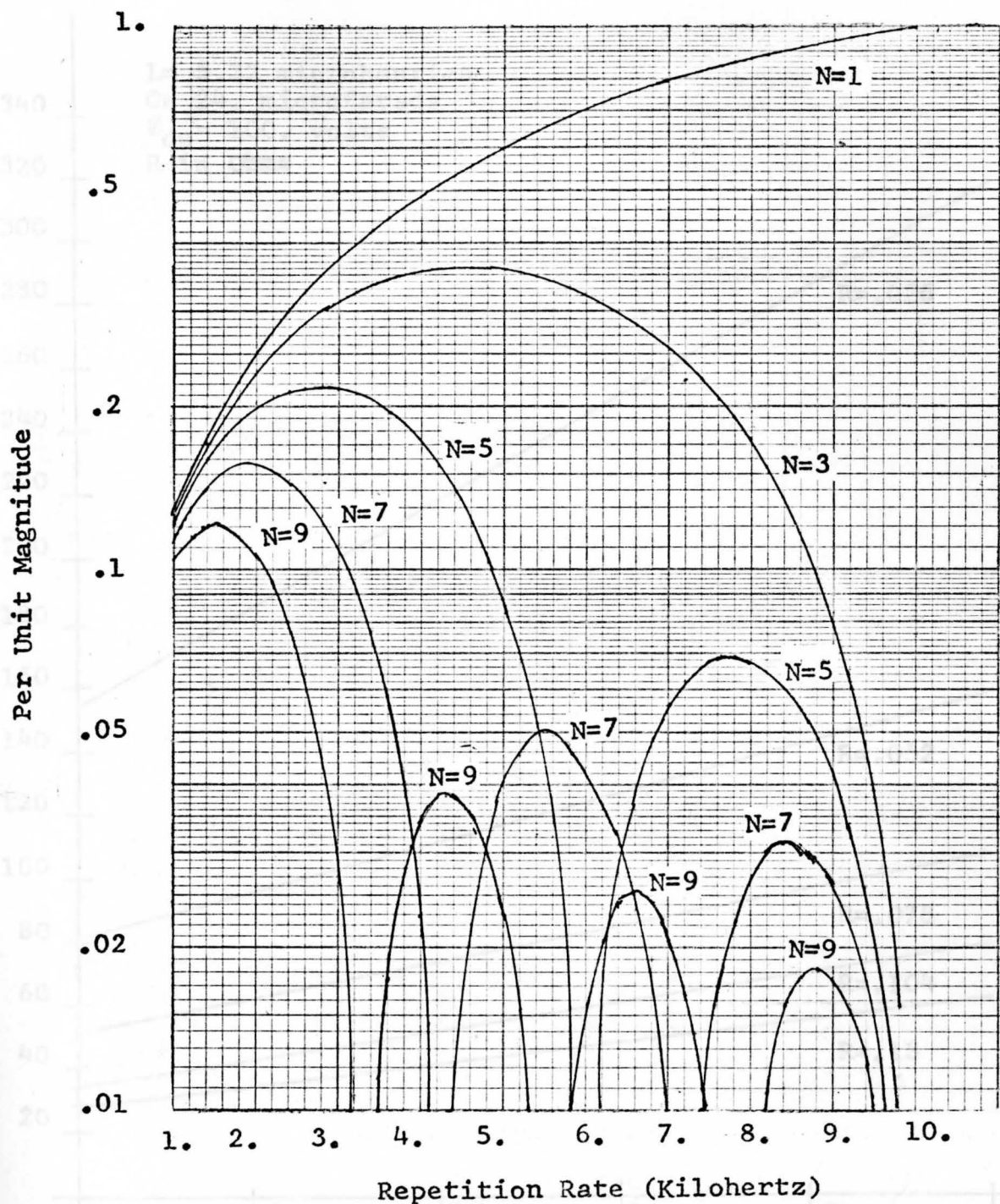


Fig. 3-3. Euler Coefficients; N is the Harmonic Number.

Fig. 3-4. Kilowatt Output Versus Repetition Rate.

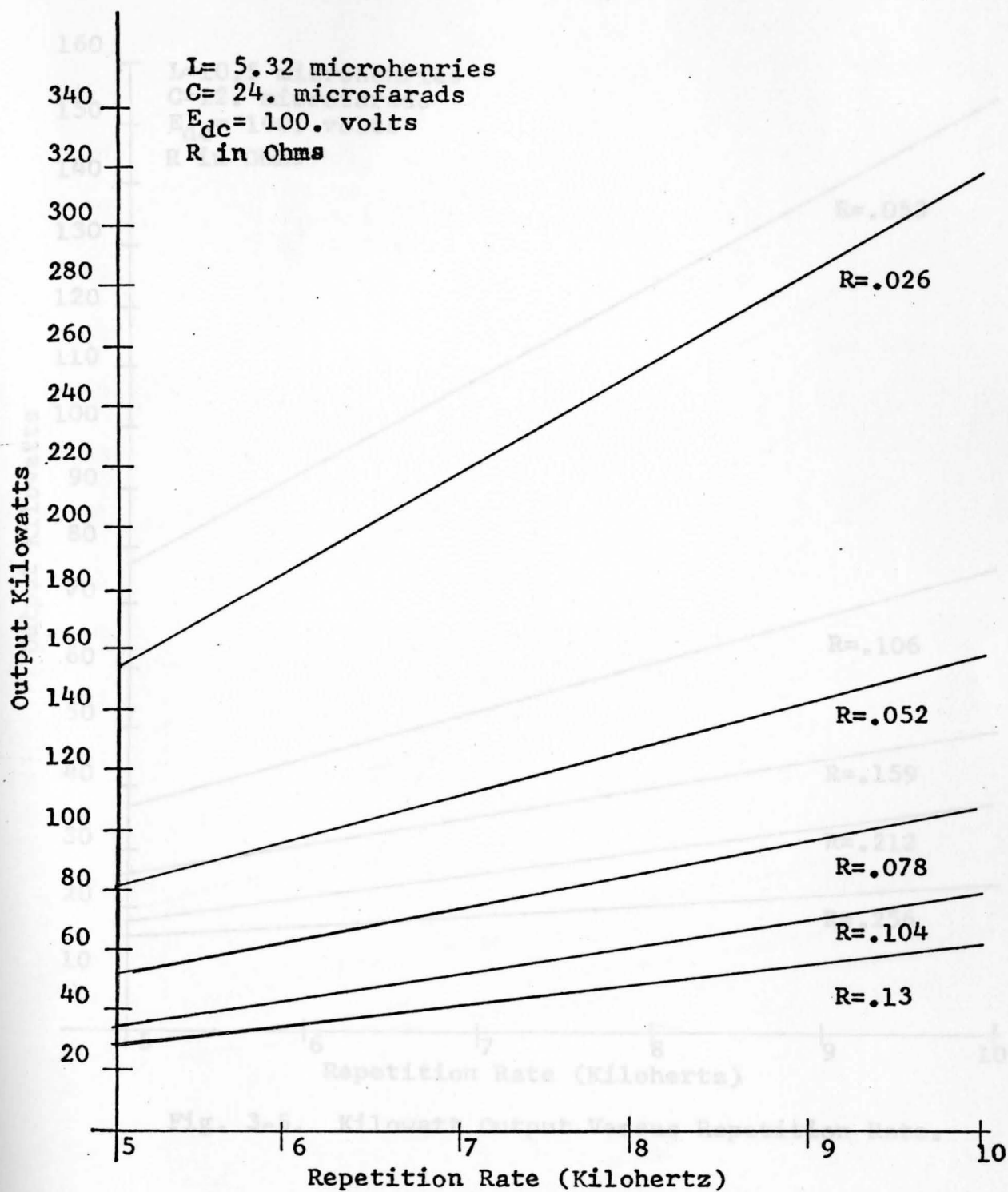


Fig. 3-4. Kilowatt Output Versus Repetition Rate.

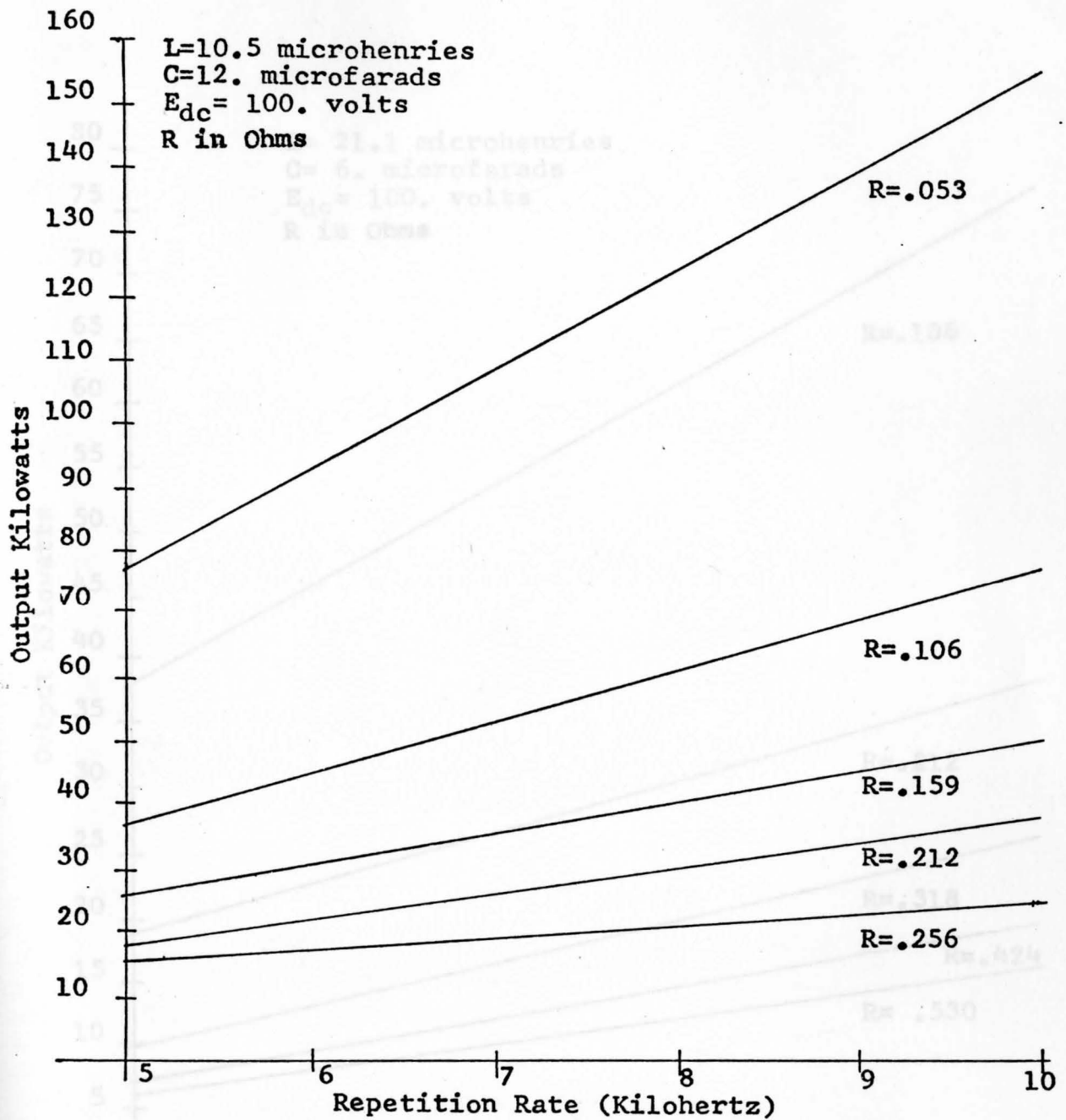


Fig. 3-5. Kilowatt Output Versus Repetition Rate.

Fig. 3-6. Output Kilowatts Versus Repetition Rate.

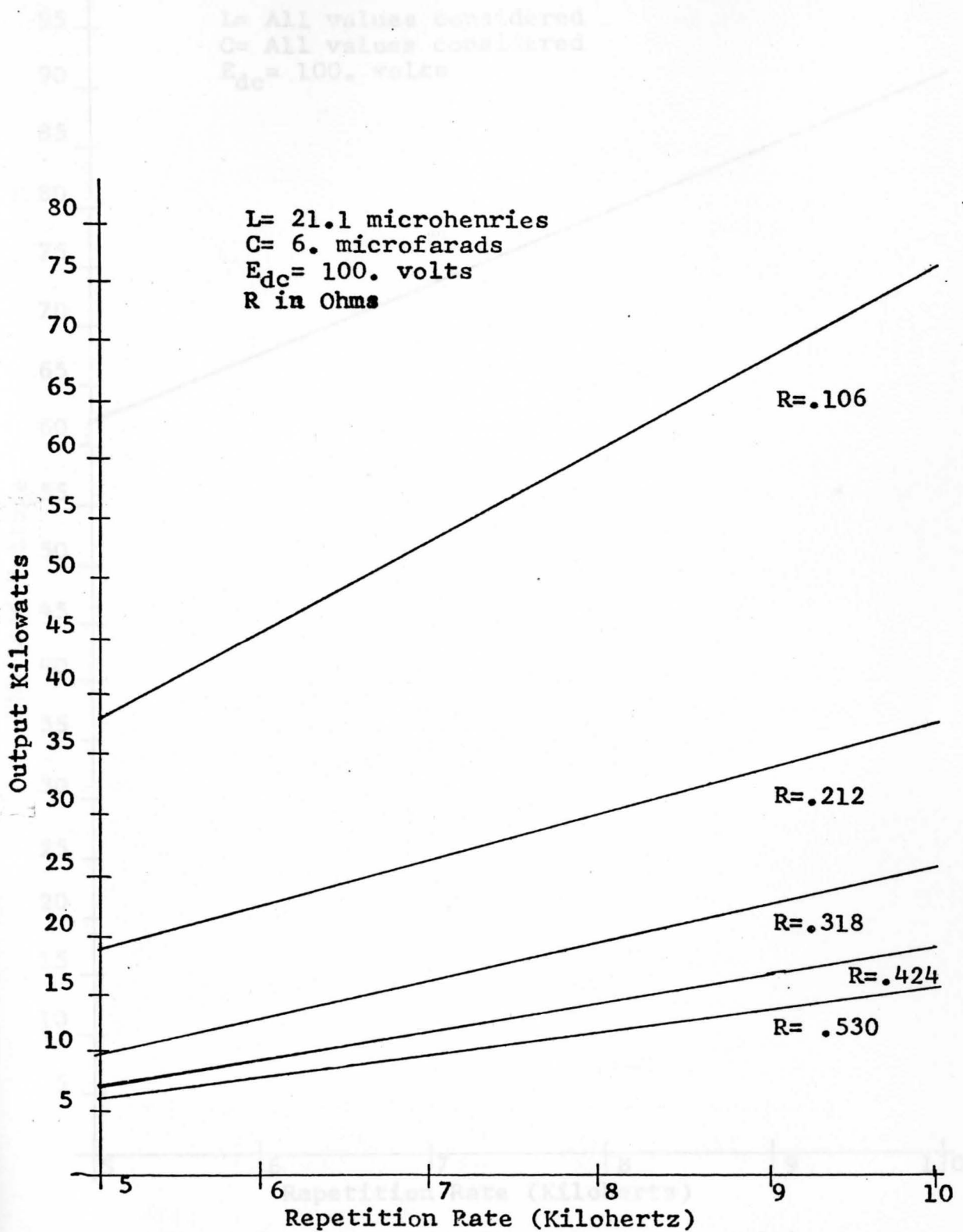


Fig. 3-6. Output Kilowatts Versus Repetition Rate.

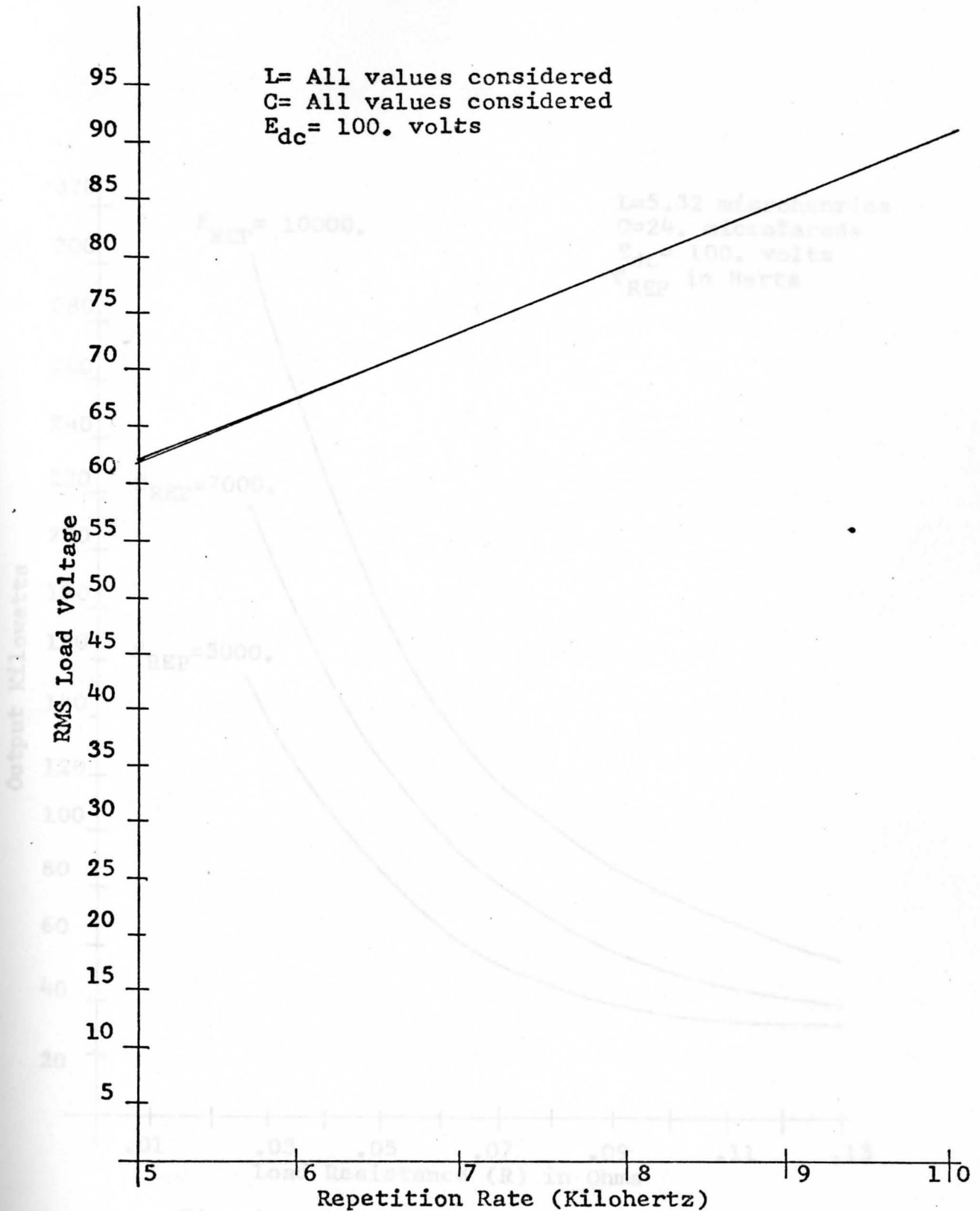


Fig. 3-7. RMS Load Voltage Versus Repetition Rate For All Load Conditions and Series Components.

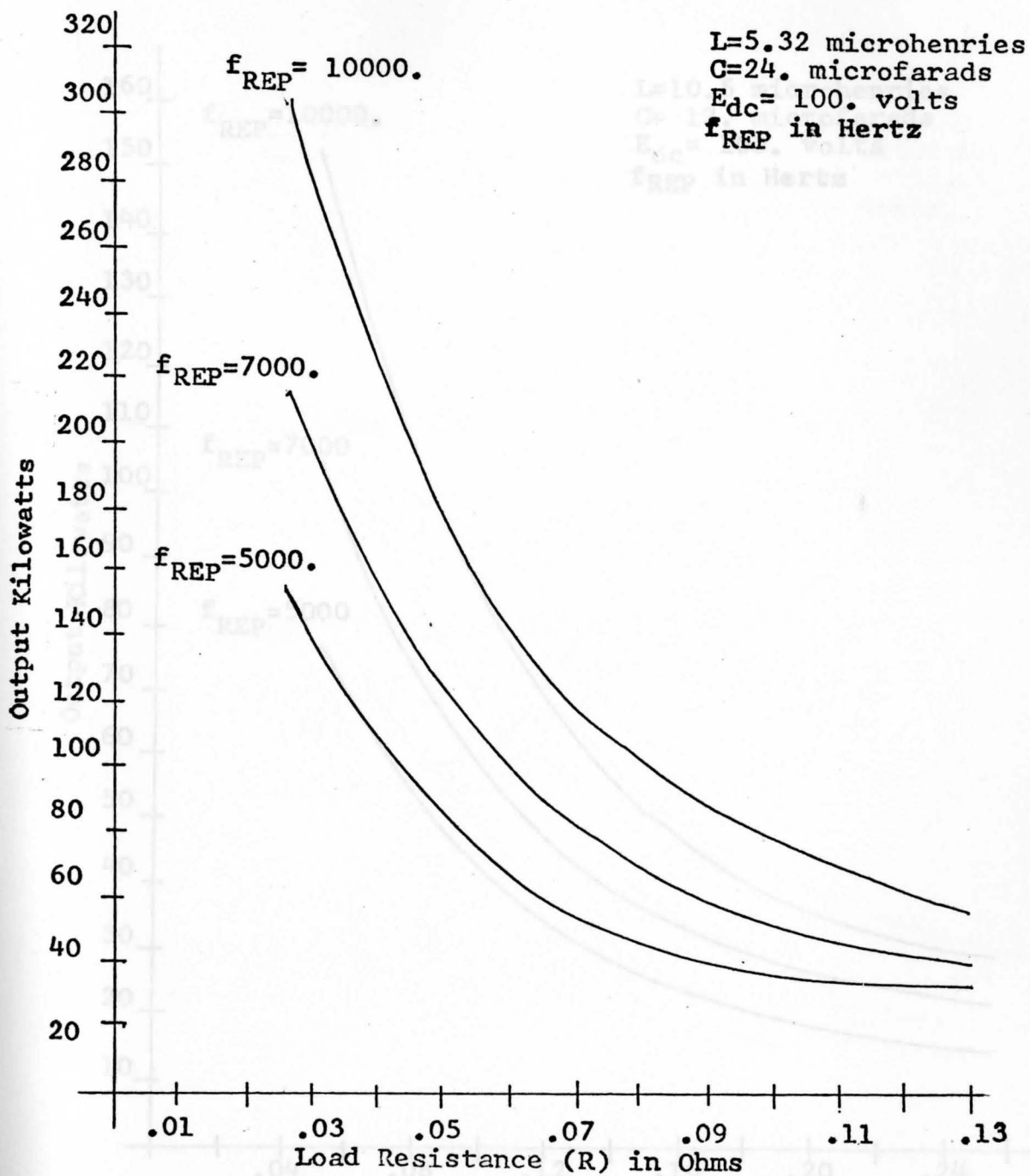


Fig. 3-8. Output Kilowatts Versus Load Resistance for a Family of Repetition Rates.

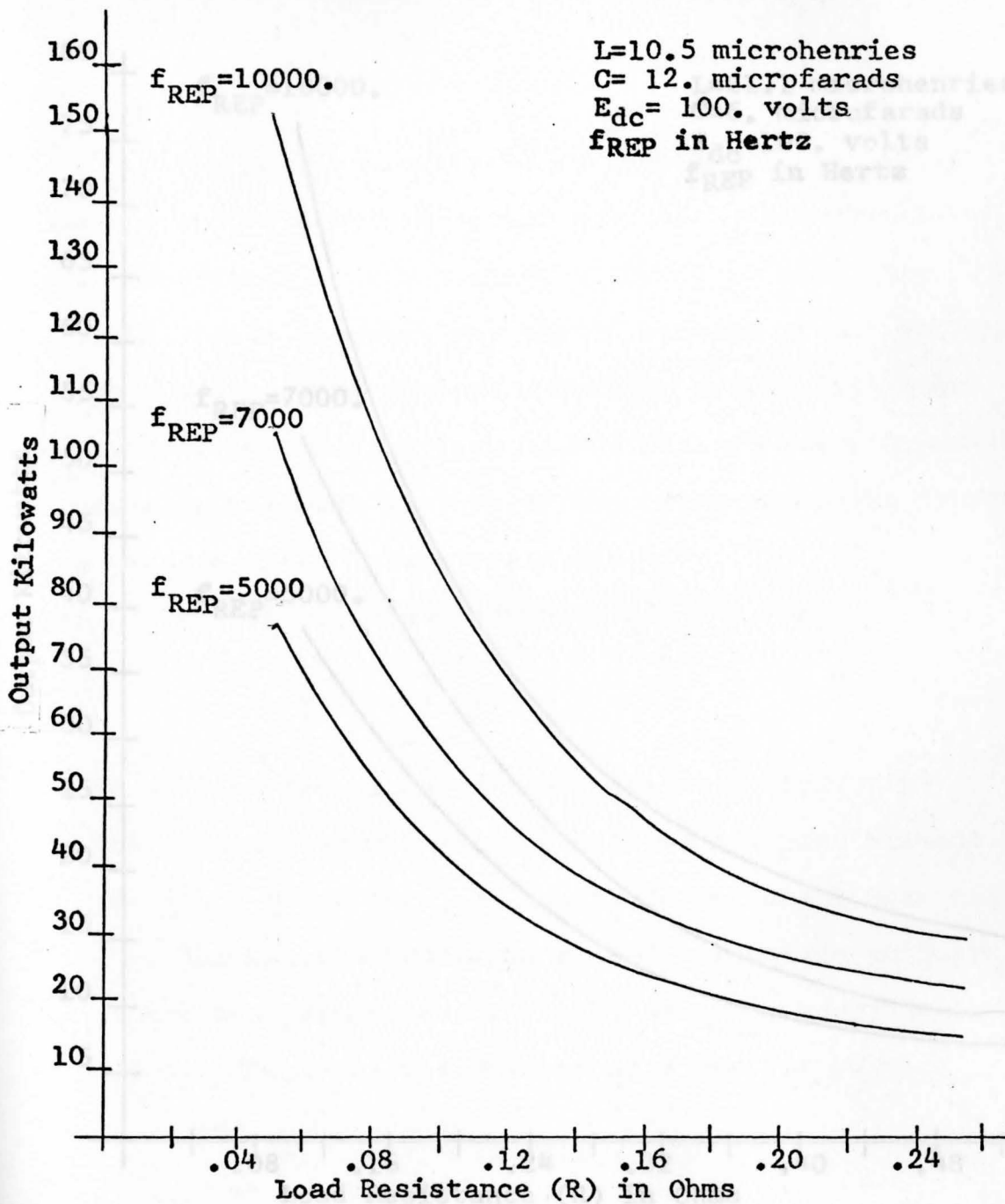


Fig. 3-9. Output Kilowatts Versus Load Resistance for a Family of Repetition Rates.

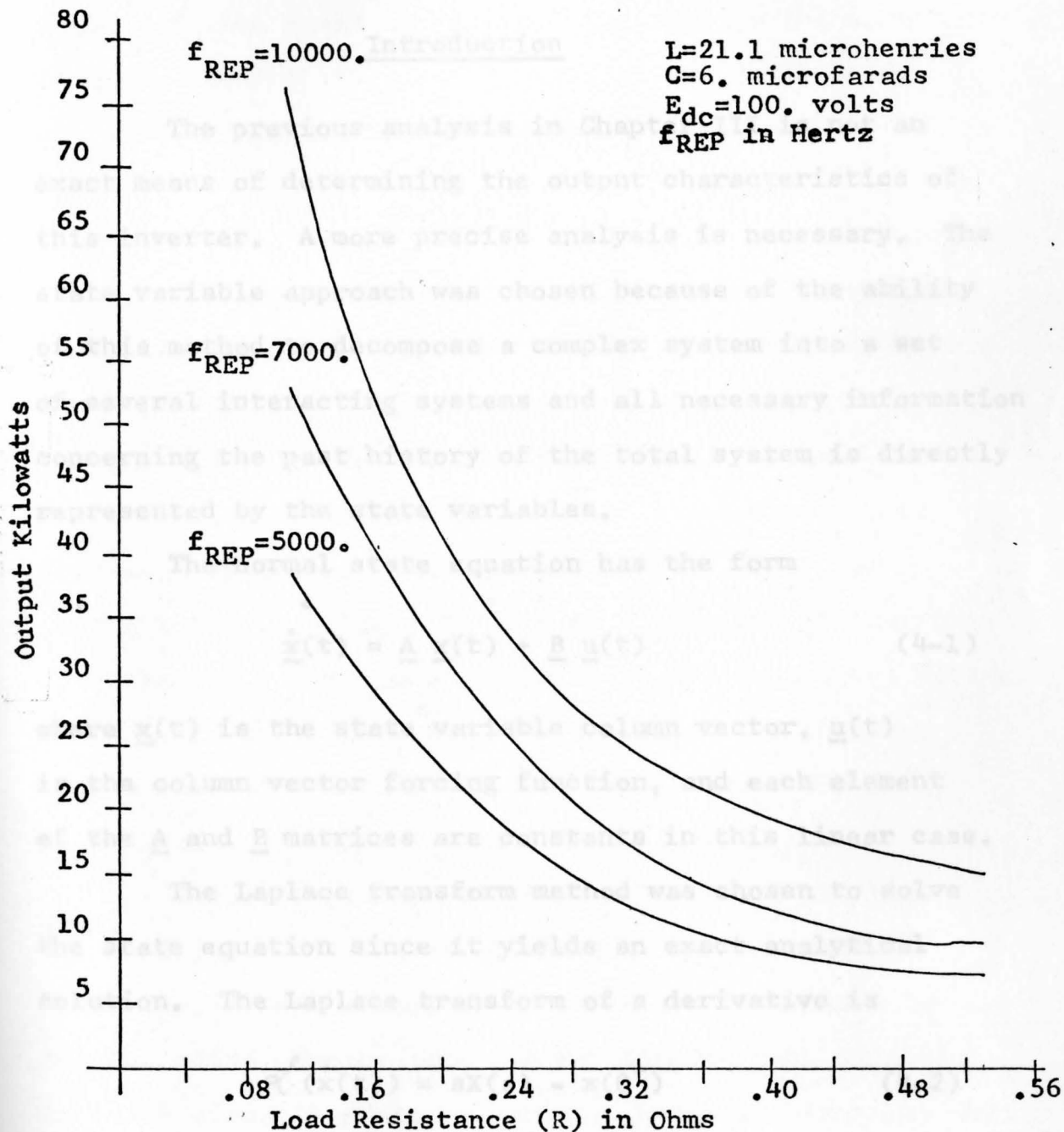


Fig. 3-10. Output Kilowatts Versus Load Resistance for a Family of Repetition Rates.

----- (4-3)

CHAPTER IV

STATE VARIABLE ANALYSIS FOR RESISTIVE LOADS (4-4)

Introduction

The previous analysis in Chapter III is not an exact means of determining the output characteristics of this inverter. A more precise analysis is necessary. The state variable approach was chosen because of the ability of this method to decompose a complex system into a set of several interacting systems and all necessary information concerning the past history of the total system is directly represented by the state variables.

The normal state equation has the form,

$$\dot{\underline{x}}(t) = \underline{A} \underline{x}(t) + \underline{B} \underline{u}(t) \quad (4-1)$$

where $\underline{x}(t)$ is the state variable column vector, $\underline{u}(t)$ is the column vector forcing function, and each element of the \underline{A} and \underline{B} matrices are constants in this linear case.

The Laplace transform method was chosen to solve the state equation since it yields an exact analytical solution. The Laplace transform of a derivative is

$$\mathcal{L}(\dot{\underline{x}}(t)) = s\underline{X}(s) - \underline{x}(0^+) \quad (4-2)$$

therefore the Laplace transform of equation (4-1) becomes

$$s\underline{X}(s) = \underline{A} \underline{X}(s) + \underline{B} \underline{U}(s) + \underline{x}(0^+) \quad (4-3)$$

or

$$\underline{X}(s) = (s\underline{I} - \underline{A})^{-1} \underline{x}(0^+) + (s\underline{I} - \underline{A})^{-1} \underline{B} \underline{U}(s) \quad (4-4)$$

where \underline{I} is the identity matrix. The rest of the work involves finding the \underline{A} and \underline{B} matrices and determining the inverse Laplace transformation. [7]

Derivation

The proposed operation of the inverter demands the existence of five circuit modes. For the inverter shown in Fig. 2-1 the five modes are shown in Figures 4-1 through 4-5. The network topology is the same for Modes two through five thus only one state equation is necessary to extract a solution for these modes, as only one SCR is allowed to fire at a time and the current must clear the energized SCR prior to any subsequent firing. Mode one is the idle mode which describes the inverter when all SCR current has cleared and no other SCR is energized.

Notice that the capacitor voltages in the loop not containing the SCR being energized are dependent variables. These capacitor voltages are determined in the following manner. The current through each capacitor is equal since they are in series. Each capacitor has the same capacitive value thus the voltage change across each is the same. The state equations, as developed, assumed

these capacitors to be lumped into one capacitor, and since the voltage change is known, then each capacitor will have exactly one half of the voltage change seen across the series combination. This voltage change across each capacitor is determined and the appropriate initial condition is summed to it to produce the value of voltage across each capacitor. This insures that the proper initial condition exists when the mode changes.

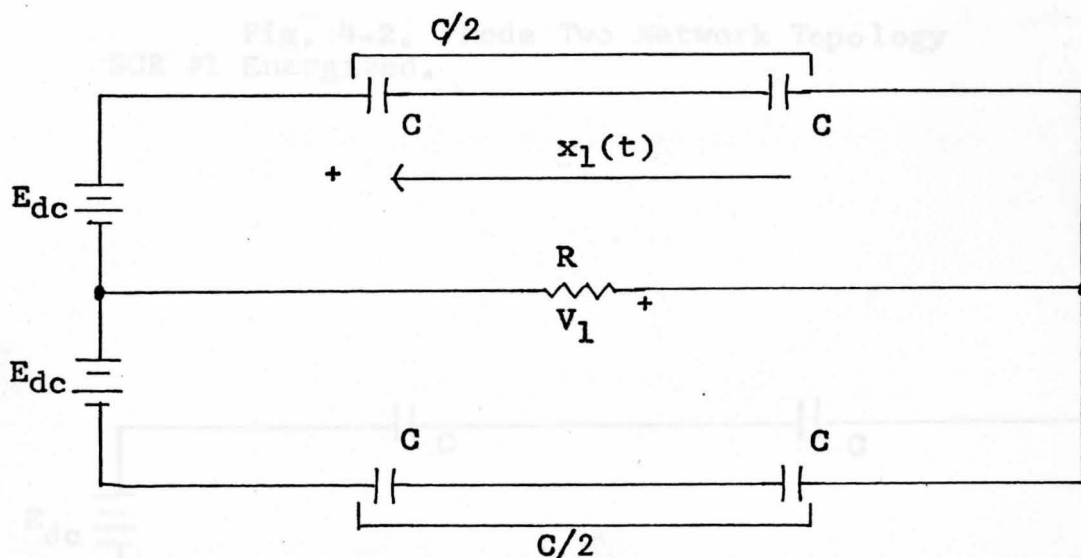


Fig. 4-1. Mode One Network Topology: No SCR's Energized.

The state solution for this mode becomes

$$\dot{x}_1(t) = -1/(RC) x_1(t) + E_{dc}/(RC) \quad (4-5)$$

Fig. 4-3. Mode Three Network Topology
SCR #3 Energized.

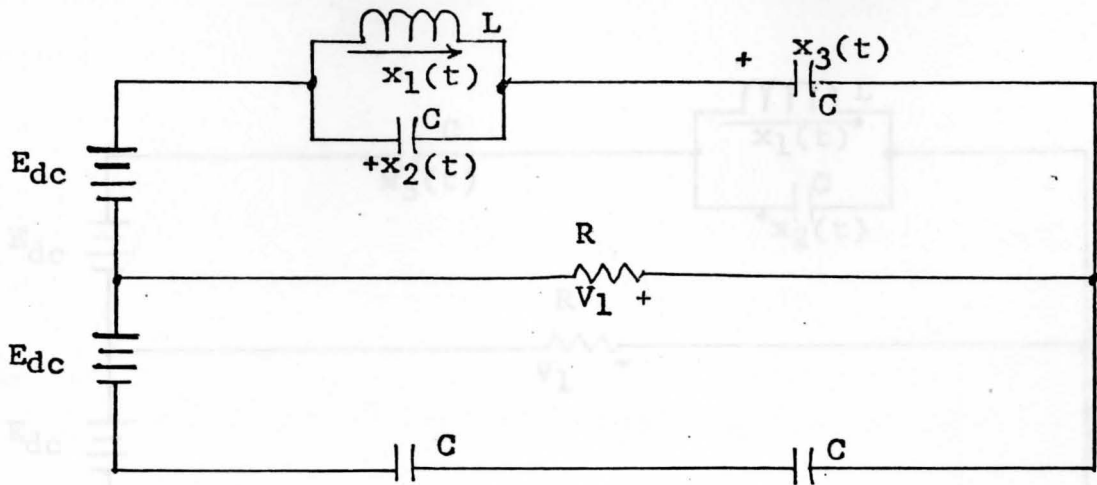


Fig. 4-2. Mode Two Network Topology
SCR #1 Energized.

Fig. 4-4. Mode Four Network Topology
SCR #3 Energized.

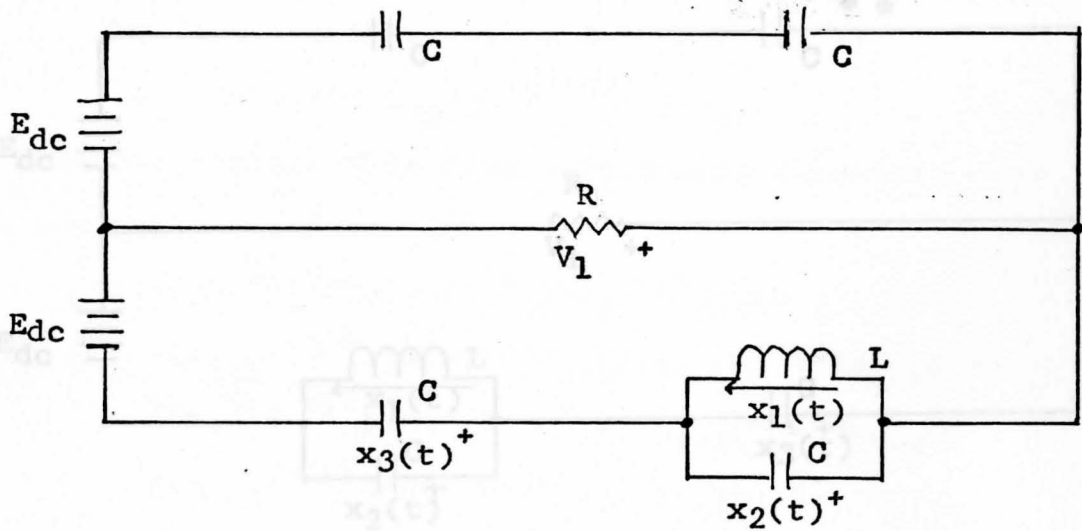


Fig. 4-3. Mode Three Network Topology
SCR #2 Energized.

The state variable solution for Modes Two through Five becomes

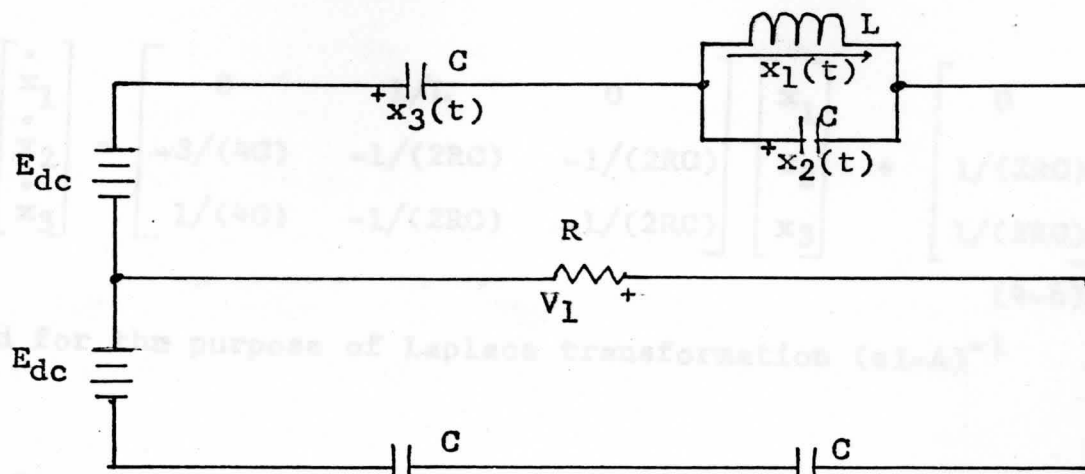


Fig. 4-4. Mode Four Network Topology
SCR #3 Energized.

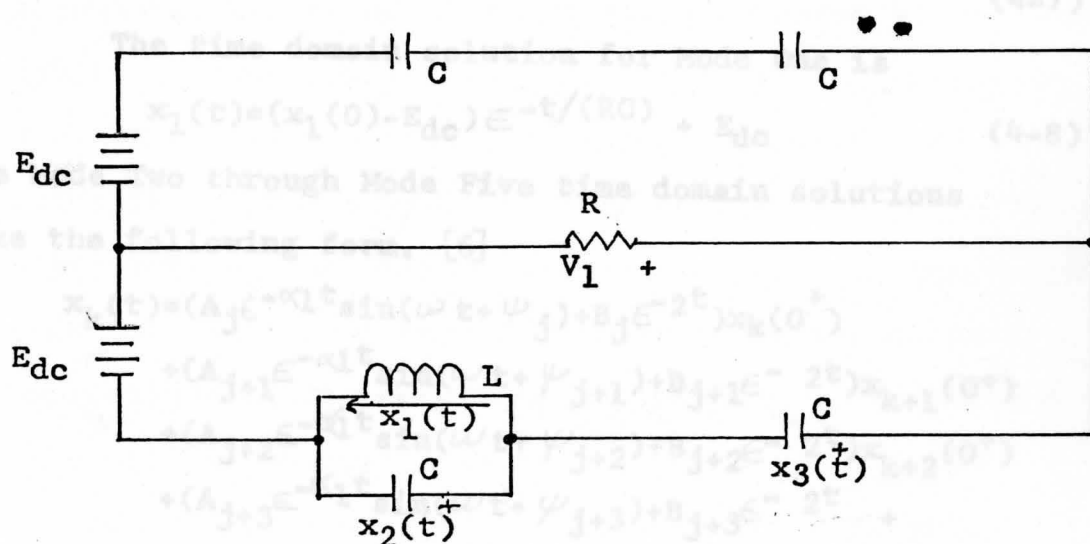


Fig. 4-5. Mode Five Network Topology
SCR #4 Energized

The state variable solution for Modes Two through Five becomes

$$\begin{bmatrix} \dot{x}_1 \\ \dot{x}_2 \\ \dot{x}_3 \end{bmatrix} = \begin{bmatrix} 0 & 1/L & 0 \\ -3/(4C) & -1/(2RC) & -1/(2RC) \\ 1/(4C) & -1/(2RC) & -1/(2RC) \end{bmatrix} \begin{bmatrix} x_1 \\ x_2 \\ x_3 \end{bmatrix} + \begin{bmatrix} 0 \\ 1/(2RC) \\ 1/(2RC) \end{bmatrix} E_{dc} \tag{4-6}$$

and for the purpose of Laplace transformation $(sI-A)^{-1}$ is

$$\begin{bmatrix} (s^2+s/(RC)) & (s/L)+(1/(2RLC)) & -1/(2RLC) \\ (-3s/(4C))-(1/(2RC^2)) & (s^2+s/(2RC)) & -s/(2RC) \\ (s/(4C))+(1/(2RC^2)) & (-s/(2RC)+1/(4LC)) & s^2+s/(2RC)+3/(4LC) \end{bmatrix}$$

$$s^3 + (s^2/(RC)) + (3s/(4LC)) + 1/(2RLC^2) \tag{4-7}$$

The time domain solution for Mode One is

$$x_1(t) = (x_1(0) - E_{dc}) e^{-t/(RC)} + E_{dc} \tag{4-8}$$

The Mode Two through Mode Five time domain solutions take the following form. [6]

$$\begin{aligned} x_k(t) = & (A_j e^{-\alpha_1 t} \sin(\omega t + \psi_j) + B_j e^{-2t}) x_k(0^+) \\ & + (A_{j+1} e^{-\alpha_1 t} \sin(\omega t + \psi_{j+1}) + B_{j+1} e^{-2t}) x_{k+1}(0^+) \\ & + (A_{j+2} e^{-\alpha_1 t} \sin(\omega t + \psi_{j+2}) + B_{j+2} e^{-2t}) x_{k+2}(0^+) \\ & + (A_{j+3} e^{-\alpha_1 t} \sin(\omega t + \psi_{j+3}) + B_{j+3} e^{-2t} + B_k) E_{dc} \end{aligned} \tag{4-9}$$

The load voltage becomes simply

$$V_1 = -E_{dc} + V_{C1} + V_{C3} \tag{4-10}$$

Results

Fig. 4-6 shows the typical transient waveshapes for a steady state operating condition. The per unit values are based on the data tabulated in Table I. As expected, the voltage across the capacitor associated with the SCR just previously fired retains its voltage for one half cycle of repetition rate thus insuring a reverse voltage across the SCR which is necessary to prevent a commutation failure.

The load voltage is plotted in Fig. 4-7 and is compared with the load voltage obtained from the Fourier analysis. Fig. 4-8 through 4-10 show the RMS load current at a 10000. Hz. repetition rate as a function of load resistance. These results are again compared to the results of the Fourier analysis. The rest of the plots show the kilowatt output versus frequency and load resistance. It should be noted that only a 3 to 5% error exists between the state variable analysis and the Fourier analysis. This fact became evident early in the data compilation and for comparing the results it was deemed reasonable to only examine the extreme values of load resistance for each series component set, for various repetition rates. At the nominal repetition rate, 10000. Hz., each value of load resistance was examined.

Magnitude (Per Unit)

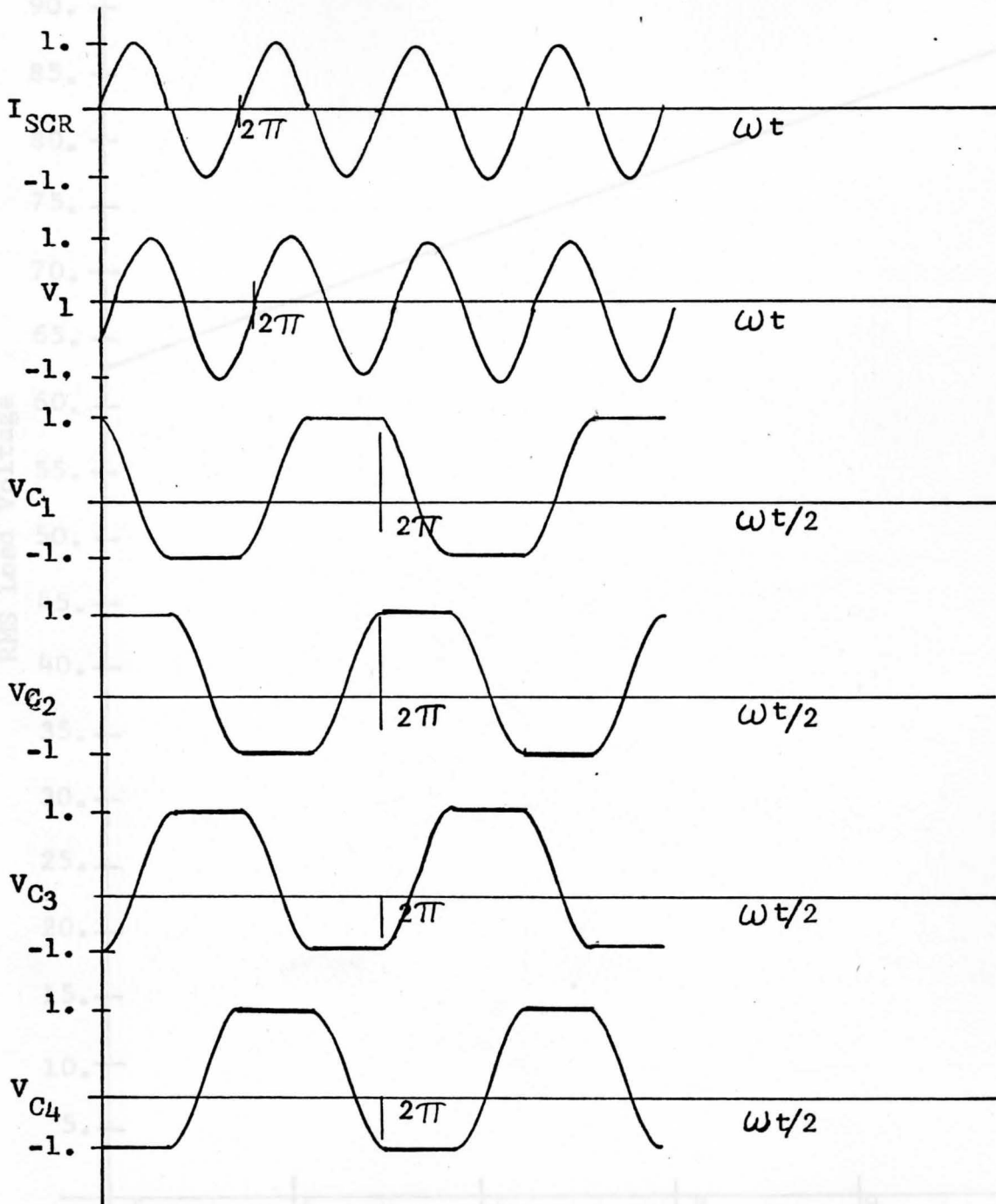


Fig. 4-6. Typical Transient Waveforms for the Inverter.

Fig. 4-7. RMS Load Voltage Versus Repetition Rate for All Load Conditions and Series Components.

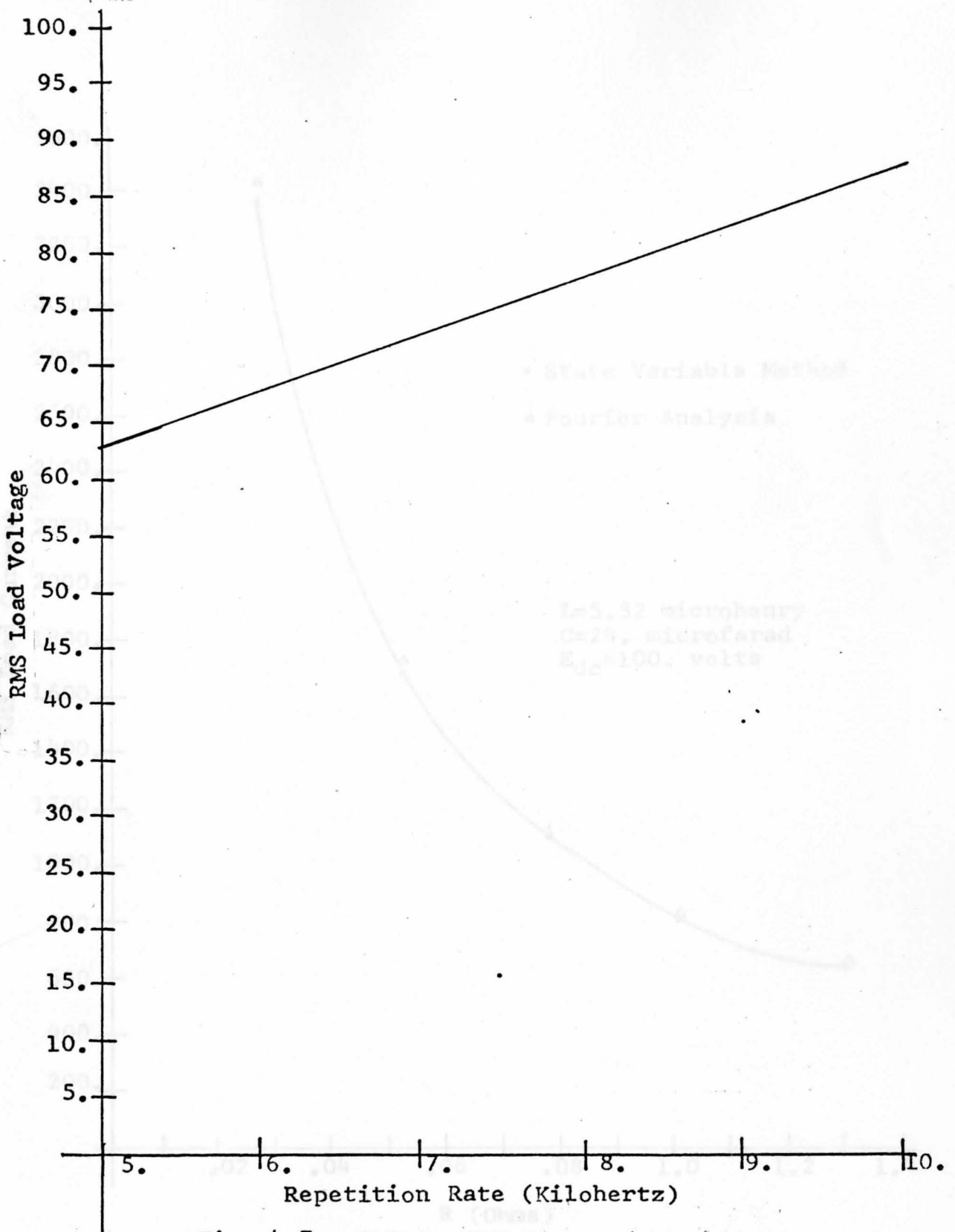


Fig. 4-7. RMS Load Voltage Versus Repetition Rate for All Load Conditions and Series Components.

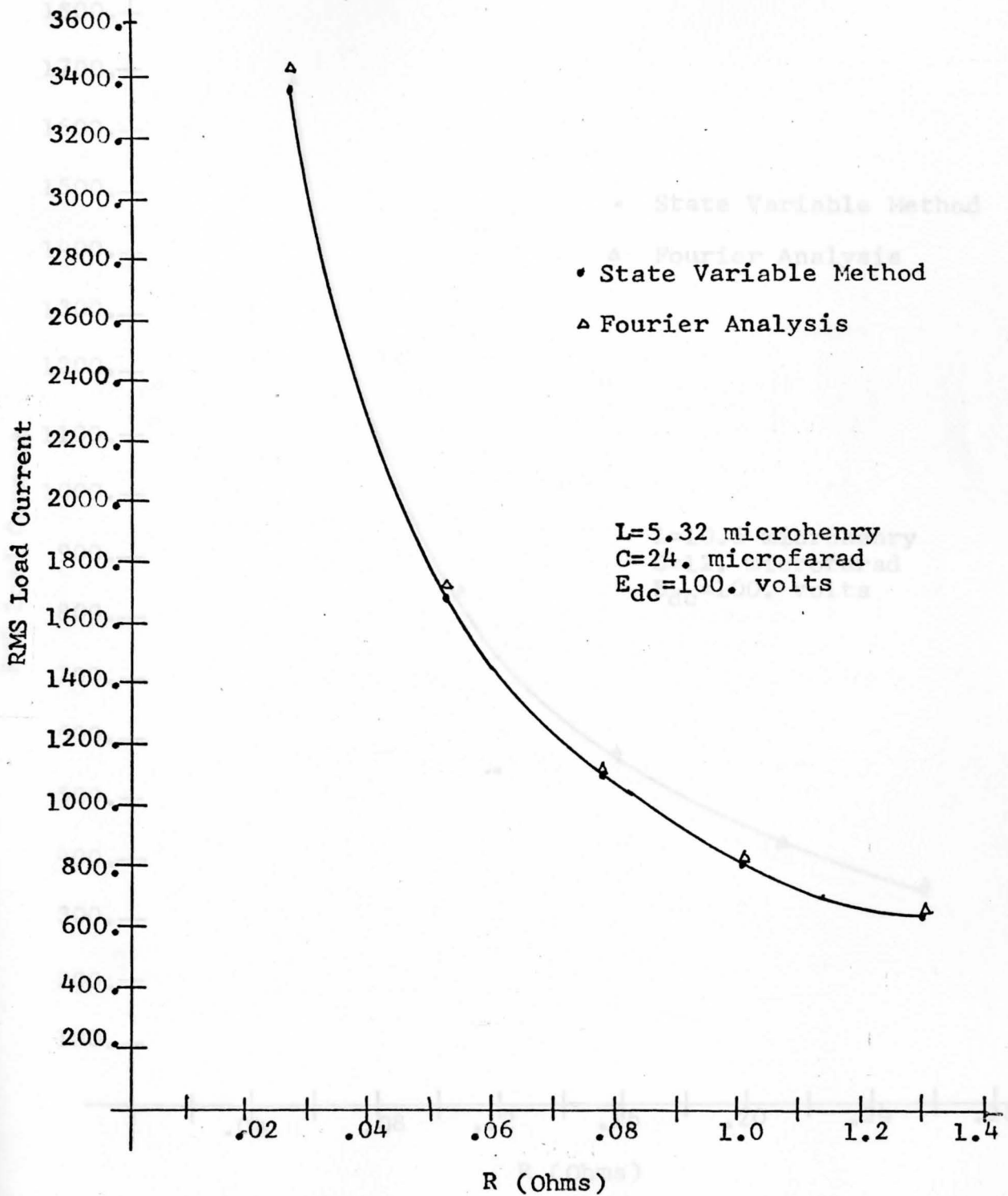


Fig. 4-8. Load Current (RMS) Versus Load Resistance at 10000. Hz.

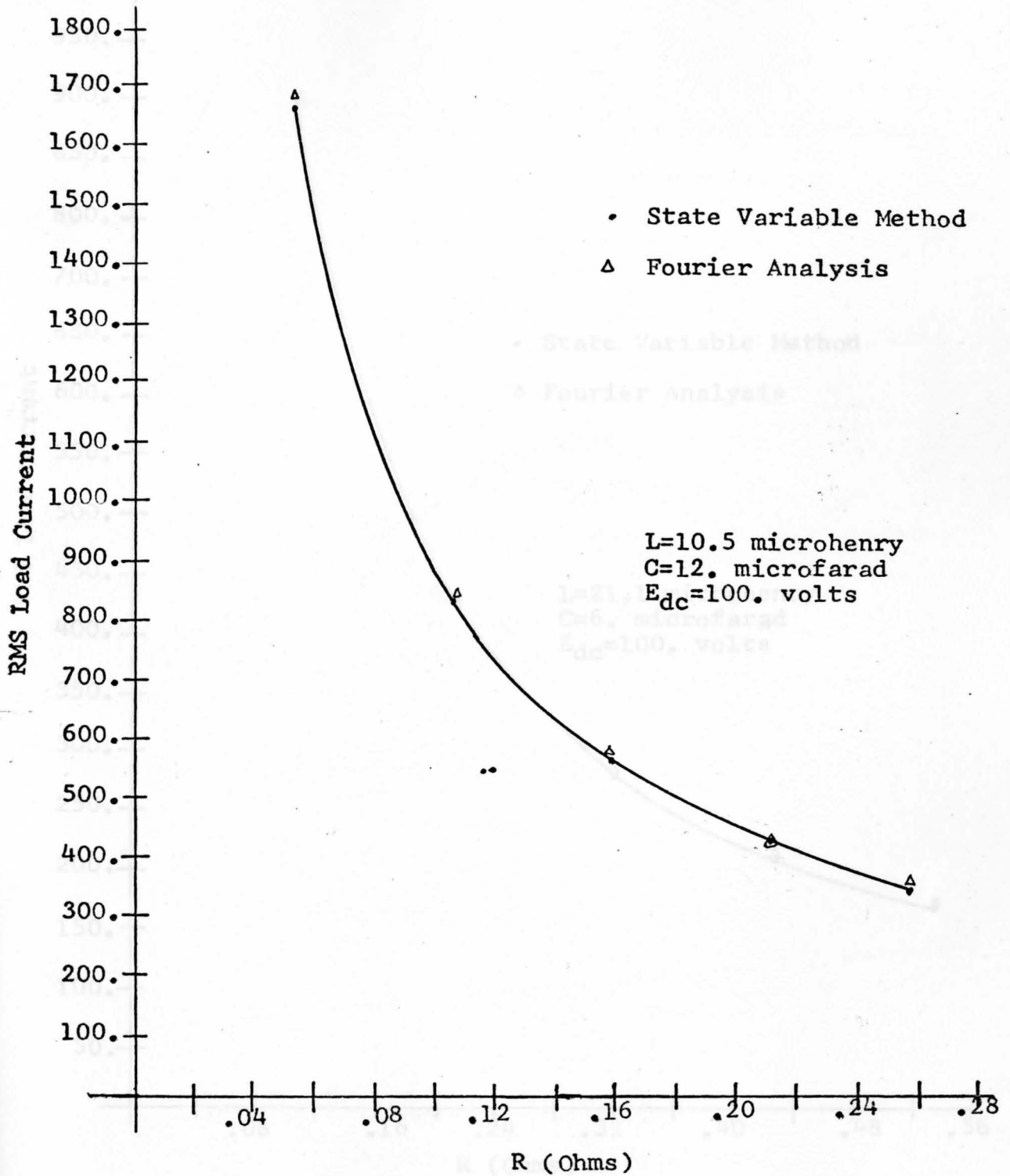


Fig. 4-9. Load Current (RMS) Versus Load Resistance at 10000. Hz.

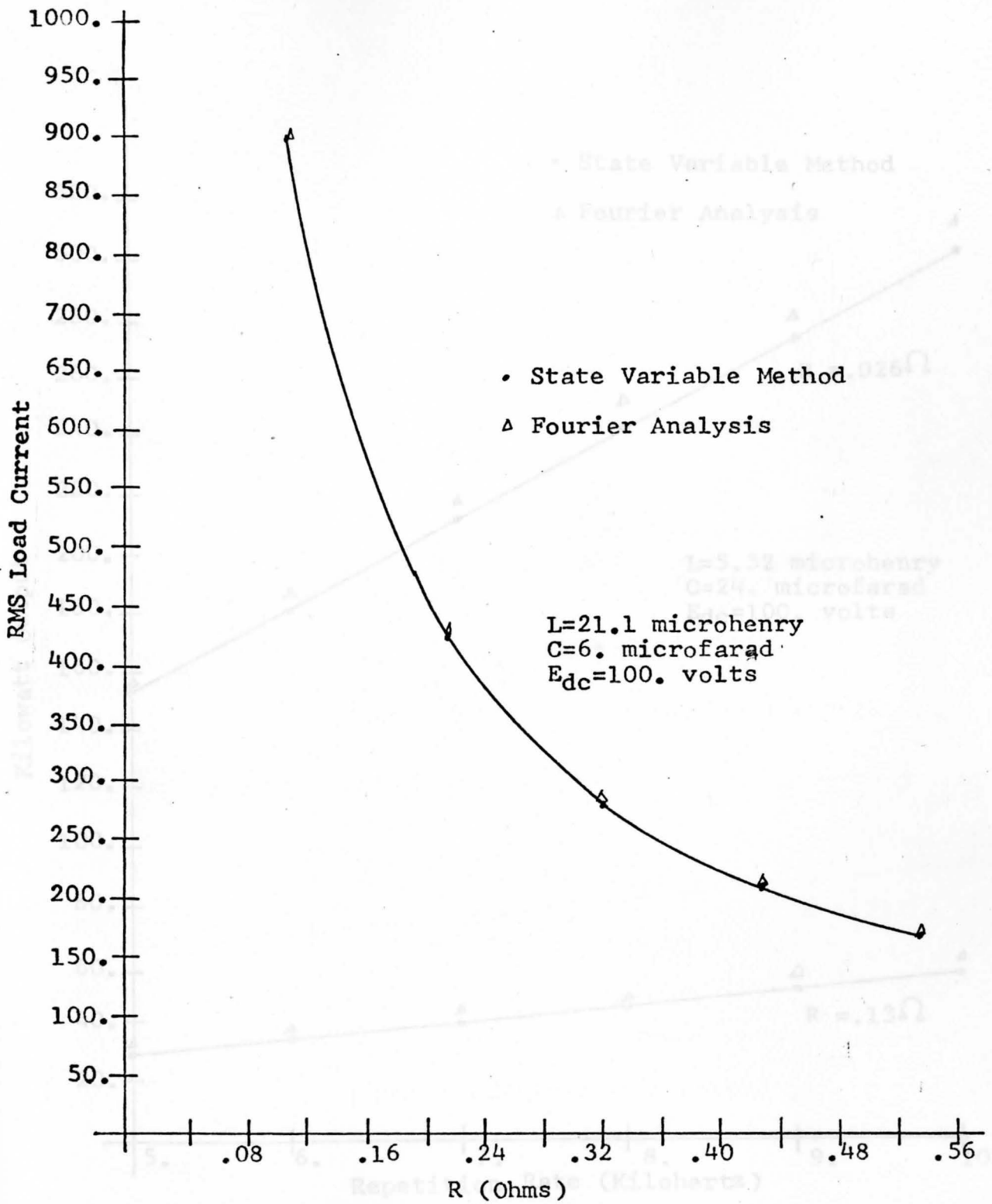


Fig. 4-10. Load Current (RMS) Versus Load Resistance at 10000. Hz.

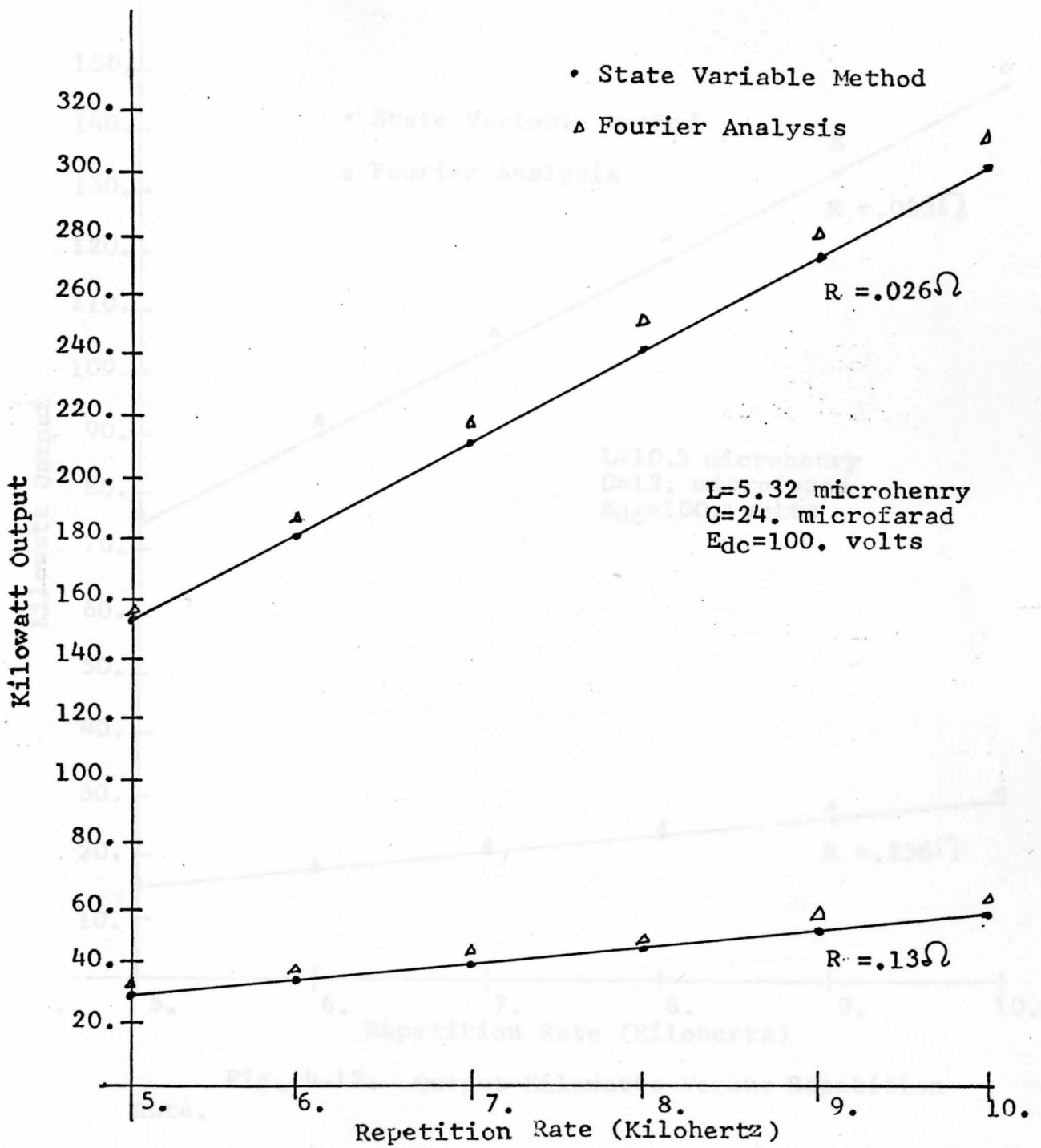


Fig. 4-11. Output Kilowatts Versus Repetition Rate.

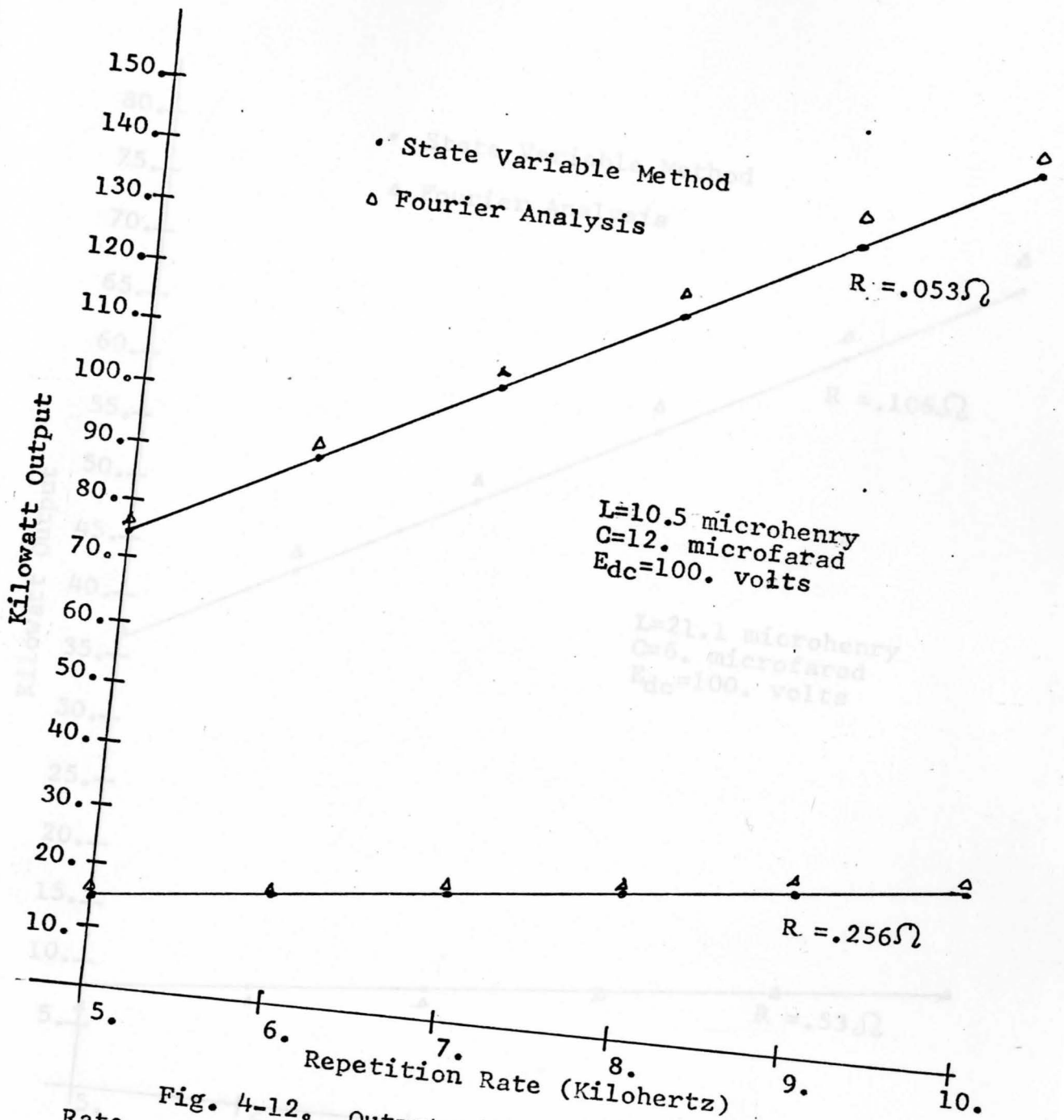


Fig. 4-12. Output Kilowatts Versus Repetition Rate.

Fig. 4-13. Output Kilowatts Versus Repetition Rate.

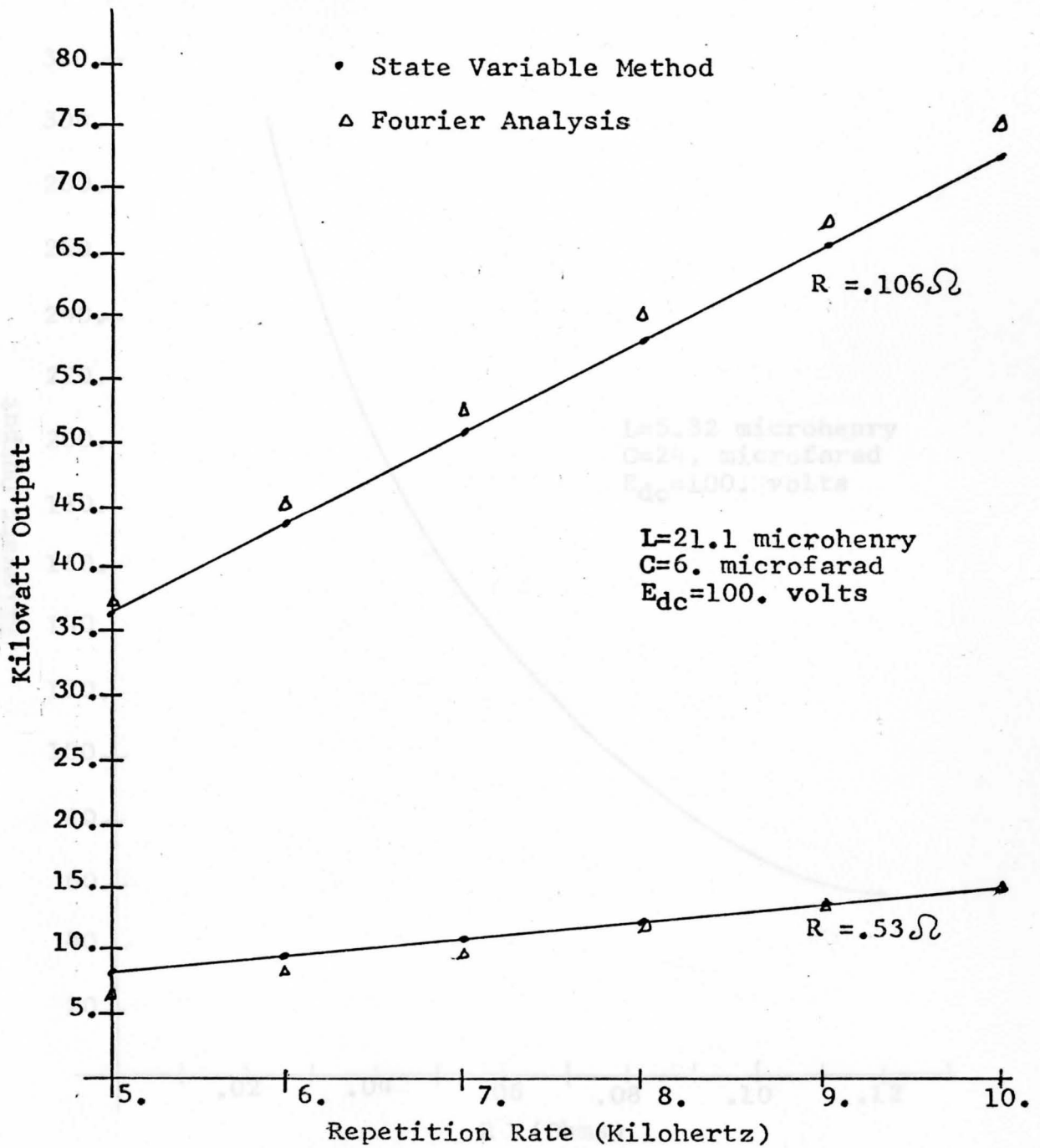


Fig. 4-13.. Output Kilowatts Versus Repetition Rate.

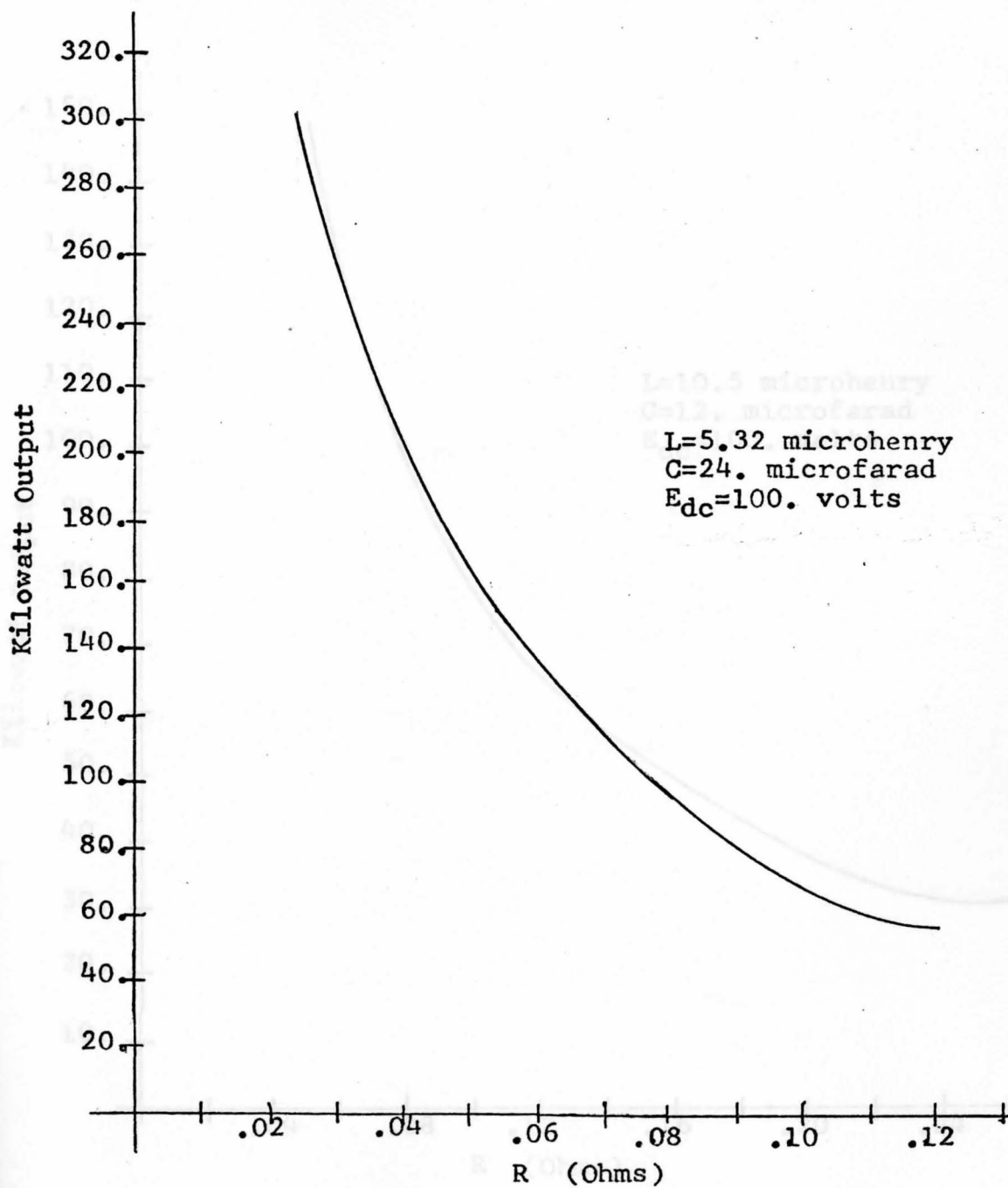


Fig. 4-14. Output Kilowatts Versus Load Resistance at 10000. Hz.

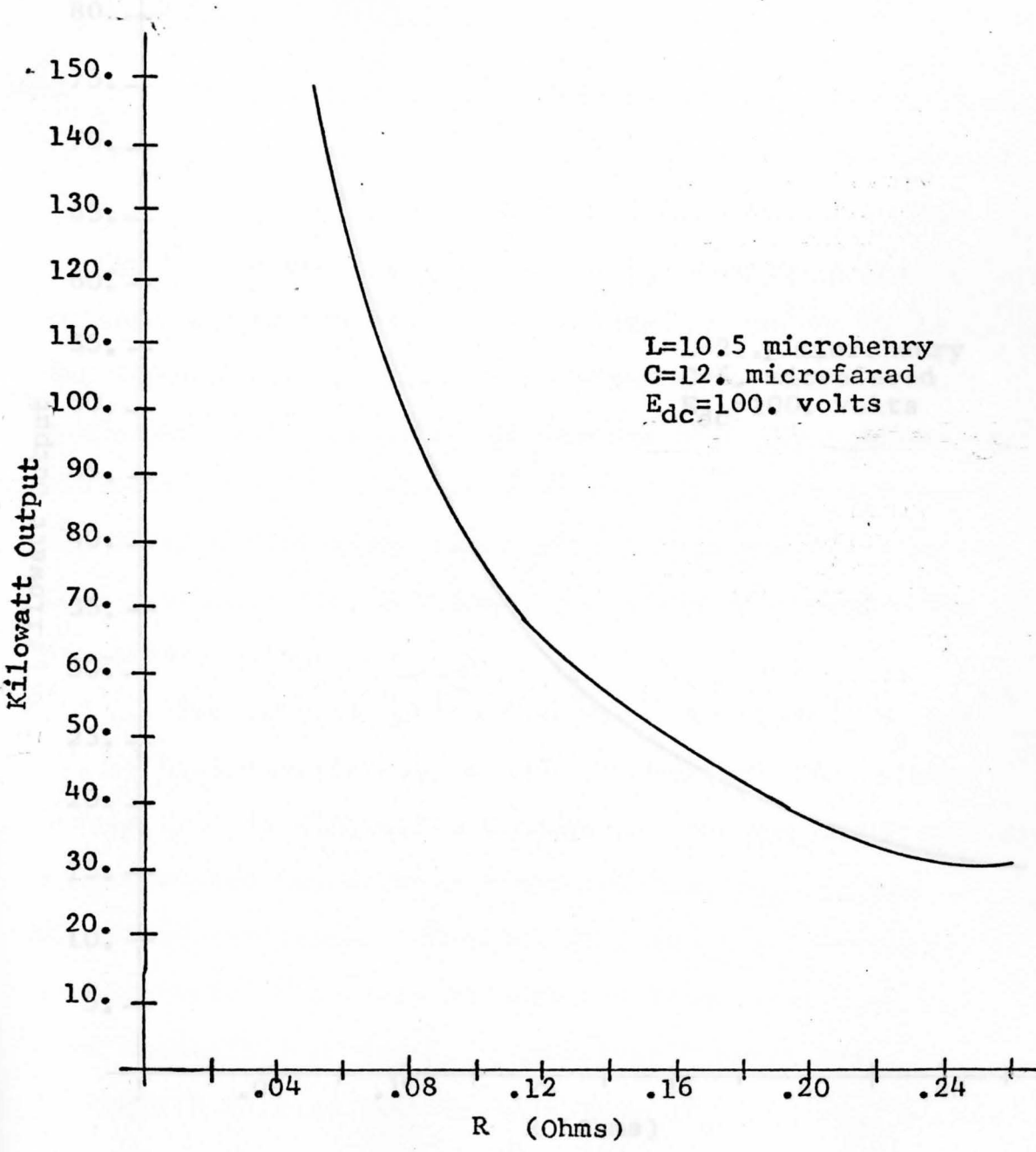


Fig. 4-15. Output Kilowatts Versus Load Resistance at 10000. Hz.

CHAPTER V

CLAMPING OF THE INVERTER

Introduction

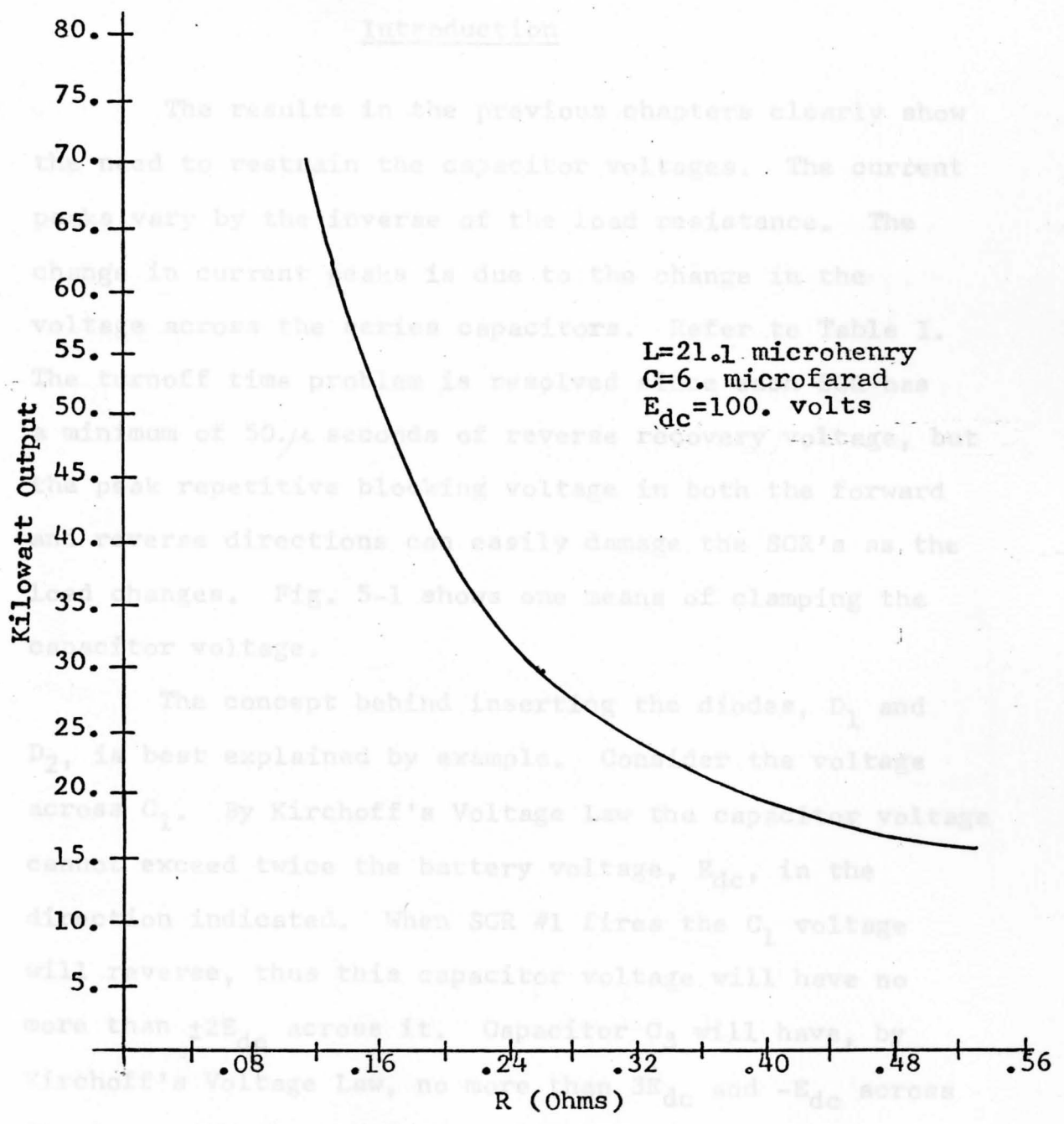


Fig. 4-16. Output Kilowatts Versus Load Resistance at 10000. Hz.

CHAPTER V

CLAMPING OF THE INVERTER

Introduction

The results in the previous chapters clearly show the need to restrain the capacitor voltages. The current peaks vary by the inverse of the load resistance. The change in current peaks is due to the change in the voltage across the series capacitors. Refer to Table I. The turnoff time problem is resolved since each SCR has a minimum of 50μ seconds of reverse recovery voltage, but the peak repetitive blocking voltage in both the forward and reverse directions can easily damage the SCR's as the load changes. Fig. 5-1 shows one means of clamping the capacitor voltage.

The concept behind inserting the diodes, D_1 and D_2 , is best explained by example. Consider the voltage across C_1 . By Kirchoff's Voltage Law the capacitor voltage cannot exceed twice the battery voltage, E_{dc} , in the direction indicated. When SCR #1 fires the C_1 voltage will reverse, thus this capacitor voltage will have no more than $\pm 2E_{dc}$ across it. Capacitor C_3 will have, by Kirchoff's Voltage Law, no more than $3E_{dc}$ and $-E_{dc}$ across it, due to the conduction of D_1 . The same situation holds for the lower series loop. Fig. 5-2 shows the waveshapes

expected when the load resistance is zero.

Development of Clamping Analysis

For the configuration shown in Fig. 5-1 there are a minimum of sixteen modes of operation. For the purpose of analysis, no SCR is allowed to conduct until the current has cleared from the last conducting SCR, and no SCR is allowed to fire until the current has essentially cleared from any conducting clamping diodes. Figures 4-1 through 4-5 show the Mode 1, 2, 3, 4, and 5 topologies. The new modes are shown in Figures 5-3 through 5-14 along with their respective state equations.

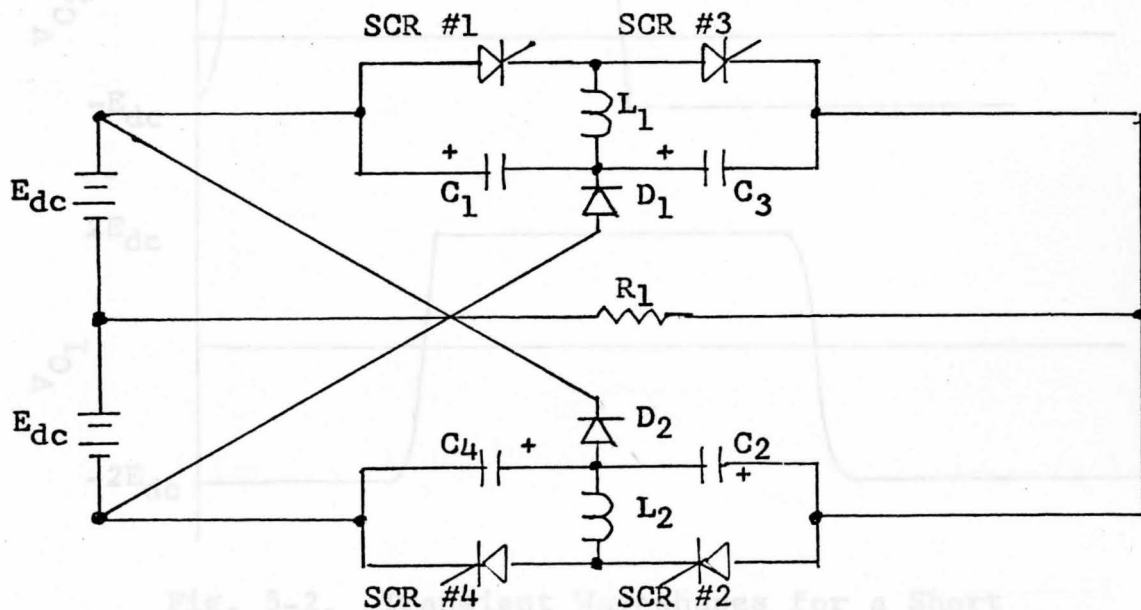


Fig. 5-1. Inverter Circuit With Diode Clamping.

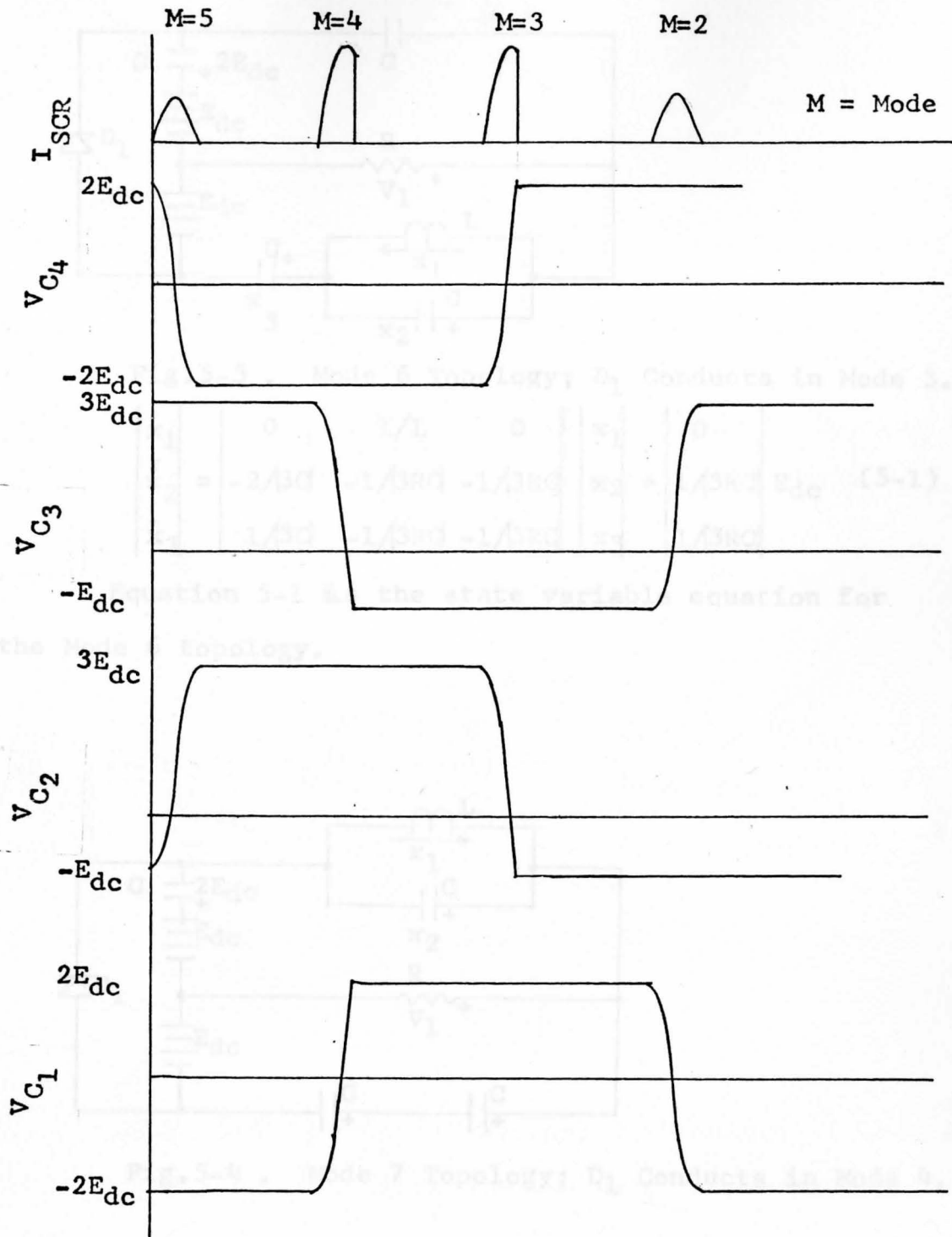


Fig. 5-2. Transient Waveshapes for a Short Circuited Load.

Equation 5-2 is the state variable equation for the Mode 7 topology.

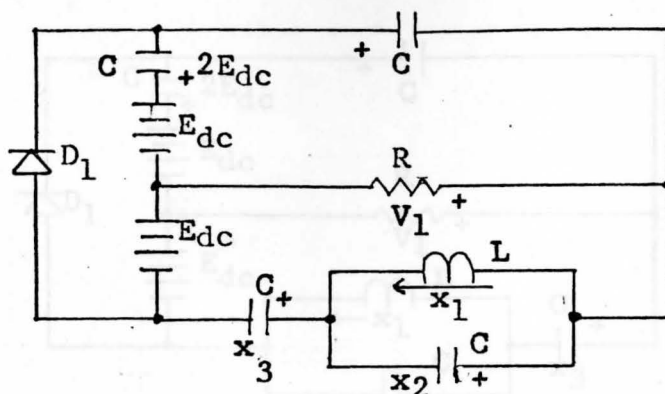


Fig.5-3 . Mode 6 Topology; D_1 Conducts in Mode 3.

$$\begin{bmatrix} \dot{x}_1 \\ \dot{x}_2 \\ \dot{x}_3 \end{bmatrix} = \begin{bmatrix} 0 & 1/L & 0 \\ -2/3C & -1/3RC & -1/3RC \\ 1/3C & -1/3RC & -1/3RC \end{bmatrix} \begin{bmatrix} x_1 \\ x_2 \\ x_3 \end{bmatrix} + \begin{bmatrix} 0 \\ 1/3RC \\ 1/3RC \end{bmatrix} E_{dc} \quad (5-1)$$

Equation 5-1 is the state variable equation for the Mode 6 topology.

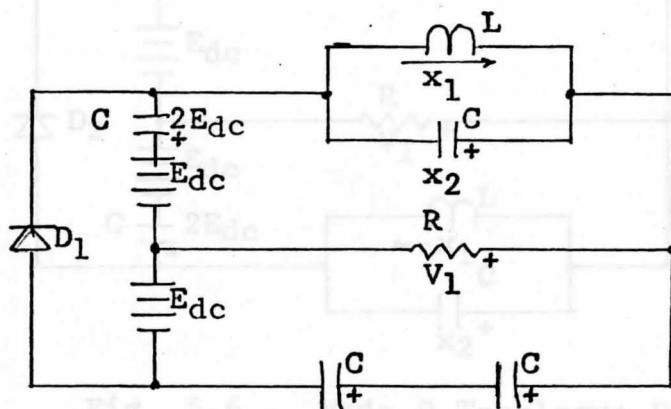


Fig.5-4 . Mode 7 Topology; D_1 Conducts in Mode 4.

$$\begin{bmatrix} \dot{x}_1 \\ \dot{x}_2 \end{bmatrix} = \begin{bmatrix} 0 & 1/L \\ -2/3C & -2/3RC \end{bmatrix} \begin{bmatrix} x_1 \\ x_2 \end{bmatrix} + \begin{bmatrix} 0 \\ -2/3RC \end{bmatrix} E_{dc} \quad (5-2)$$

Equation 5-2 is the state variable equation for the Mode 7 topology.

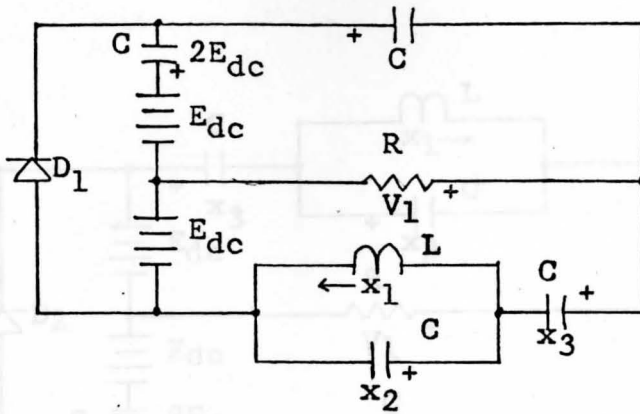


Fig.5-5 . Mode 8 Topology; D_1 Conducts in Mode 5.

The state equations are the same as for Mode 6.

Mode 4.

The state equations are the same as for Mode 6.

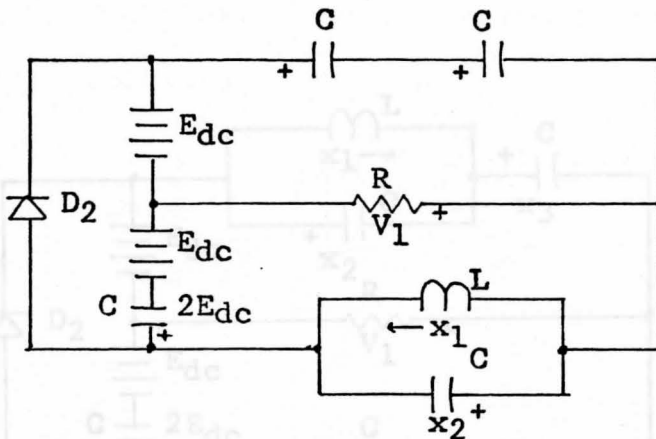


Fig. 5-6 . Mode 9 Topology; D_2 Conducts in Mode 3.

The state equations are the same as for Mode 7.

The state equations are the same as for Mode 6.

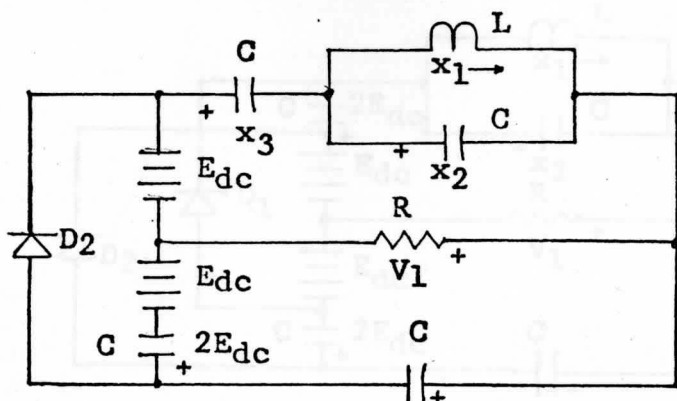
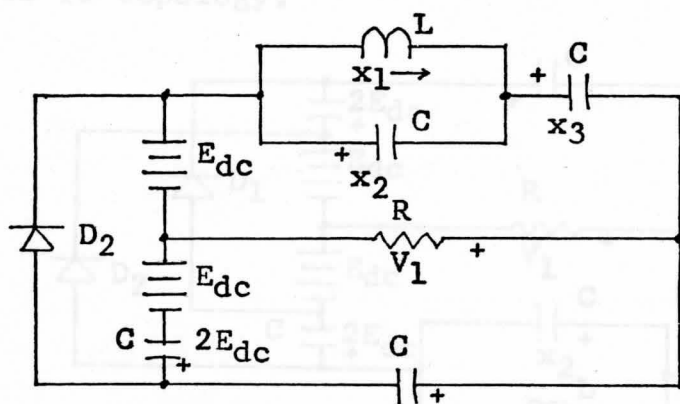


Fig. 5-7 . Mode 10 Topology; D_2 Conducts in Mode 4.

The state equations are the same as for Mode 6.



2. Fig. 5-8 . Mode 11 Topology; D_2 Conducts in Mode

The state equations are the same as for Mode 6.

The state equations are the same as for Mode 11.

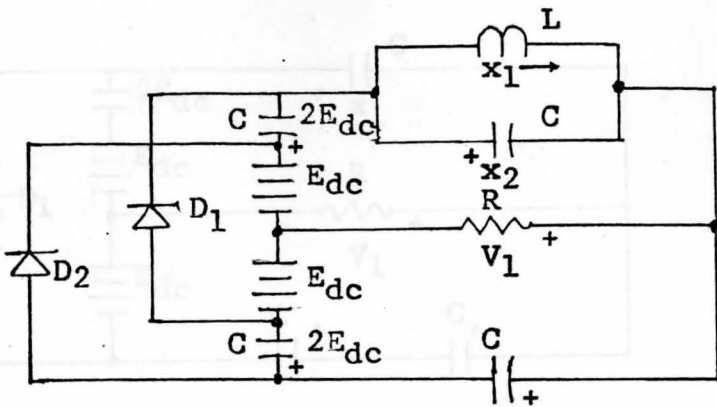


Fig. 5-9 . Mode 12 Topology; D_1 and D_2 Conduct in Mode 4.

$$\begin{bmatrix} \dot{x}_1 \\ \dot{x}_2 \end{bmatrix} = \begin{bmatrix} 0 & 1/L \\ -1/2C & -1/2RC \end{bmatrix} \begin{bmatrix} x_1 \\ x_2 \end{bmatrix} + \begin{bmatrix} 0 \\ -1/2RC \end{bmatrix} E_{dc} \quad (5-3)$$

Equation 5-3 is the state variable equation for the Mode 12 topology.

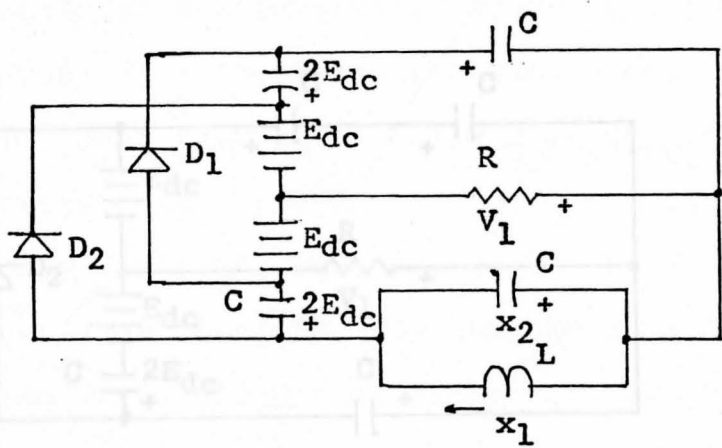


Fig. 5-10. Mode 13 Topology; D_1 and D_2 Conduct in Mode 3.

The state equations are the same as for Mode 12.

The state equations are the same as for Mode 14.

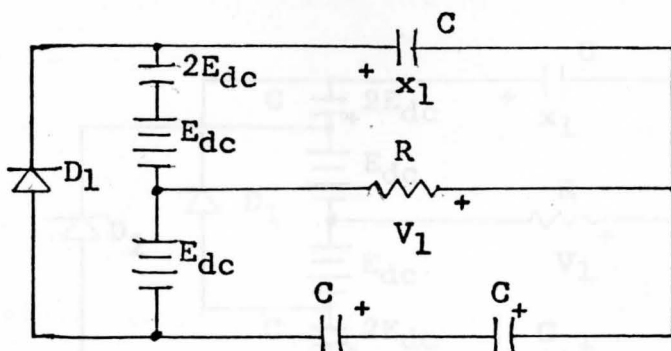


Fig. 5-11. Mode 14 Topology; No SCR's Are Conducting and D_1 Conducts.

$$\dot{x}_1 = -2/3RC x_1 - 2/3RC E_{dc} \quad (5-4)$$

Equation 5-4 is the state variable equation for the Mode 14 topology.

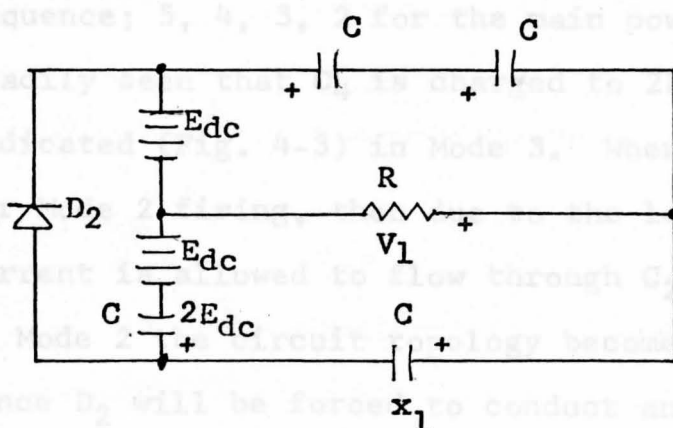


Fig. 5-12. Mode 15 Topology; No SCR's Are Conducting and D_2 Conducts.

The state equations are the same as for Mode 14.

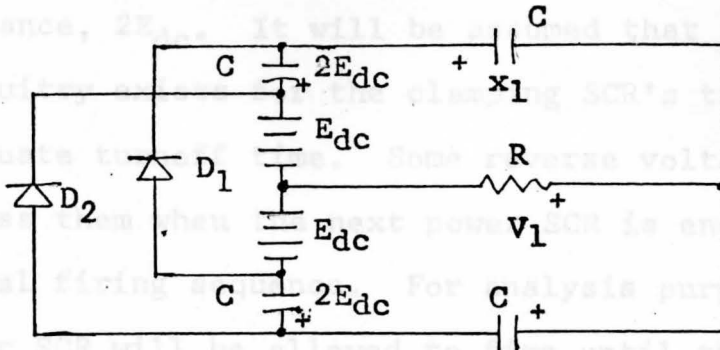


Fig. 5-13. Mode 16 Topology; No SCR's Are Conducting and Both D_1 and D_2 Conduct.

$$\dot{x}_1 = -1/2RC \ x_1 - 1/2RC \ E_{dc} \quad (5-5)$$

Equation 5-5 is the state variable equation for the Mode 16 topology.

Inserting a load resistance results in asymmetric operation of the inverter. By using the mode firing sequence; 5, 4, 3, 2 for the main power SCR's it is readily seen that C_4 is charged to $2E_{dc}$ in the direction indicated (Fig. 4-3) in Mode 3. When SCR #1 energizes for Mode 2 firing, then due to the load resistor a current is allowed to flow through C_2 and C_4 . Instead of Mode 2 the circuit topology becomes that of Mode 11, since D_2 will be forced to conduct and since V_{C_4} cannot exceed $2E_{dc}$ the modes of operation then become; 5, 4, 7, 14, 3, 9, 15, 11, 15. The modes wherein a power SCR fires is underlined.

This asymmetry can be eliminated by replacing

D_1 and D_2 by SCR's. These clamping SCR's can be fired when C_1 and C_4 reach the appropriate voltage, in this instance, $2E_{dc}$. It will be assumed that the proper circuitry exists for the clamping SCR's to insure adequate turnoff time. Some reverse voltage will exist across them when the next power SCR is energized in the normal firing sequence. For analysis purposes, no power SCR will be allowed to fire until the clamping current is essentially nil. A typical waveform for this operation is shown in Fig. 5-14. The only modes allowed are 1, 2, 3, 4, 5, 7, 9, 14, and 15.

Fourier Analysis

Turning to Fig. 5-2 it seemed reasonable to perform a Fourier analysis on the inverter under the SCR clamping conditions. This analysis was intended to be only an approximation. From equation 2-9 and Fig. 5-2 it was approximated that the average peak current would be

$$I_{P_{ave}} = 2.5E_{dc}\sqrt{C/(2L)} \quad (5-5)$$

The same equations from the Fourier analysis of Chapter III will still hold for the inverter. Figures 5-15 through 5-21 show the results of this analysis.

Fig. 5-14. Typical Transient Waveforms for a resistive load.

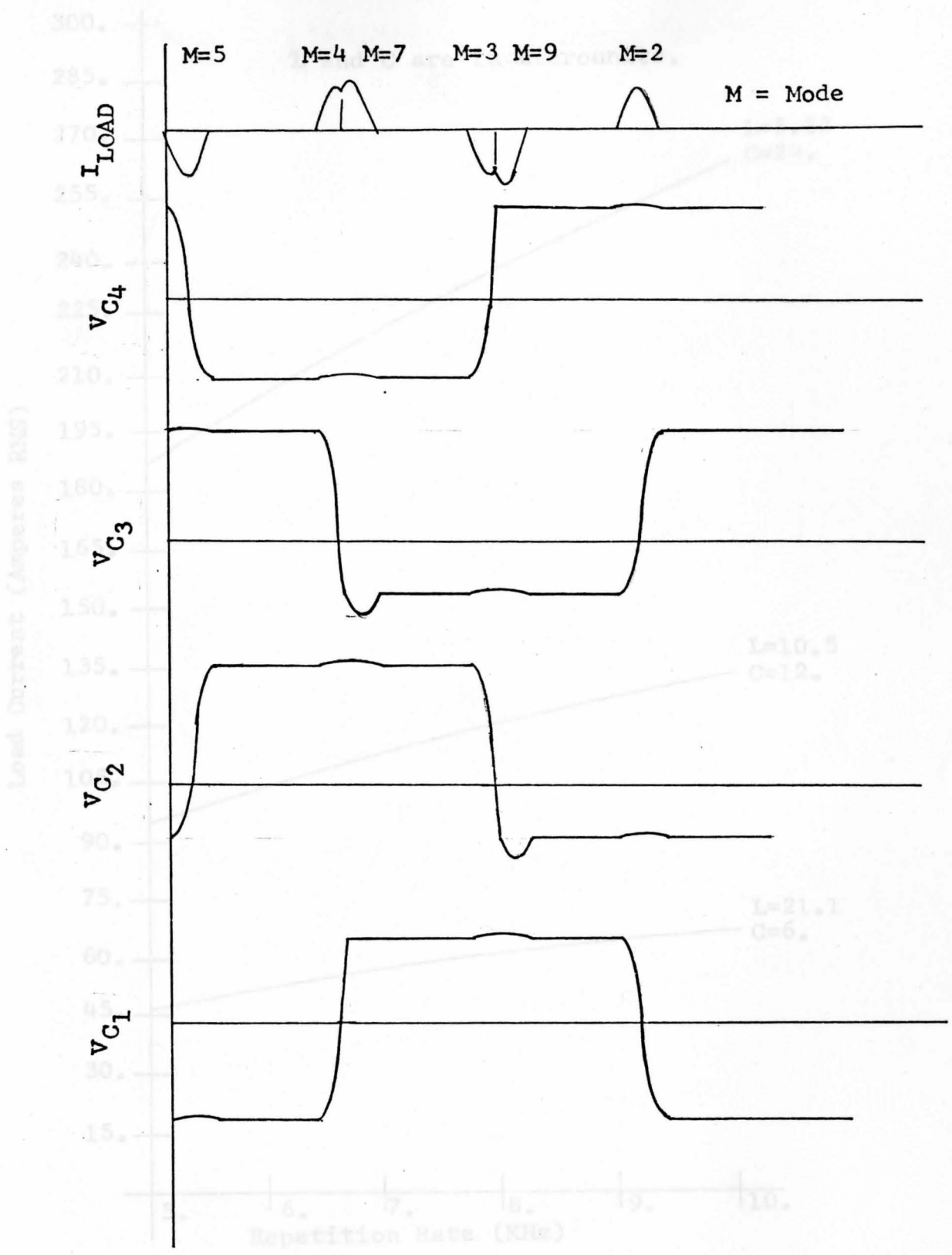


Fig. 5-14. Typical Transient Waveforms for a Resistive Load.

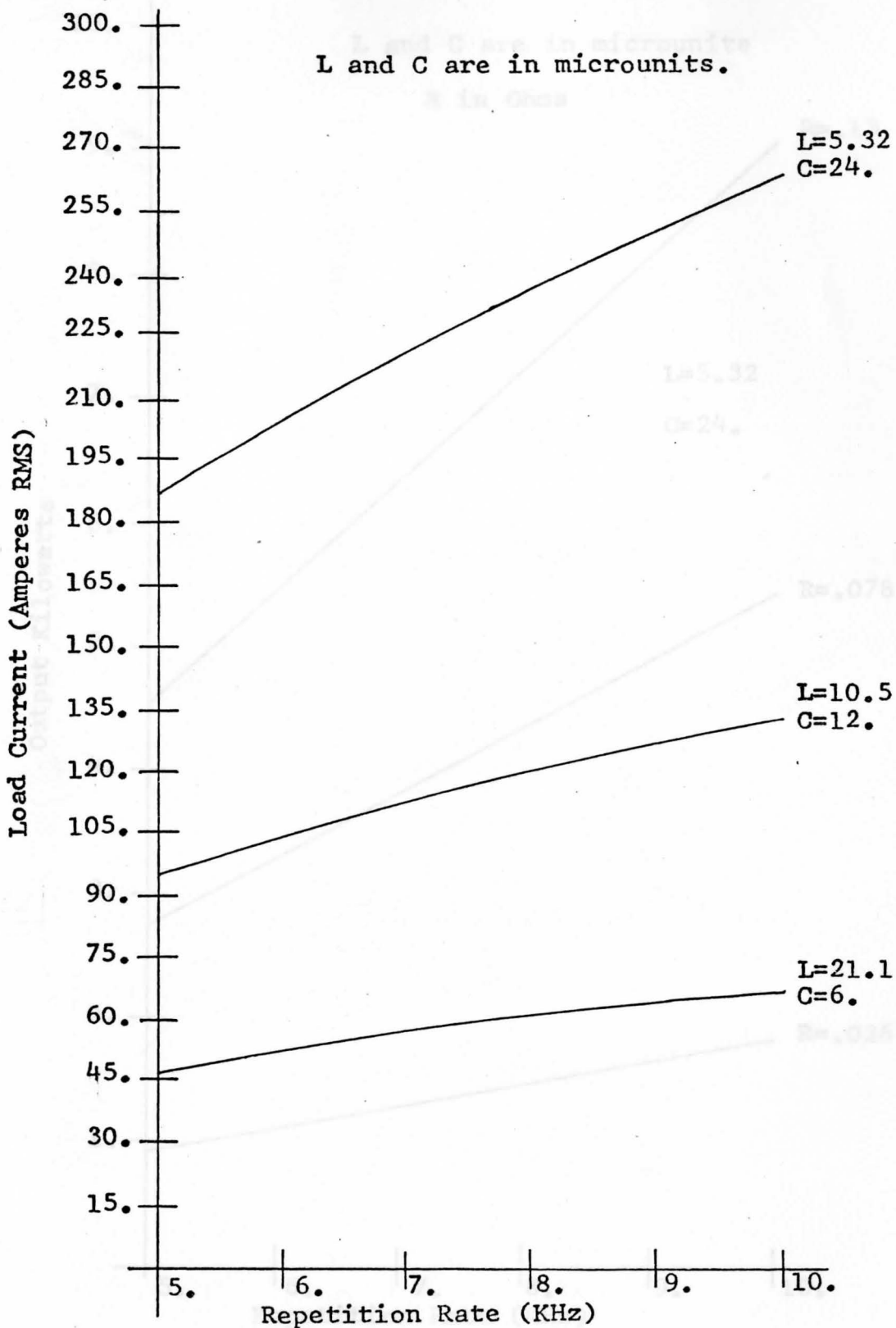


Fig. 5-15. RMS Load Current Versus Repetition Rate.

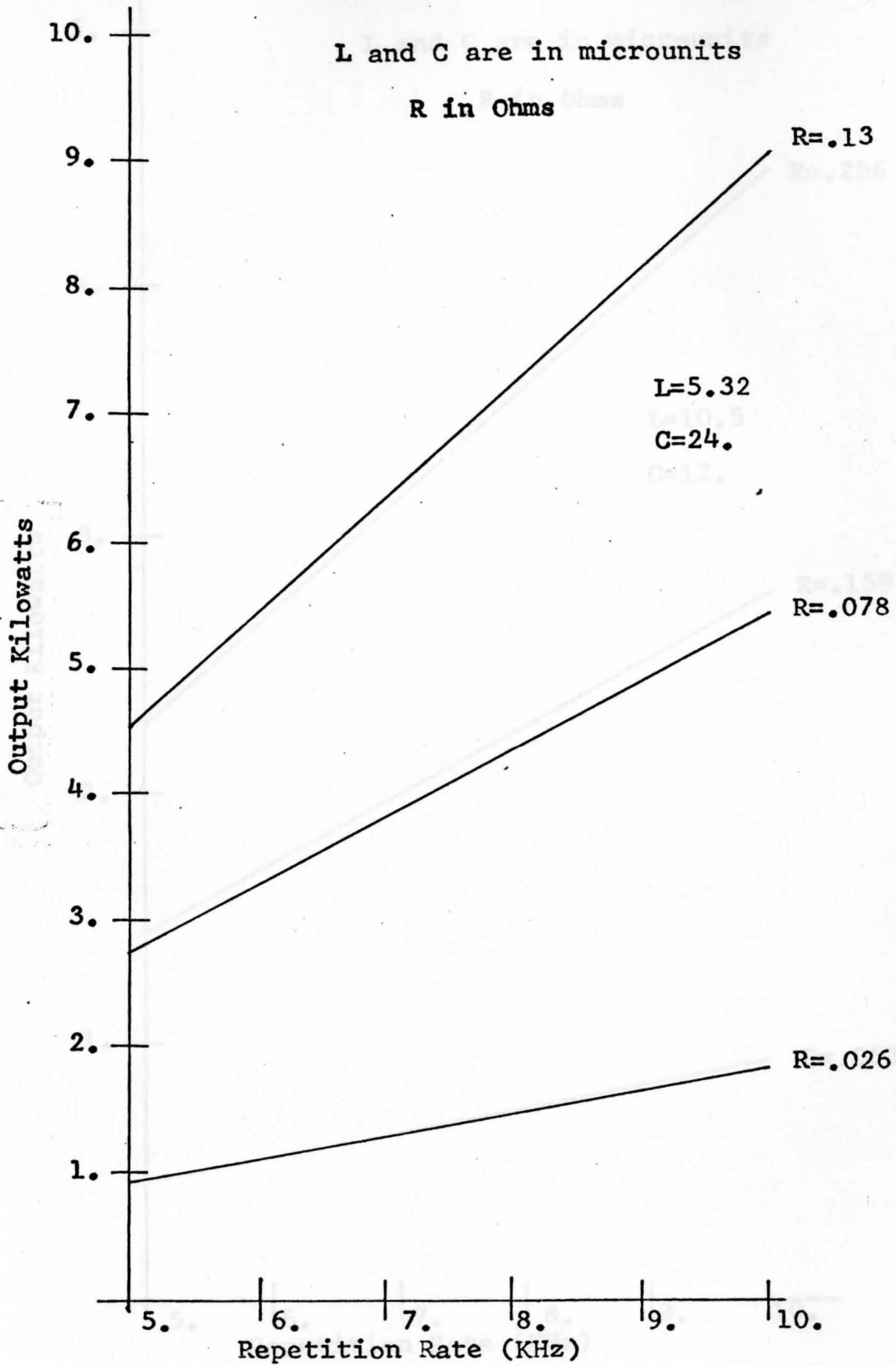


Fig. 5-16. Kilowatt Output Versus Repetition Rate.

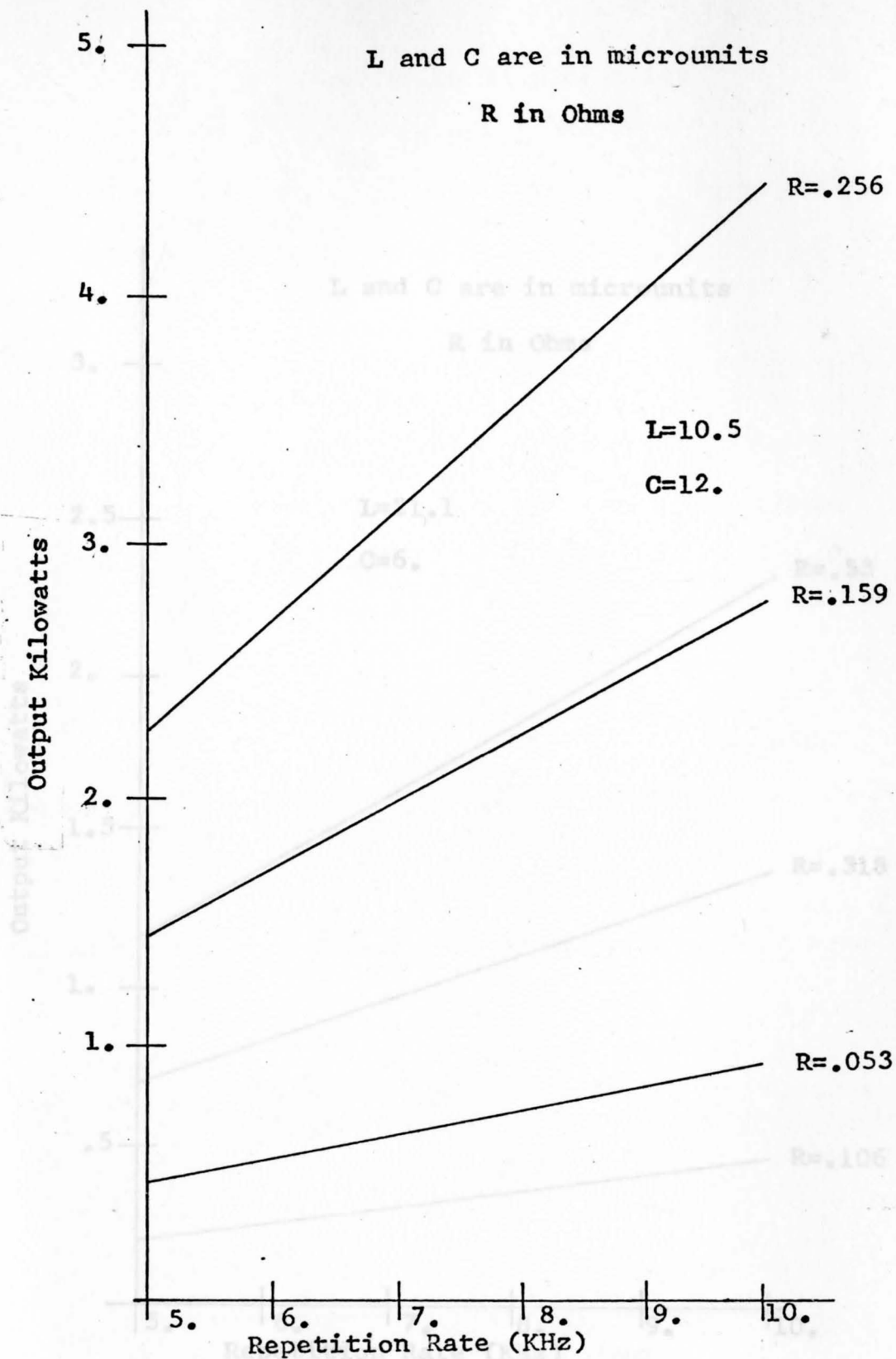


Fig. 5-17. Kilowatt Output Versus Repetition Rate

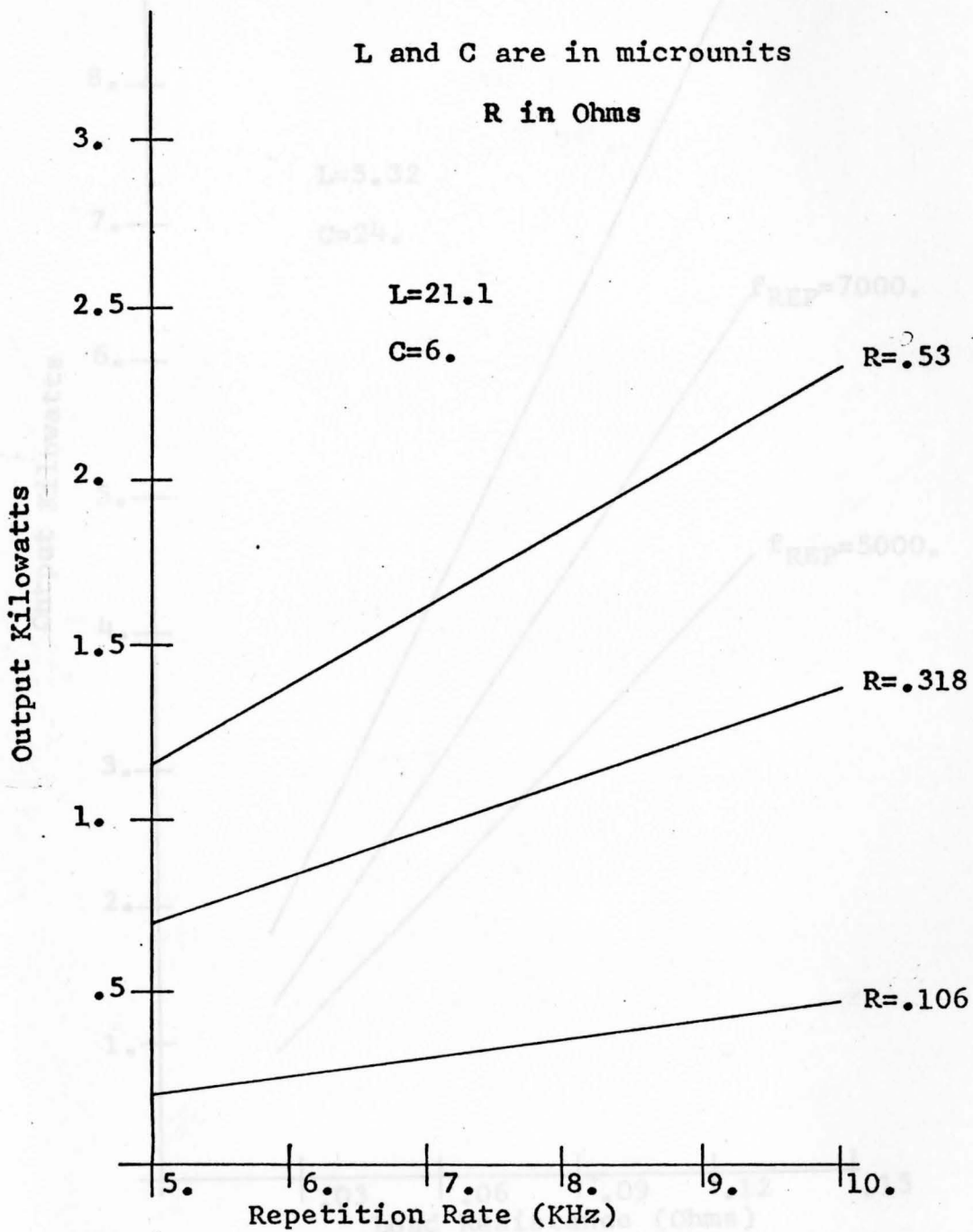


Fig. 5-18. Kilowatt Output Versus Repetition Rate.

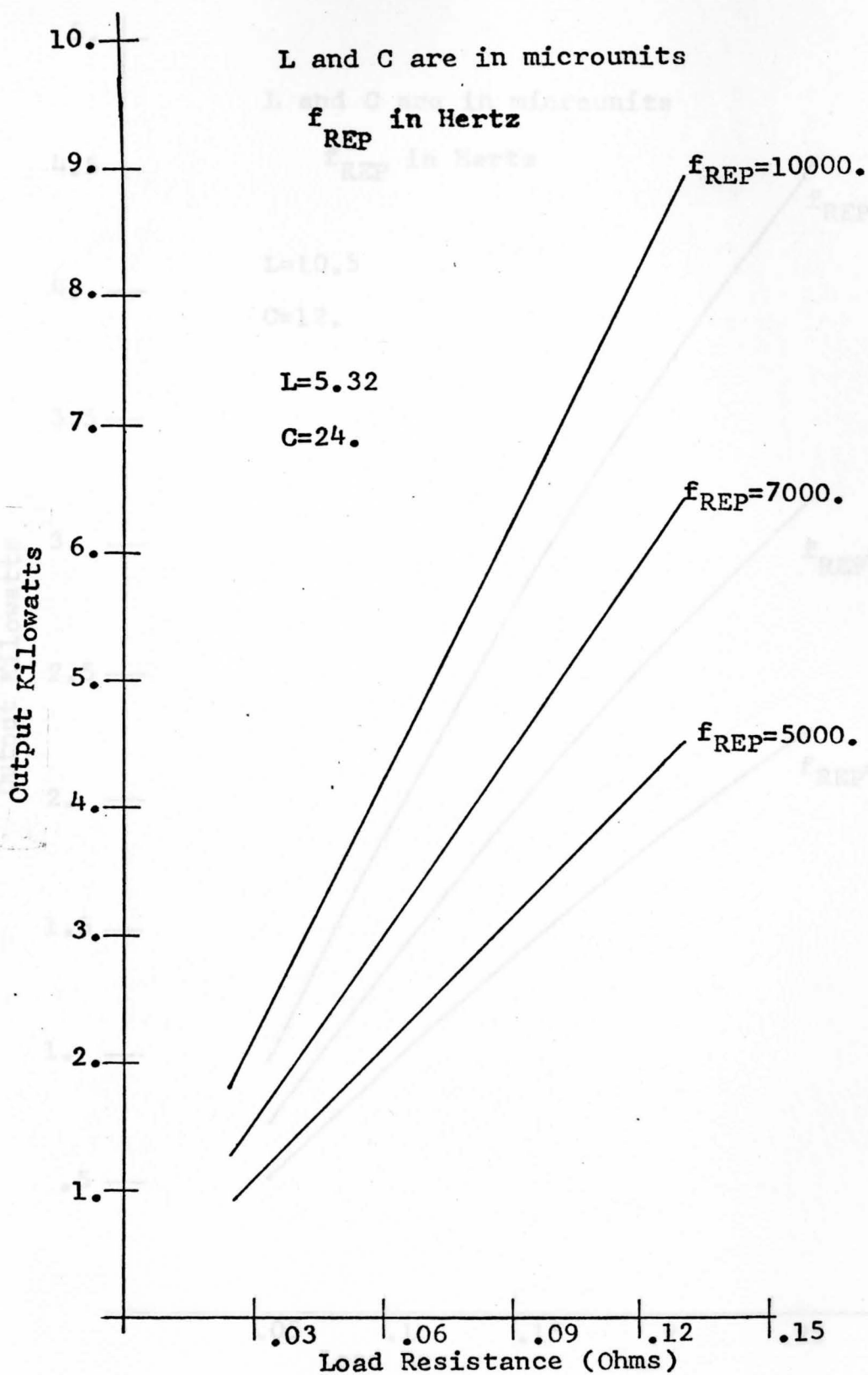


Fig. 5-19. Output Kilowatts Versus Load Resistance.

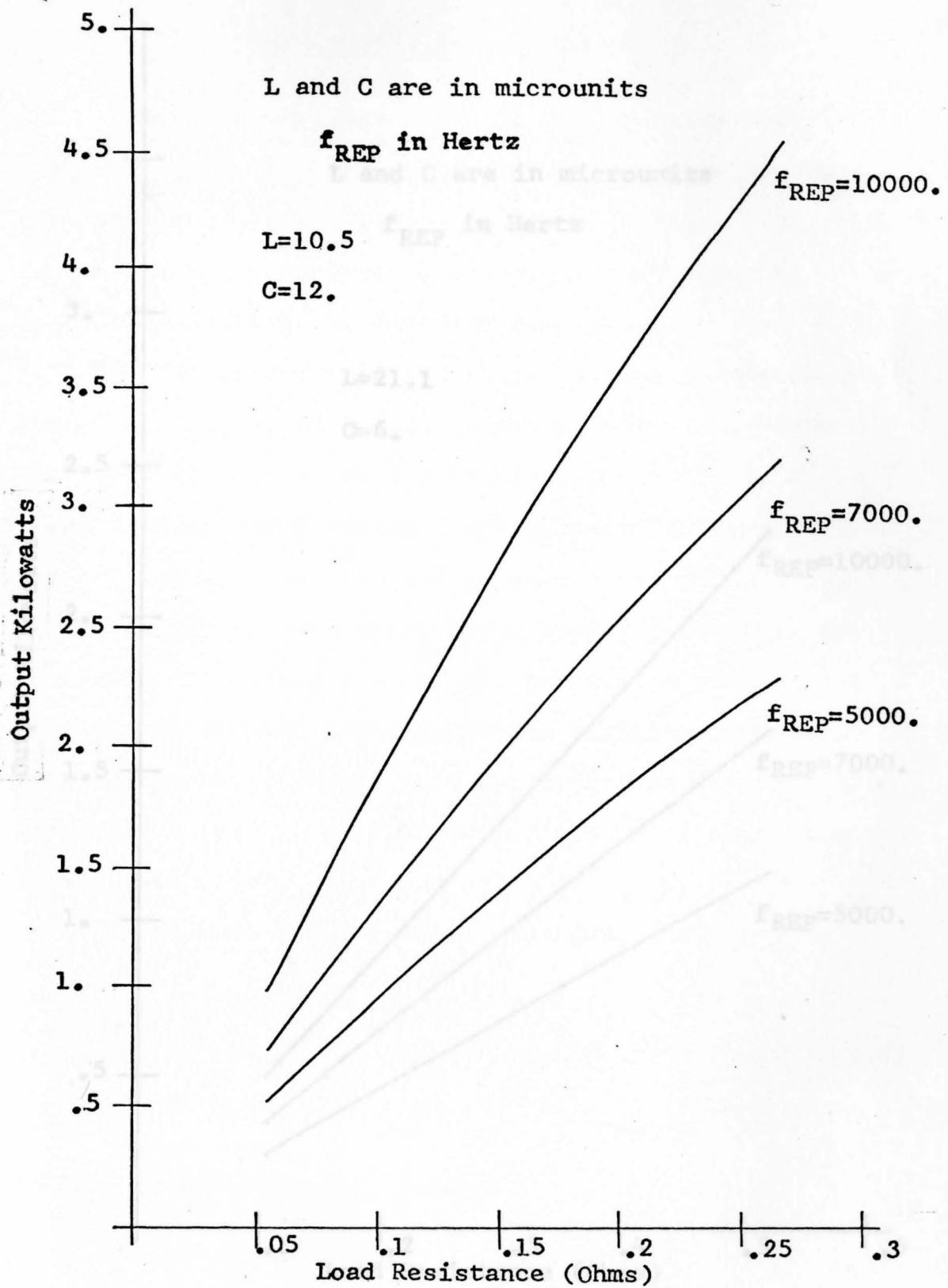


Fig. 5-20. Output Kilowatts Versus Load Resistance.

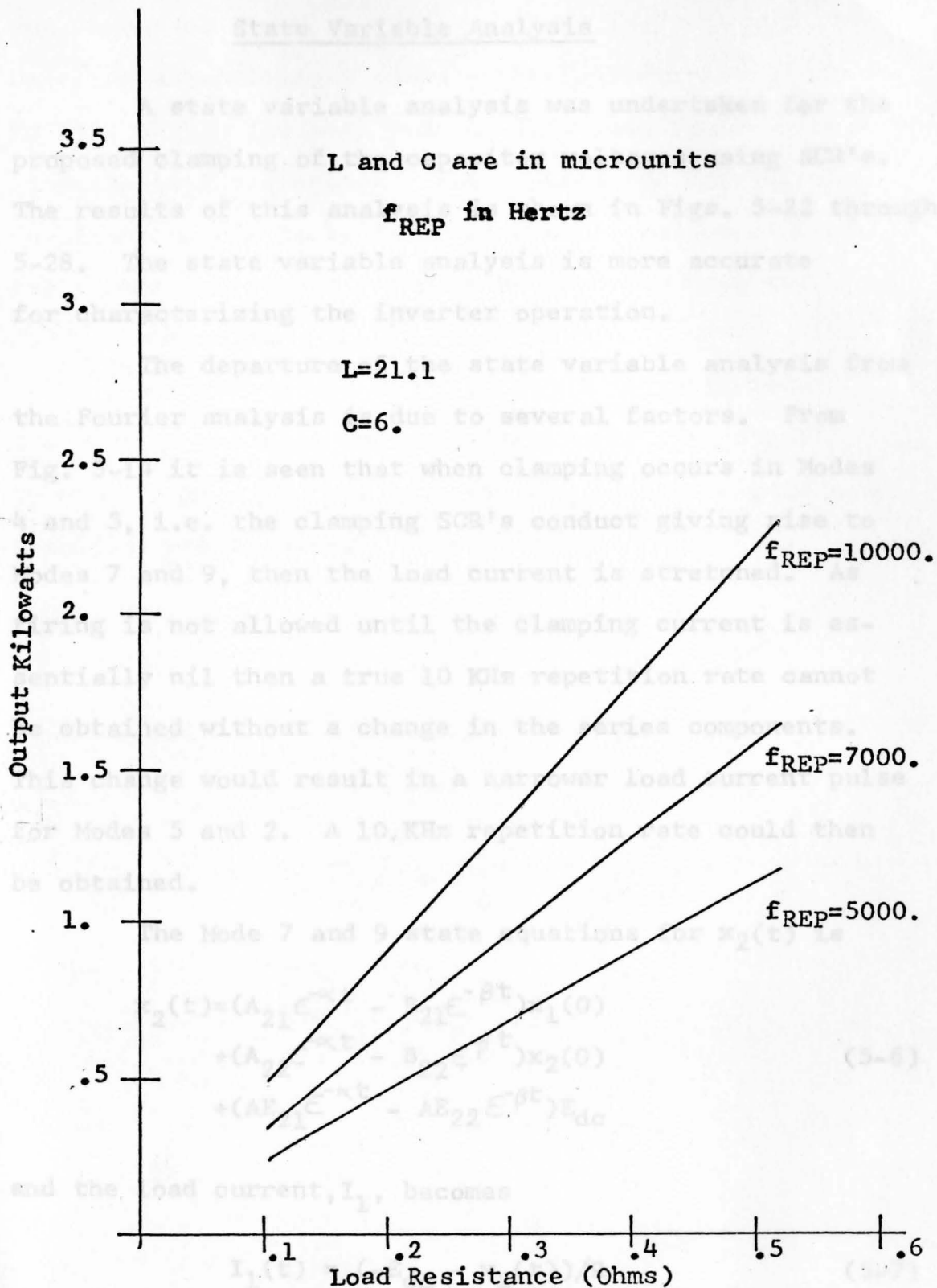


Fig. 5-21. Output Kilowatts Versus Load Resistance.

State Variable Analysis

A state variable analysis was undertaken for the proposed clamping of the capacitor voltages using SCR's. The results of this analysis is shown in Figs. 5-22 through 5-28. The state variable analysis is more accurate for characterizing the inverter operation.

The departure of the state variable analysis from the Fourier analysis is due to several factors. From Fig. 5-14 it is seen that when clamping occurs in Modes 4 and 3, i.e. the clamping SCR's conduct giving rise to Modes 7 and 9, then the load current is stretched. As firing is not allowed until the clamping current is essentially nil then a true 10 KHz repetition rate cannot be obtained without a change in the series components. This change would result in a narrower load current pulse for Modes 5 and 2. A 10, KHz repetition rate could then be obtained.

The Mode 7 and 9 state equations for $x_2(t)$ is

$$\begin{aligned} x_2(t) = & (A_{21}e^{-\alpha t} - B_{21}e^{-\beta t})x_1(0) \\ & + (A_{22}e^{-\alpha t} - B_{22}e^{-\beta t})x_2(0) \\ & + (AE_{21}e^{-\alpha t} - AE_{22}e^{-\beta t})E_{dc} \end{aligned} \quad (5-6)$$

and the load current, I_1 , becomes

$$I_1(t) = (-E_{dc} - x_2(t))/R \quad (5-7)$$

The nature of equation (5-6) and thus (5-7) is such as to cause an additional peak on the load current as shown in Fig. 5-14. The amplitude of this peak varies inversely with the load resistance. This causes the RMS value of the load current to be larger for small values of load resistance than would normally be expected from the Fourier analysis.

For the values of L, C, and R investigated, the Fourier analysis successfully showed the output trends inherent in this inverter but failed to give more specific, useful data.

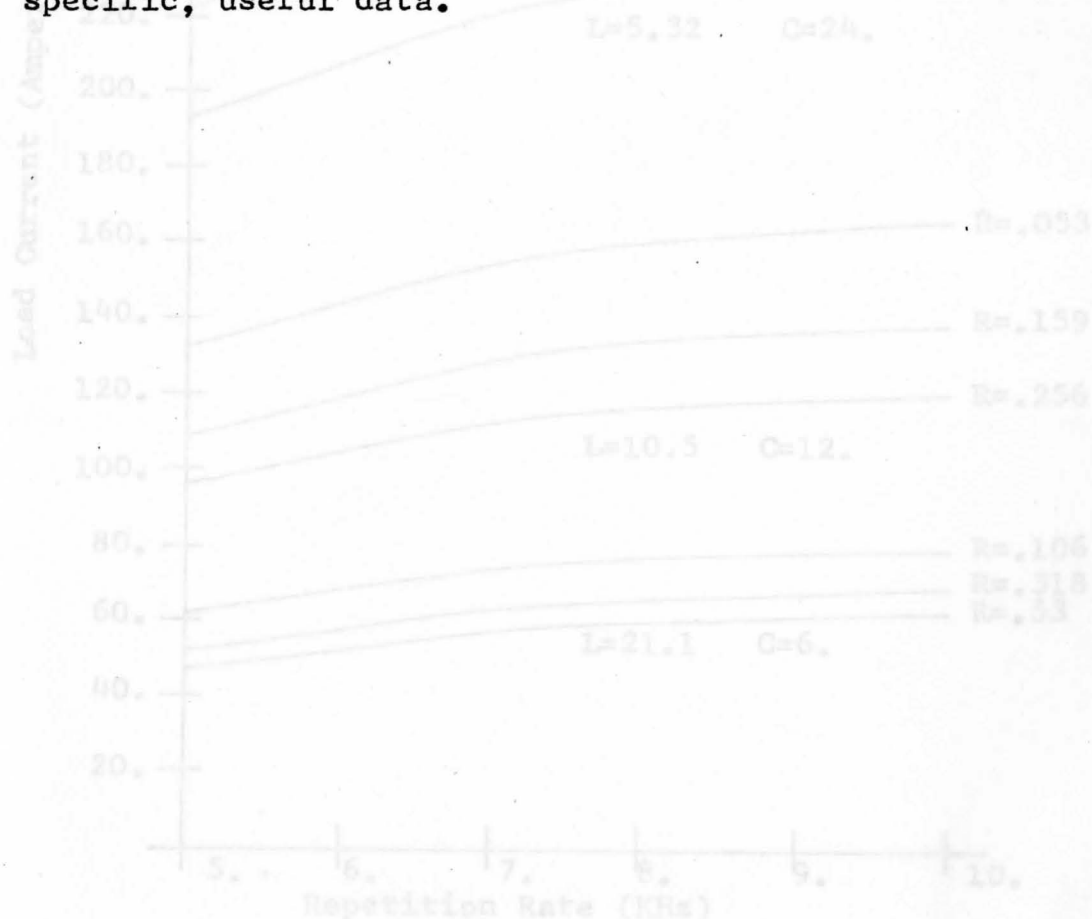


Fig. 5-22. RMS Load Current Versus Repetition Rate.

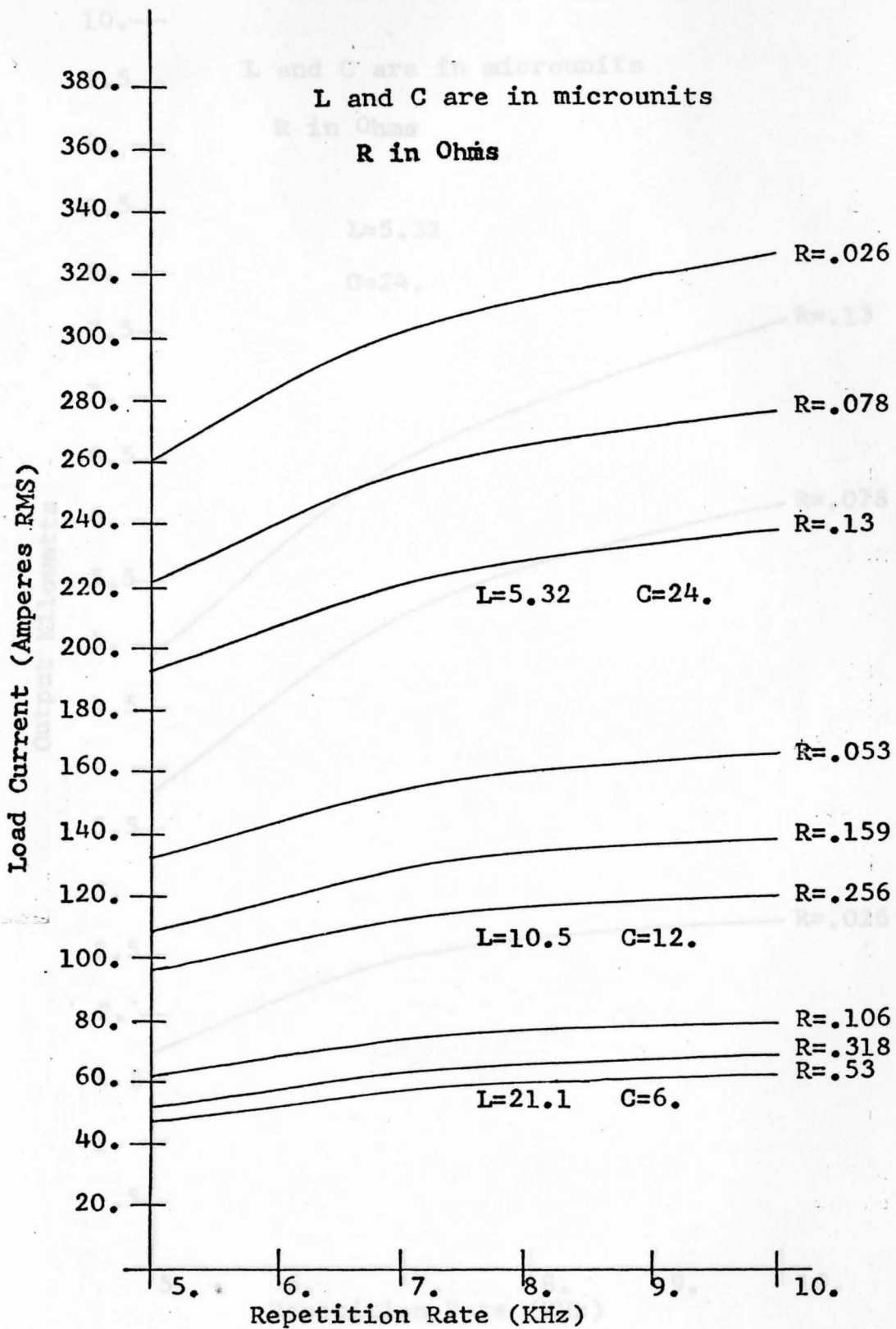


Fig. 5-22. RMS Load Current Versus Repetition Rate.

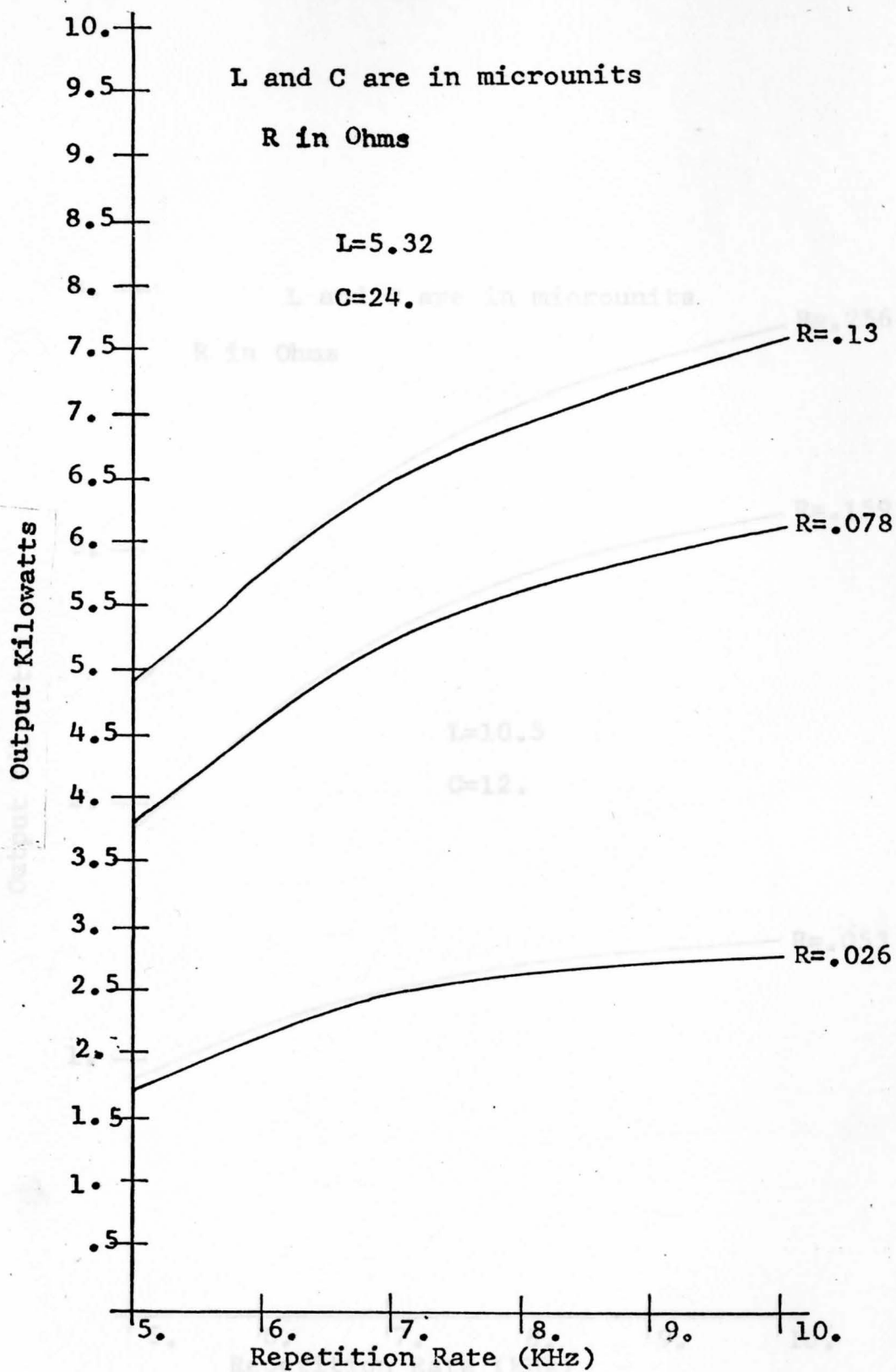


Fig. 5-23. Output Kilowatts Versus Repetition Rate.

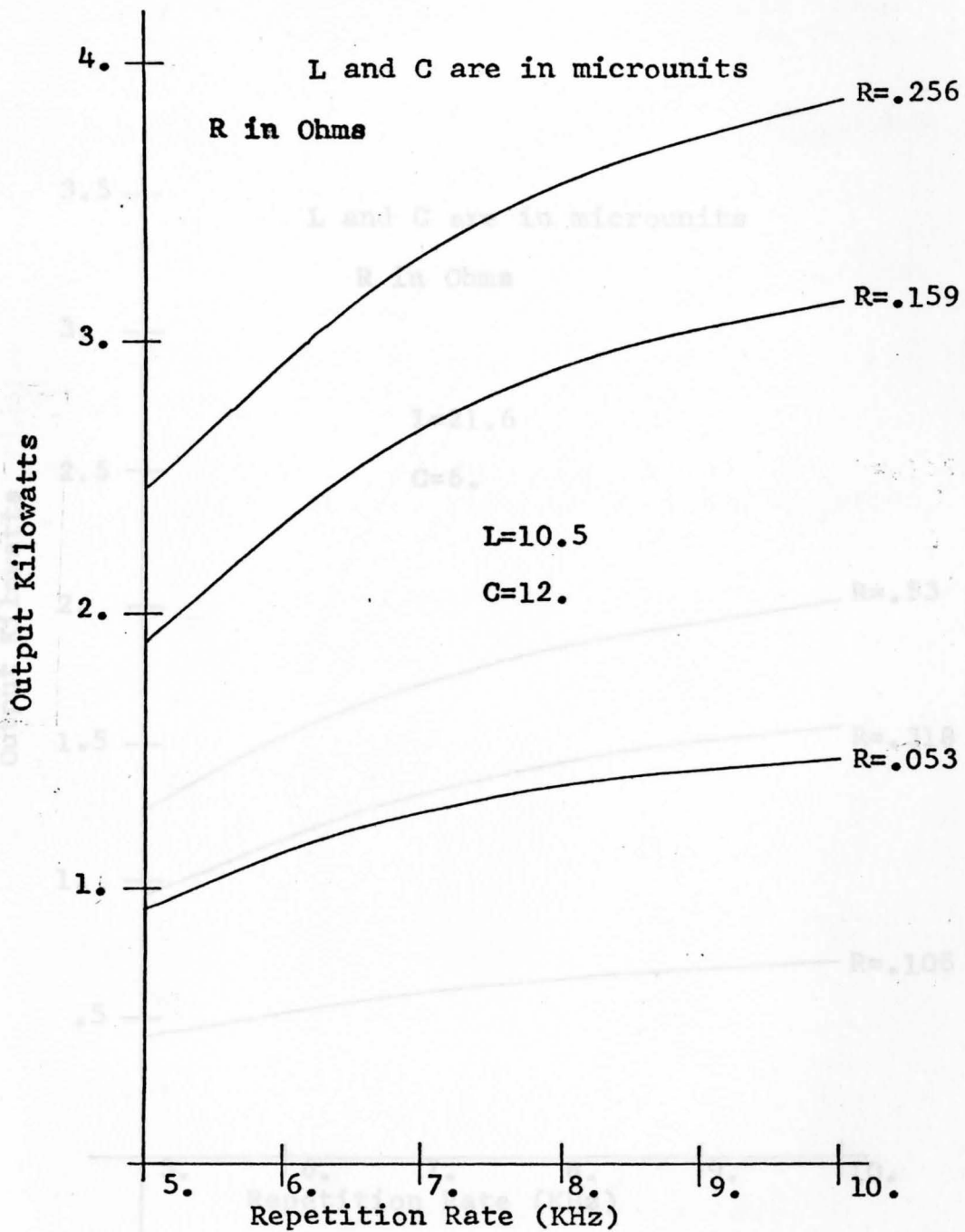


Fig. 5-24. Output Kilowatts Versus Repetition Rate.

Fig. 5-25. Output Kilowatts Versus Repetition Rate.

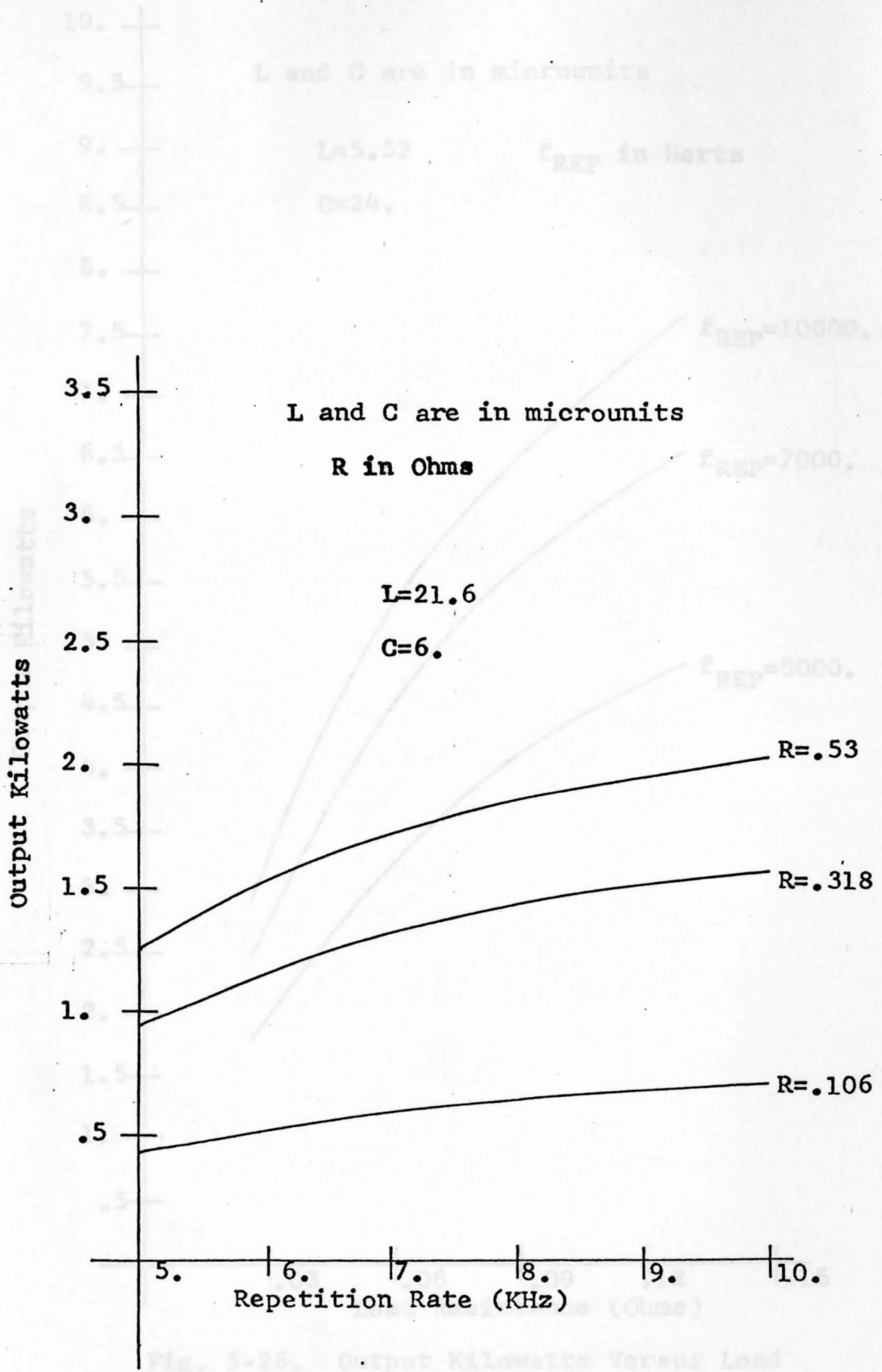


Fig. 5-25. Output Kilowatts Versus Repetition Rate.

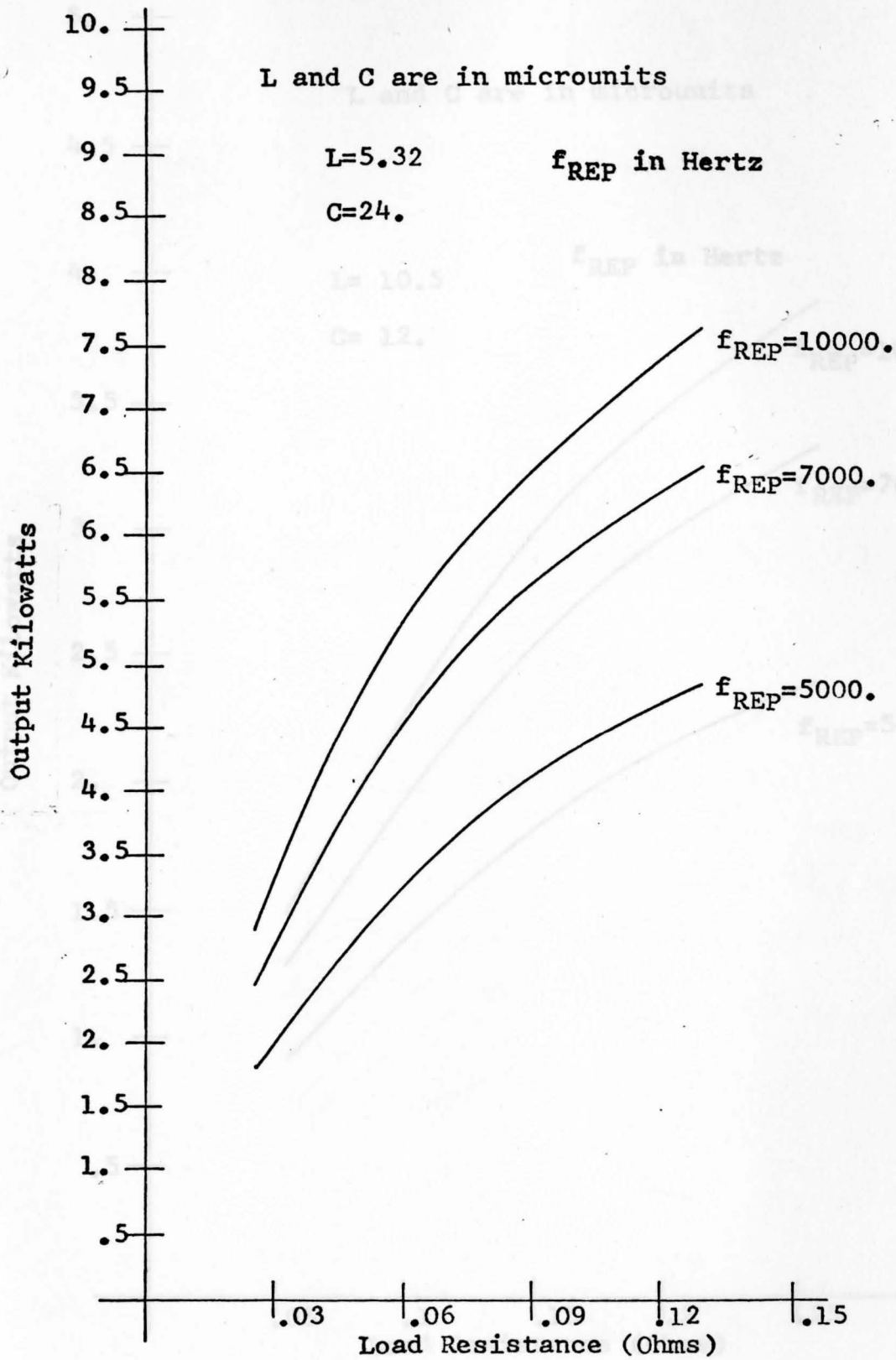


Fig. 5-26. Output Kilowatts Versus Load Resistance.

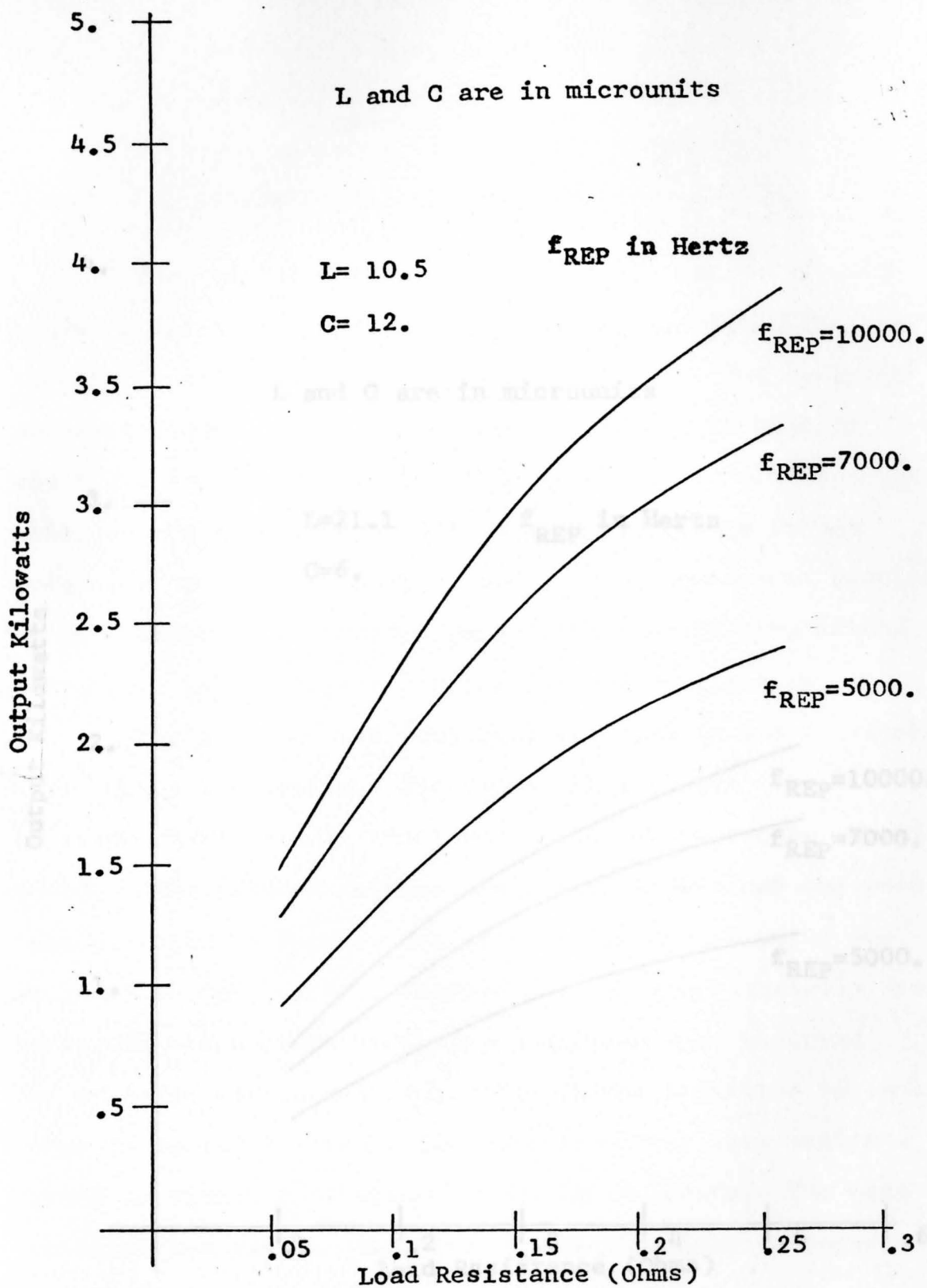


Fig. 5-27. Output Kilowatts Versus Load Resistance.

CHAPTER VI

RESULTS AND CONCLUSIONS

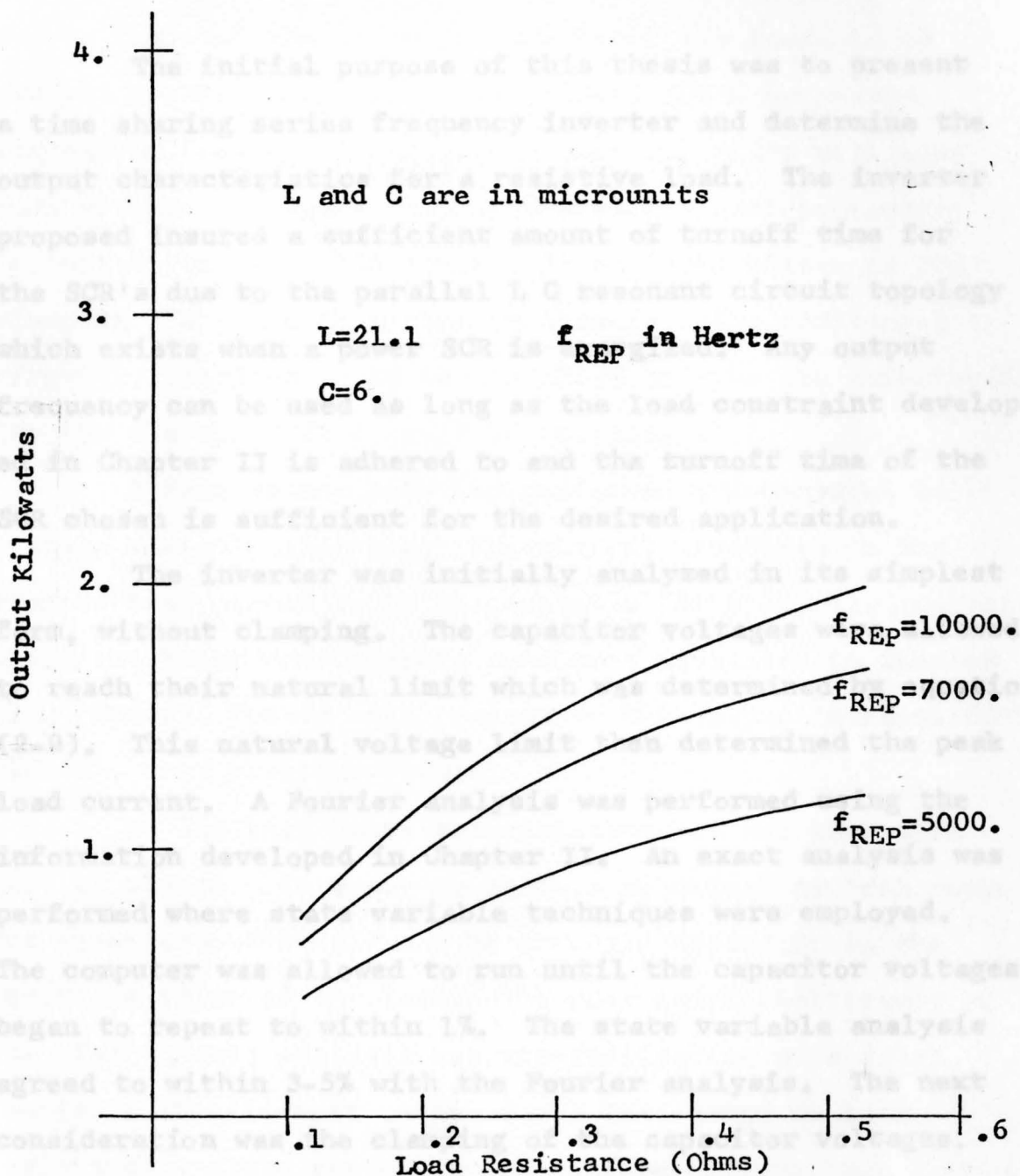


Fig. 5-28. Output Kilowatts Versus Load Resistance.

CHAPTER VI

RESULTS AND CONCLUSIONS

The initial purpose of this thesis was to present a time sharing series frequency inverter and determine the output characteristics for a resistive load. The inverter proposed insured a sufficient amount of turnoff time for the SCR's due to the parallel LC resonant circuit topology which exists when a power SCR is energized. Any output frequency can be used as long as the load constraint developed in Chapter II is adhered to and the turnoff time of the SCR chosen is sufficient for the desired application.

The inverter was initially analyzed in its simplest form, without clamping. The capacitor voltages were allowed to reach their natural limit which was determined by equation (2-9). This natural voltage limit then determined the peak load current. A Fourier analysis was performed using the information developed in Chapter II. An exact analysis was performed where state variable techniques were employed. The computer was allowed to run until the capacitor voltages began to repeat to within 1%. The state variable analysis agreed to within 3-5% with the Fourier analysis. The next consideration was the clamping of the capacitor voltages.

The reason for the clamping is to prevent the catastrophic failure of the series capacitor or SCR due

to small changes in the load resistance. The clamping allows for a more flexible inverter with respect to the load.

It has been noted in this thesis that diode clamping was not sufficient for successful operation of this inverter due to the fact that a DC voltage level was found to be present on the load. For this reason, SCR's were used instead of diodes. Although the clamping SCR's will have some reverse voltage across them when the next sequential firing of the power SCR occurs, it would be better if the clamping SCR's are in a chopper circuit. The additional circuitry required would be justified because the commutation for the clamping SCR's would be certain.

A Fourier analysis was performed and compared to a state variable analysis. The current waveforms in the clamped case proved to be unacceptable for a Fourier analysis where the Euler coefficients used were developed in Chapter III. General trends with respect to the output characteristics were the only positive result.

As any load heats the resistance of the load will tend to change. In order to allow a practical control range the power output should not be strongly dependent on the resistive value of the load. The most beneficial result of the clamped case analysis was the realization of a 2.7:1 change in the kilowatt output for a 5:1 change in load resistance and the prevention of catastrophic voltage failure due to load changes. In the unclamped case the power output varied directly with the load resistance.

A DC voltage of 100 volts was chosen as the one per unit supply voltage. The output power can be determined for other voltages by noting that the power output will vary by the square of the supply voltage.

Future work on this system would include the study of this inverter with inductive, capacitive and resonant loads. Experimental determinations could also be included for the further study and development of this inverter.

Any SCR is designed ultimately for repetitive off-state blocking voltage, maximum average current, and speed or minimum turnoff time. The design involves tradeoffs of these parameters.

The n-base thickness, for all practical purposes, determines the rated repetitive off-state blocking voltage. The approximate relationship for the n-base thickness is given as

$$W_n = 150 \cdot V_{RM}^{3/2} \quad (A-1)$$

where

W_n is the n-base thickness (μ m)

and

V_{RM} is the rated repetitive blocking voltage.

The on-state voltage expression developed is

$$V_T = 0.8 + .15 V_{Tmax} (V_{RM} / V_{E0})^{3/2} \quad (A-2)$$

APPENDIX A

SCR Tradeoffs

An SCR is a four layer p-n-p-n device. The outer p and n regions are, respectively, the anode and cathode; the inner regions are the p-base and n-base, or gate. Any SCR is designed ultimately for repetitive off-state blocking voltage, maximum average current, and speed or minimum turnoff time. The design involves tradeoffs of these parameters.

The n-base thickness, for all practical purposes, determines the rated repetitive off-state blocking voltage. The approximate relationship for the n-base thickness is given as

$$W_n = 150 \cdot V_{RM}^{3/2} \quad (A-1)$$

where

W_n is the n-base thickness (μ m)

and

V_{RM} is the rated repetitive blocking voltage.

The on-state voltage expression developed is

$$V_T = 0.8 + .15 \sqrt{J_T} \exp(4(V_{RM}/\sqrt{t_q})^{3/2}) \quad (A-2)$$

where

V_T is the on-state voltage

J_T is the on-state current density (A/mm^2)

and

t_q is the turnoff time (μ sec).

The J_T , V_T product defines the power dissipation density, P_T . The average power dissipation density, P_{TAVE} , depends on P_T , cathode area, total silicon area, and the duty cycle. P_{TAVE} should be kept less than 2 watts/ mm^2 so that the junction will not be thermally over stressed.

Equation A-2 clearly shows that, for a constant V_{RM} and J_T , as t_q grows smaller V_T increases thus P_{TAVE} increases. Clearly a large load-power controlling ability tends to require a large turnoff time.

Fig. A-1 is a plot of the V_{RM} , J_T product for several turnoff times. These points are plotted at the power dissipation density equal to the maximum, 2 watts/ mm^2 . The plot shows that if a high load-power controlling capability is necessary at a high repetition rate, which normally requires a short turnoff time, a time sharing scheme is necessary. [8]

Fig. A-1. Blocking Voltage Versus the Blocking Voltage Current Density Product.

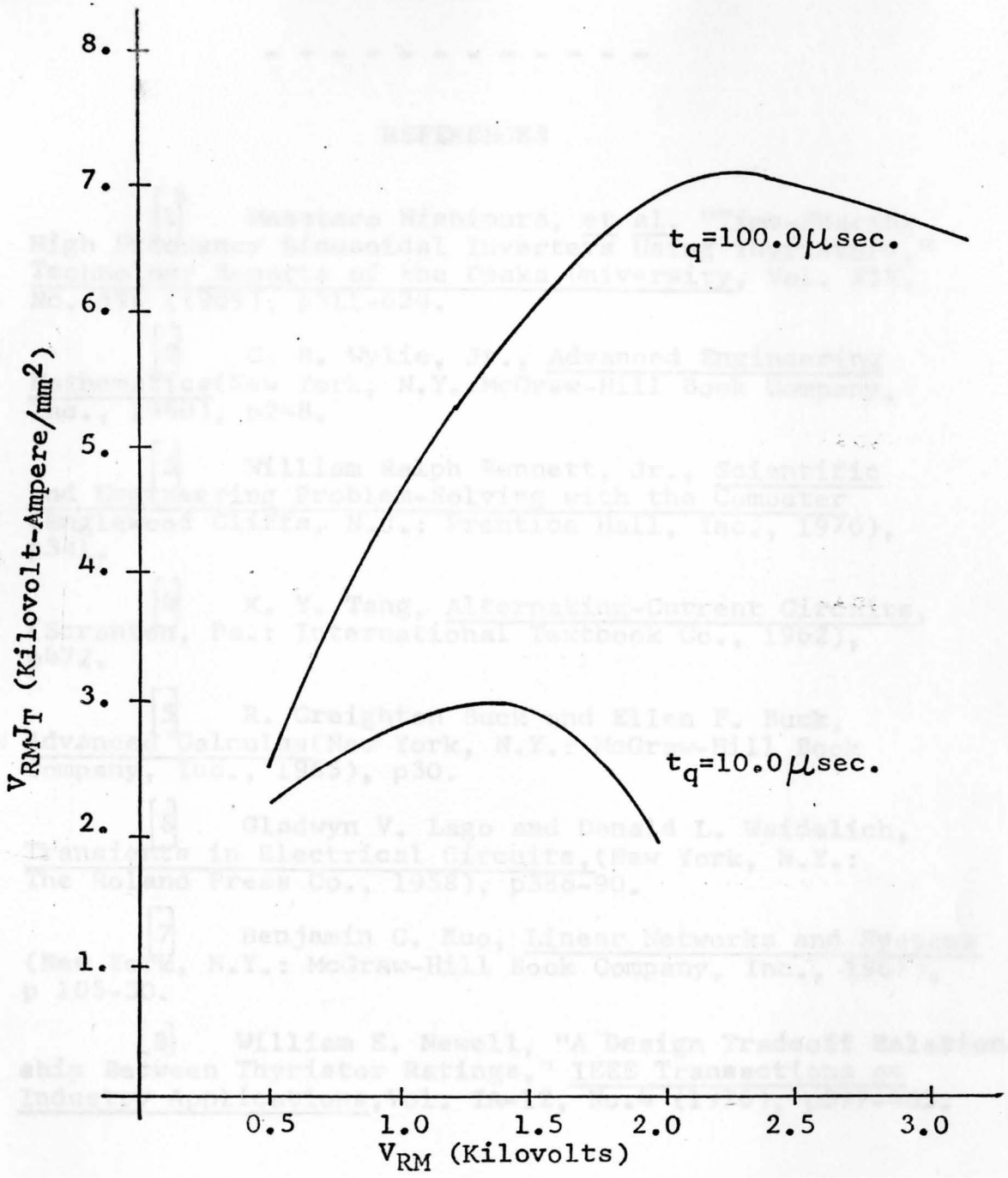


Fig. A-1. Blocking Voltage Versus the Blocking Voltage Current Density Product.

REFERENCES

- [1] Masataro Nishimura, et al, "Time-Sharing High Frequency Sinusoidal Inverters Using Thyristors," Technology Reports of the Osaka University, Vol. XIX, No. 896 (1969), p511-624.
- [2] C. R. Wylie, Jr., Advanced Engineering Mathematics(New York, N.Y.:McGraw-Hill Book Company, Inc., 1960), p248.
- [3] William Ralph Bennett, Jr., Scientific and Engineering Problem-Solving with the Computer (Englewood Cliffs, N.J.: Prentice Hall, Inc., 1976), p341.
- [4] K. Y. Tang, Alternating-Current Circuits, (Scranton, Pa.: International Textbook Co., 1962), p472.
- [5] R. Creighton Buck and Ellen F. Buck, Advanced Calculus(New York, N.Y.: McGraw-Hill Book Company, Inc., 1965), p30.
- [6] Gladwyn V. Lago and Donald L. Waidelich, Transients in Electrical Circuits,(New York, N.Y.: The Roland Press Co., 1958), p386-90.
- [7] Benjamin C. Kuo, Linear Networks and Systems (New York, N.Y.: McGraw-Hill Book Company, Inc., 1967), p 105-30.
- [8] William E. Newell, "A Design Tradeoff Relationship Between Thyristor Ratings," IEEE Transactions on Industry Applications, Vol. IA-12, No.4 (1976), p397-405.

