WIRELESS ASYNCHRONOUS COMMUNICATION VIA INFRARED TRANSMISSION AND RECEPTION

by

KURT ALAN HEDDLESTON

Submitted in Partial Fulfillment of the Requirement

for the Degree of

Master of Science

in the

Electrical Engineering

Program

Salvatore R. Pansino 3/9/90

Advisor Date

Sally M. Hotchkiss March 20, 1990

Dean of the Graduate School Date

YOUNGSTOWN STATE UNIVERSITY

MARCH, 1990

ABSTRACT

WIRELESS ASYNCHRONOUS COMMUNICATION
VIA INFRARED TRANSMISSION AND RECEPTION

Kurt A. Heddleston
Master of Science in Engineering
Youngstown State University, 1990

Asynchronous communication is discussed and various information protocol packets are investigated. Special attention is given to the PC's UART chip and RS-232 communication standard.

Circuits for wireless asynchronous communication, via an infrared transmitter and receiver between computers, were designed, built, and tested. The use of infrared as a medium in modern day wireless communications is discussed.

The infrared transmitter and receiver circuits were built using commercial off-the-shelf equipment. A simple but effective program written in the BASIC programming language was used for initial tests. A commercially available software package, KERMIT, was used for more intensive testing.

ACKNOWLEDGEMENTS

I would like to expresss my sincere gratitude to my advisor, Professor Salvatore Pansino, for the excellent job he has done as my advisor, and to Professors R.H. Foulkes and M. Siman for agreeing to be on my thesis committee.

I would also like to express my appreciation to my engineering collegues at the Naval Weapons Support Center for their technical expertise and assistance.

My deepest respect goes to my parents, who encouraged and supported me to seek an advanced degree.

TABLE OF CONTENTS

LIST OF SYMBOLS

SYMBOL	DEFINITION
ACE	Asynchronous Communications Element
ASCII	American Standard Code for Information and Interchange
bps	bits per second
CRT	Cathode Ray Tube
DC3	Device Control character #3
FTP	File Transfer Protocol
SOH	Start Of Header character
ARQ	Automatic Repeat Request
ACK	Acknowledge
NAK	Negative Acknowledge
BS	Back Space character
HT	Horizontal Tab character
LF	Line Feed character
VT	Vertical Tab character
FF	Form Feed character
CR	Carriage Return character
STX	Start of Text character
ETX	End of Text character
RTTY	Radio Teletype
ASK	Amplitude Shift Keying
FSK	Frequency Shift Keying

PSK	Phase Shift Keying
QPSK	Quadrature Phase Shift Keying
EIA RS-232C	Electronic Industries Association Recommended Standard Number 232, Revision C
DTE	Data Terminal Equipment
DCE	Data Communications equipment
PC	Personal Computer
UART	Universal Asynchronous Receiver/Transmitter
SDU	Serial Data Unit
TBE	Transmitter Buffer Empty flag
TXE	Transmitter Empty flag
FIFO	First In First Out
TTL	Transistor Transistor Logic
I/O	Input or Output
MHz	10^6 Hertz (megahertz)
KHz	10^3 Hertz (kilohertz)

LIST OF FIGURES

LIST OF TABLES

CHAPTER 1

INTRODUCTION

1.1 Introduction

The idea for this study developed from discussions by members of a concept design team about their mission of building a man-portable, ruggedized, networked computer system for the military; what is the most effective means of communicating between computers? There are several factors involved in choosing a transmission medium including development and production cost of any new equipment compared with existing equipment, but there are two factors very important to the military that are particularly important in making this decision: (1) the equipment or devices chosen must be lightweight, and (2) the data being transmitted must not be detectable by enemy equipment.

1.2 Lightweight

The distance between portable computers in the field is continually changing, making it difficult to determine the length of networking cable needed. Carrying enough cable for all situations would place an unacceptable weight burden on an individual; the military is continually investigating ways to lighten the carrying load of a soldier. In addition, battlefield

conditions may be such that it would be impossible to string a cable from one PC to another PC located at a different site. This suggests some sort of wireless communication, possibly radio.

1.3 Detectability

Another concern is the ability to intercept the data being transmitted between the computers. If radio is chosen as the transmission medium, then the concern is that there are many electronic devices that can intercept radio signals. The military currently uses special equipment which encrypts radio transmission to ensure that any intercepted data cannot be understood. These devices are large and heavy, effectively eliminating the use of radio in a highly portable environment. Ultimately, infrared was chosen to be evaluated. By using infrared, all concerns could be met including unwanted signal detection. Infrared can only be detected in the line of sight. My task was to build, test, and determine the feasibility of using infrared as the transmission medium.

CHAPTER 2

DEVELOPMENT

2.1 Cost

Once infrared was chosen as the transmission medium to evaluate, the next concern was the time and cost of building and testing an infrared transmitter and receiver for evaluation. Most of the development money is being spent on development of the lightweight, portable, ruggedized computer that is going to be used in the field. The rest of the money is being spent on software packages being developed to run on the new hardware. This leaves very little funding for developing an infrared transmitter and receiver.

To keep development cost to a minimum, it was decided that only a single engineer would be assigned to this project for a period of two months. At the end of the two-month period, an engineering review board would determine whether additional funding would be required for further development based upon the results of this project. Additionally, no special testing equipment would be purchased for this project. All parts and devices were to be chosen from available stock whenever possible and commercially available when not.

2.2 Approach

Due to the time and cost constraints, building an infrared transmitter and receiver on a printed circuit board would be out of the question. The logical choice was to build these circuits on a breadboard. Likewise, time and money do not lend themself to building multiple transmitters and receivers for testing purposes. Therefore, it was decided that only one infrared transmitter and receiver would be built. Initially each would be on the same breadboard for testing purposes. The advantages include: (1) a single power supply can be used to power each of the circuits, and (2) a single PC can be used for transmitting and receiving data.

A source of information dealing with infrared transmission and reception was needed. Ideal sources are television and VCR manufacturers; virtually all televisions and VCR's today have an infrared remote control. Although manufacturers are reluctant to give out proprietary information, it was discovered that most of the remote controls use standard infrared LEDs which are readily available from companies that produce optoelectronic devices. The remote control receivers use either a PIN photo diode or a phototransistor as the device to detect infrared signals.

All PCs have an asynchronous RS-232 serial port designed for external communications with peripherals and other PCs. This is the obvious choice and will be used as the interface between the

infrared circuits and the PC. Information concerning asynchronous serial data transmission is reviewed in Appendix A. Background material discussing information transfer and various associated protocols is provided in Appendix B. Finally, a thorough knowledge of RS-232 and the internal workings of the UART chip is essential for understanding exactly how a computer communicates through this port. This information is discussed in Appendices C and D.

CHAPTER 3

HARDWARE DESIGN AND ANALYSIS

3.1 Introduction

The infrared transmitter was the first circuit to be built. The basic design is similar to that of a television remote control infrared transmitter. However, whereas remote control transmitters usually have a chip which generates specific data codes for each key pressed, this transmitter does not. It simply transmits any data sent from the RS-232 port of the computer.

3.2 Infrared Transmitter

Figure 1 shows the schematic of the transmitter. The transmitter functions like a switch, passing current through the infrared emitting diodes only when it's turned on. The resistor values were chosen to keep the collector and base currents within the given specifications of both the transistor and infrared emitting diodes. The two diodes connected between the base of the transistor and ground insure proper biasing of the transistor base.[1]

---

[1]Motorola CMOS/NMOS Special Functions Data Manual 1988, pp 7-10

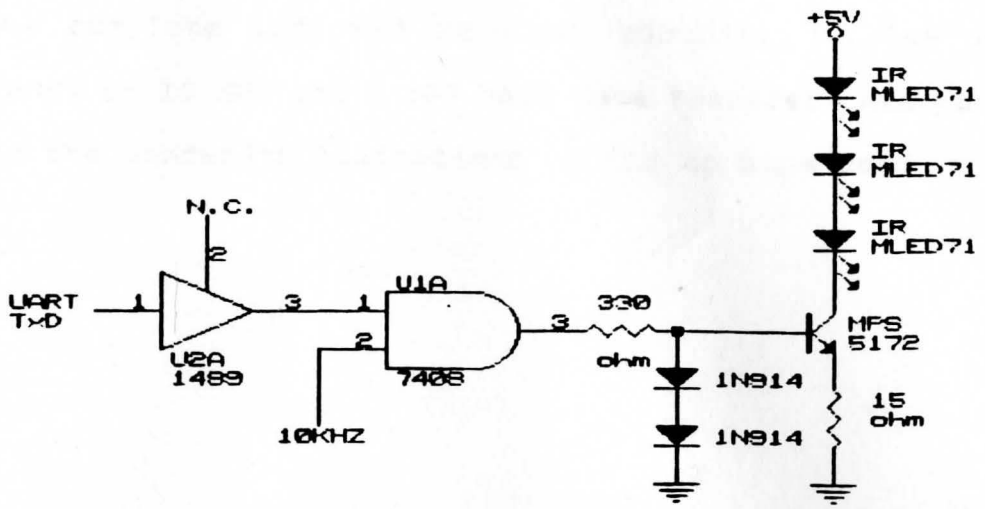


FIGURE 1. Infrared Transmitter Schematic

Data originates from the RS-232 Transmit Data (TxD) pin of the PCs communications port which is connected to the UART. The signal must be converted from RS-232 voltage levels to Transistor Transistor Logic (TTL) levels, via the 1489 line receiver chip. The transmitter infrared modulation control is accomplished by ANDing the modulation clock with the data signal. A MARK is modulated with a 10 KHz signal and a SPACE is unmodulated.

3.3 Infrared Receiver

The infrared receiver circuit detects an infrared modulated signal, filters out all unwanted signals and transmission noise, amplifies the desired signal, demodulates the signal, and converts the signal to RS-232 levels. Figure 2 shows the schematic

of the complete infrared receiver circuit; a low modulation frequency of 10 KHz and a 300 baud data transfer rate was selected due to the bandwidth limitations of the op amps used.

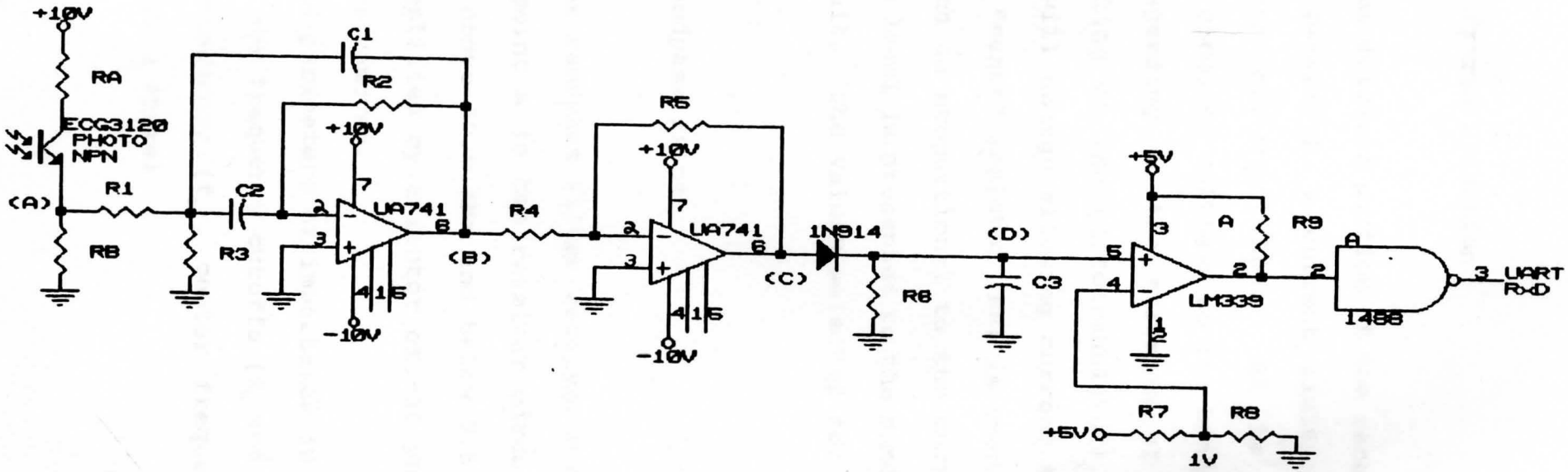


FIGURE 2. Infrared Receiver Schematic

3.3.1 Infrared Detection

The detector portion of the receiver circuit is composed of a phototransistor, a current limiting resistor (RA), and a current sense resistor (RB). RA is chosen to provide the appropriate range of voltages to the bandpass filter.

Depending on the strength of the signal (number of photons falling on the phototransistor), the resistance of the transistor will change allowing current to pass proportionately. The current "sense" resistor (RB) is used to provide a voltage at point A which is proportional to the current passing through it. This voltage level is presented to the bandpass filter located next in the circuit. The values selected for RA and RB are listed in Table 1.

3.3.2 Bandpass Filter

The bandpass filter receives a small modulated positive voltage at point A in the receiver circuit, and filters out all frequencies above 10.5 KHz and below 9.5 KHz. In addition, the signal is amplified by a factor of -10 while the DC component of the signal is removed.

The parameters of importance in the bandpass filter are the high and low frequency cutoffs (f_h and f_l), the bandwidth (Δf), the center frequency (f_c), center frequency gain (A_0), and the selectivity or Q where:

$$\Delta f = f_h - f_l$$

$$f_c = \sqrt{f_h * f_l}$$

$$Q = f_c/\Delta f$$

In the design of the single op amp bandpass filter, a few general rules were followed[2]:

$$1 < Q < 10 \text{ to } 20$$

$$f_c > 1/2\pi\sqrt{R1R2}\ C \qquad \text{where } C=C1=C2$$

$$2Q^2 > A_0$$

Equations used in solving for C, R1, R2, and R3 are:

$$R1 = -R2/2A_0$$

$$R2 = 2/2\pi\Delta fC$$

$$R3 = R1/4\pi^2 R1R2f_c^2C^2-1$$

A capacitance value of 2200 pF was chosen for both C1 and C2. In addition, a closed loop gain of -10, and a low and high frequency cutoff of 9.5 KHz and 10.5 KHz respectively were selected. Substituting into the equations above, and carefully observing the rules discussed above, results in the resistor values for R1, R2, and R3 listed in Table 1.

---

[2]J.Michael Jacob, Applications and Design with Analog Integrated Circuits, Reston, 1982, p.363-373

TABLE 1. Receiver Circuit Component Values

Component	Value
RA	1K ohm
RB	1K ohm
R1	3.6K ohm
R2	72.3K ohm
R3	907 ohm
R4	10K ohm
R5	100K ohm
R6	1.56K ohm
R7	10K ohm
R8	2.5K ohm
R9	10K ohm
C1	2200 pF
C2	2200 pF
C3	1 μF

3.3.3 Inverting Amplifier

Once the signal has been detected with all transmission noise and unwanted signals filtered out, it must be further amplified. The filtered signal enters the inverting amplifier stage of the receiver circuit at point B. The amount of amplification depends on the desired distance from the transmitter to the receiver, and the gain bandwidth product (GBW) of the receiver amplifying devices (741 op amps).

The high frequency cutoff (f_h) and the closed loop gain (A_0) define the GBW:

$$GBW = f_h A_0$$

Substituting for GBW (1 MHz for the 741) and using 10 KHz as the high cutoff frequency, a total closed loop gain of 100 can be achieved. However, the bandpass filter gain is -10, limiting the

inverting op amp gain to an additional factor of -10. Together, the two result in a total signal gain of 100. So, choosing a gain of -10, selecting a convenient value for R4, and substituting into the inverting op amp gain equation

$$A_0 = -R5/R4$$

yields the values of R4 and R5, shown in Table 1.

3.3.4 Half-Wave Capacitor Filtered Rectifier

The half-wave capacitor filtered rectifier beginning at point C in the receiver circuit is used to form the desired bit pattern by demodulating the modulated signal. During the time interval when the diode is conducting, the voltage at point C is impressed directly across the load resistor (R6), assuming the diode drop can be neglected. During the interval when the diode is nonconducting, the capacitor discharges with a time constant of C3R6. The output waveform consists of portions of sinusoids (when diode is on) joined to exponential segments (when diode is off)[3]. The result, at point D, is a positive DC voltage with a small ripple at its peek. The time constant for charging and discharging the capacitor limits the speed at which the bits can be formed, and hence transmitted. Values used for R6 and C3 are listed in Table 1.

---

[3]Jacob Millman, MICROELECTRONICS: Digital and Analog Circuits and Systems, McGraw-Hill, 1979, pp 350-351.

3.3.5 Comparison and Conversion

The voltage level of the demodulated signal varies with the number of photons falling on the phototransistor. In addition, due to the noise introduced by the breadboard and potentiometers used in the circuit, the OFF voltage is held slightly above zero. A LM339 comparator is used to convert any signal above a 1 volt reference to a proper TTL level. This insures that a clean TTL voltage is presented during a MARK and not for line noise. R9 is used as a pull up resistor for the TTL levels.

The TTL voltage level is then presented to a 1488 RS-232 line driver chip. The 1488 accepts TTL voltage levels and produces the proper conversion to RS-232 levels. This output is connected directly to the UARTs Receive Data (RxD) pin.

CHAPTER 4

TEST AND EVALUATION

4.1 Introduction

Initially the transmitter and receiver were built approximately 4 inches apart on the same breadboard to allow testing with only one desktop PC; basic debugging and testing of the transmitter and receiver circuits were completed using a single PC connected to the infrared transmitter and receiver circuits in a loop back configuration. Once debugged, and with single character transmission accomplished, more extensive distance and file transfer testing was completed; the transmitter and receiver were placed on separate breadboards and a second computer was added in a dual PC communication configuration.

4.2 Single PC Loop Back

Figure 3 shows how the transmitter and receiver circuits were connected for use in a single PC testing environment. This is the simplest method to determine if the circuits are working properly. A simple program written in the BASIC computer language is used to transmit a single character out of the UART; the system then waits until a character has been received. If a character has been received, then it is outputed to the screen.

The program repeats this process continually. Appendix E shows a listing of the program. Once the circuits were determined to be working properly, then they were ready to be tested in a dual PC communication's environment.

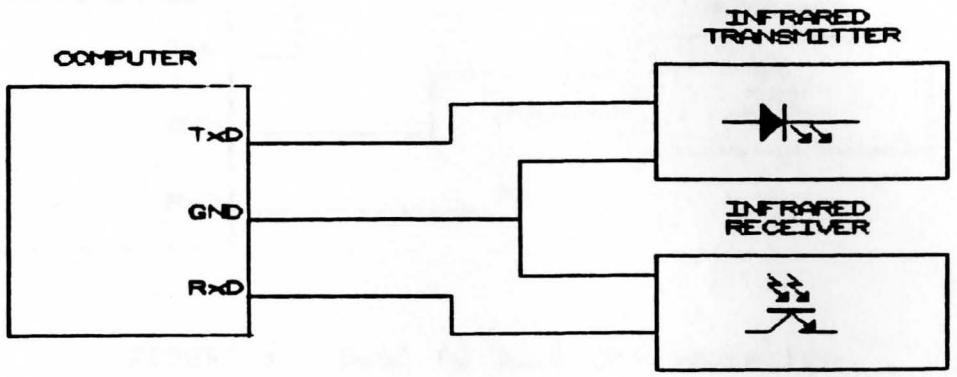


FIGURE 3. Single PC Loop Back Configuration

4.3 Dual PC Communication

For testing purposes, a single transmitter and receiver were used; In actual operation each PC will have a transmitter and receiver of its own. Figure 4 shows how the transmitter and receiver circuits were connected in the dual PC test environment.

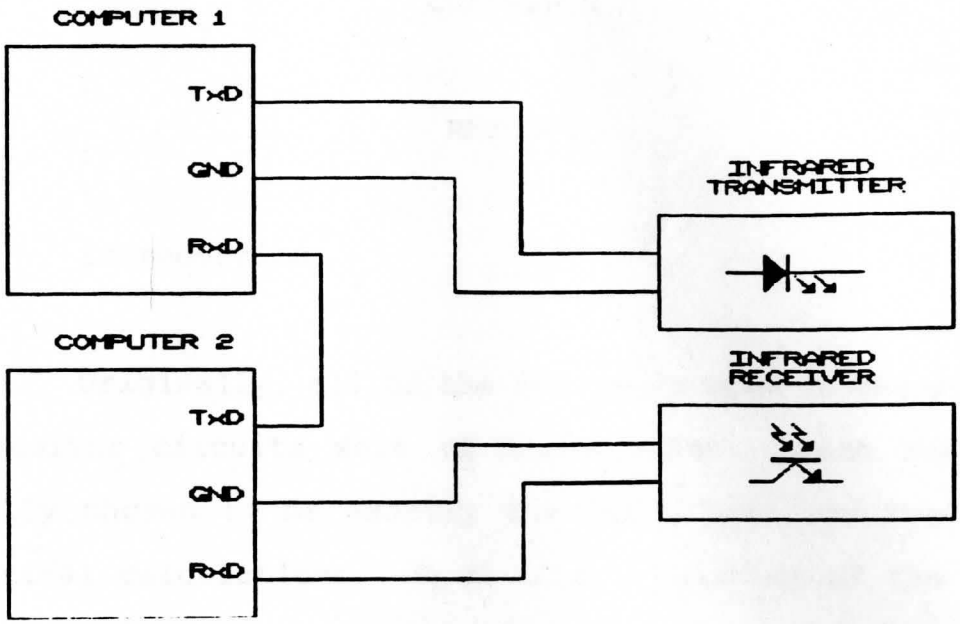


FIGURE 4. Dual PC Test Configuration

A commonly used file transfer package called Kermit was used to transfer entire files from the PC with the transmitter connected to it, to the other PC connected to the receiver. Kermit is a public domain send-and-wait packet protocol (discussed in Appendix B). The transmit and receive lines that are connected directly between the PCs (simulating another infrared transmitter and receiver) are needed to permit the package to send ACK and NAK packages back to the sender. Kermit is much too complex to discuss here. The circuits did work properly using this file transfer protocol. More information about Kermit can be obtained from the University library.[4]

---

[4]Kermit Protocol Manual, New York: Columbia University, April, 1984.

CHAPTER 5

RESULTS

5.1 Introduction

Originally, all of the resistors used in the transmitter and receiver circuits were of fixed value. Each resistor was carefully chosen to be exactly the value that resulted from the theoretical calculations. Upon initial testing of the circuits, using a multimeter and an oscilloscope, it was found that many of the voltage and current levels at various points throughout were not what was needed for proper operation. After further investigation it was found that the resistance and capacitance values varied at different points in the circuits.

5.2 Error

It was soon found that a large source of the error involved could be attributed to the resistances and capacitances built into the breadboard. The solution was to replace all fixed resistors with potentiometers; then, it was found that potentiometers introduce noise into the circuits. Eventually, a combination of potentiometers and fixed value resistors was found to be sufficient for proper operation.

Since the receiving circuit involves amplification, any

unwanted noise in the circuits result in unwanted noise amplification. Noise from the power supply was indeed a problem. To correct this, several large capacitors were placed on the breadboard between power and ground.

The circuits were then tested in the single PC loop back configuration, sending individual characters, and found to perform well at a 300 baud data transfer rate. A data transfer rate of 600 baud was attempted but failed. The bandwidth limitations of the op amps used simply will not allow a faster data transfer rate. The transmitter and receiver were then placed on separate breadboards and tested in the dual PC configuration. Complete file transfer, from one PC to another, at 300 baud, was successful at distances of up to approximately three feet.

CHAPTER 6

CONCLUSION

Based upon the technical results of this project and the fact that an infrared transmitter and receiver were built and tested in under two months from commercial, off-the-shelf hardware, it was determined that funding for advanced development including a complete team of engineers would be beneficial to the man-portable computer project and to the military in general.

As infrared technology develops and the cost of the associated electronics falls, asynchronous communications using infrared as the transmission medium will become widespread. Indeed, consumer electronics such as televisions and video tape recorders have been using infrared remote controls for years. With the availability of higher bandwidth op amps and fast switching infrared LEDs and phototransistors, electronic equipment with high speed transfer rates such as computers can take advantage of the wireless benefits of infrared.

Applications for infrared communications include use in environments where wires lying on the floor could be a safety hazard or where dirty, dusty, or oily environments will not allow exposed communication ports on computer-controlled equipment. Personal computers in an office could all be tied together on an infrared network with each PC reflecting its own transmission off a mirror, which is common to all others. Where security is

concerned such as in the military, infrared communications do not have to be limited to computer communications. Voice can be transmitted securely using infrared as well. The possibilities are limitless.

CHAPTER 7

RECOMMENDATIONS

7.1 Upgrades to Current Circuits

There are a few changes that can be made to the current infrared transmitter and receiver circuits to increase transmission distance and reduce the susceptibility to low frequency noise. An increase in transmission distance could be obtained by increasing the current through the infrared emitting diodes to their limit. This can be accomplished by either increasing the 5 volt supply or reducing the value of the current limiting resistors in the transmitter circuit. In addition, infrared-emitting diodes and transistors which will allow the flow of more current can be obtained (at an additional cost) and used.

At the receiver end, an increase in transmission distance can be obtained by improving the sensitivity; then it requires op amps with much greater bandwidths, permitting increased amplification. Higher bandwidth op amps would permit higher modulation frequencies. The smaller capacitances needed for rectification will result in faster data transfer rates. The use of higher modulation frequencies will also reduce unwanted low frequency noise; the filters can be designed to keep these frequencies from passing through and being amplified. Finally, the use of higher modulation frequencies will most likely add the need

for a multistage filter which will also contribute to faster data transfer rates.

7.2 Suggested Future Work

Some more exotic and time-consuming enhancements to the infrared transmitter circuit include the use of high intensity infrared LEDs controlled by a constant current modulator. Further, the transmitter could make use of a collimating lens to focus the infrared into a very narrow, intense beam, giving the infrared transmitter an unusually long range.

The receiver could make use of a fresnel lens which concentrates the infrared beam and directs it to the phototransistor. Additionally, the phototransistor/op amp detector portion of the receiver could be replaced with a PIN photodiode and a FET source follower circuit for increased sensitivity. This increase in sensitivity would allow the detection of weaker (farther away) transmission signals and hence improve the transmission distance.

Finally, a means of using the PCs own power supply to power both the infrared transmitter and receiver circuits needs to be developed so that a separate power supply is no longer required.

CHAPTER 8

SUMMARY

After thorough background research into asynchronous serial communication, an infrared transmitter and receiver were successfully designed, built, and tested at a maximum distance of approximately three feet. The basic background information needed to fully understand asynchronous communication is discussed in Appendices A through D. The hardware is discussed in chapter 3 and the testing procedure and software used is covered in chapter 4. The single PC loop back testing software is listed in Appendix E.

The goal of this project was to determine the feasibility of using infrared as the network transmission medium between computers; both the time and funding for completion of the project were severely limited. The results were to be used to determine whether or not additional funding for an advanced development and production effort by a team of engineers was warranted.

All of the goals of this project were met. Background research, design, testing, and evaluation of the infrared transmitter and receiver circuits were accomplished in under two months. In addition, they were built completely from commercial off-the-shelf components which kept cost at a minimum. Finally, the successful transfer of files at a distance of three feet was enough to warrant further funding for advanced development of infrared transmitters and receivers.

APPENDIX A

SERIAL ASYNCHRONOUS COMMUNICATIONS

The Asynchronous Communications Element (ACE) is a device designed to send and receive serial data asynchronously. In a PC, the ACE is the UART chip which has to transform data from an internal, parallel format to a bit-at-a-time serial format. In order to understand the ACE fully, background information on asynchronous serial communications is needed. This will provide context for the discussion in the following sections. First, the concepts of serial transmission vs parallel transmission will be discussed and then the tradeoffs of these two alternatives will be analyzed.

A.1 Serial Communications

Consider two computers that need to send ASCII character data back and forth to each other. What are the options? Since digital data is sent in discrete chunks, we have two obvious options: send one character at a time (parallel transmission) or send one bit at a time (serial transmission). If we send one character at a time, we will have to have one data line per bit, or eight data lines for an extended ASCII character. Figure 5 illustrates these differences.

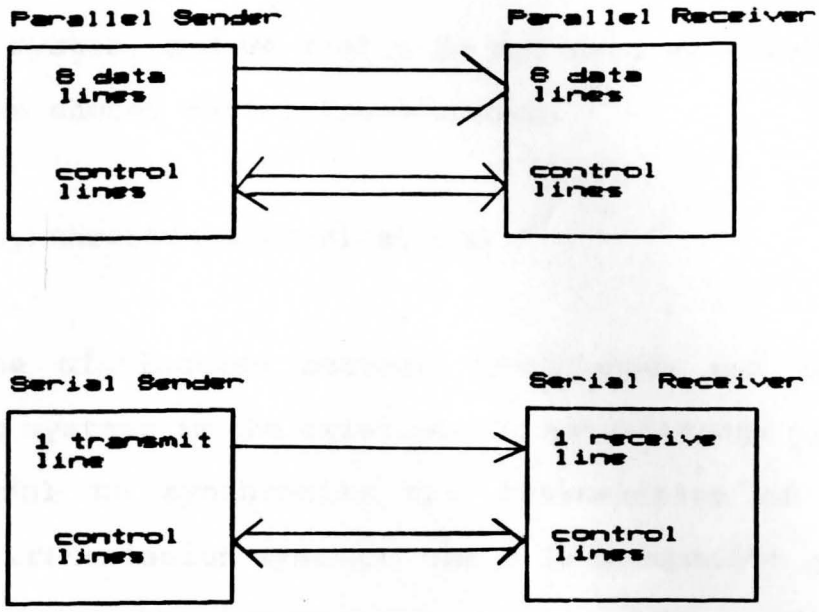


FIGURE 5. Serial vs Parallel Transmission

Further, if we want to send both ways at the same time (i.e., full-duplex transmission), we will need sixteen lines, not to mention a few lines for control signals. This is technically feasible within a single physical installation and will allow much faster, and therefore much greater capacity, transmission than with serial transmission schemes. However, the cost of the data lines is much more expensive.

Serial transmission provides slower transmission, that is, lower data rates than parallel transmission. Nevertheless, the lower costs outweigh the negative aspects for many transmission systems except those with very high data traffic

requirements. For microcomputers, the case is clear. We need an inexpensive system, and we really do not need extremely high data rates. So we choose serial transmission.

A.2 Asynchronous Communications

The distinction between synchronous and asynchronous transmission systems is the existence or nonexistence of a clocking control signal to synchronize the transmission of data. In synchronous transmission systems, there is a separate control wire for synchronizing the transmitter and receiver. When a signal appears on this control wire, the receiver reads the data off the data wire (or wires). There is no such synchronizing mechanism in asynchronous transmission systems so that synchronization must be achieved by different means. For the serial asynchronous transmission system provided by the ACE, the synchronizing mechanism is the start bit that precedes each stream of data bits (see Figure 6[5]).

---

[5]IBM Technical Reference Manual, rev. ed. (April 1983), p. 1-226.

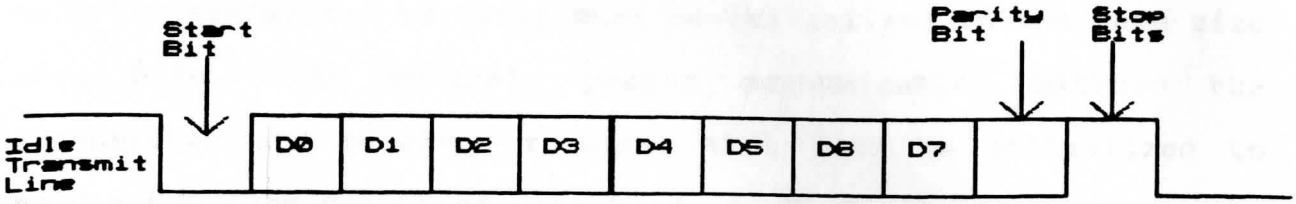


FIGURE 6. Serial Data Format

The start bit allows the receiving ACE to synchronize its internal clock to the incoming character. Thereafter, it will use its internal clock to sample the incoming signal at approximately the middle of each incoming bit and shift the sampled value (one or zero) into the end of a shift register. When the stop bit arrives, signaling the end of the character, the ACE moves the assembled character into a holding buffer and signals the CPU that a character has been received. The ACE is designed to stay in step with the transmitter only through the end of a single character, so it must resynchronize for every character it receives.

The hallmark of asynchronous transmission is the fact that characters can arrive at any time. Between characters, the line is held at a high (1) by convention. This is called the "marking condition," or just simply "marking." The "space" condition (or "spacing") is the term applied when the line goes low (0). A start bit is defined as the line held at 0 (spacing) for 1-bit time. Any shorter time will be interpreted as line noise.

The stop bit is defined to be the line held at 1(marking) for 1-, 1½-, or 2- bit times, depending on how the ACE is initialized. Both the sender and receiver must be initialized to the same size stop bits. In general, proper communication between the transmitter and receiver requires that both be initialized to handle the same number of data bits (5, 6, 7, 8), the same parity convention (odd, even, or none), and the same stop bit length. If one is initialized differently from the other one, transmission errors will result.

APPENDIX B

INFORMATION TRANSFER

B.1 Baud Rate

Since "baud" is often incorrectly used to mean "bits per second," it is worth spending a few moments to differentiate between these two terms. Baud rate is the measure of the fundamental electrical signaling rate of a communications line. Stated another way, baud rate is the frequency at which electrical impulses are transferred to the communications line. Because it is an electrical unit of measure and not a unit of information, baud rate implies no relationship between the voltages that appear on the communications line and the data represented by those voltages.[6]

Although it sounds simple, the rate of transfer of information is the bit transfer rate, and is expressed in bits per second (bps). The baud rate and the bit transfer rate are therefore equal only when one data bit is encoded during one signaling period.

---

[6]Ted J. Biggerstaff, Systems Software Tools, Prentice Hall, 1986, p.88

B.2 Communications Line Usage

Because of the enormous expense and difficulty in erecting telegraph and telephone lines, where serial communication was originally used, researchers constantly searched for a way to send more than one message simultaneously (or apparently so) over the same line. Eventually the following terminology was used to describe the traffic on communications lines:

Simplex: Communication is single-direction with a receiving or a transmitting device (but not both) at either end. A ticker-tape device is an example of a simplex receiver.

Half-duplex: Communication is possible in both directions, but not simultaneously. Many modern forms of communication devices work in this manner, including the CB radio.

Full-duplex: Communication can occur simultaneously in both directions. The Telegraph quickly became one of the earlier devices to use this; today most two-way communication is full-duplex.

Multiplex: This form of communication is used if more than a single channel of information is required. Multiplexing is a technique for creating several communications channels by sequentially allocating frequencies or time slices from a single channel.

More and more communication systems rely on multiplexing.

B.3 Flow Control

Before communications can begin, a physical communications link must be established. This link can be: (1) a simple cable connecting a computer to its CRT, (2) two computers exchanging data over the telephone network with modems, or (3) two computers, exchanging data, directly connected together.

Regardless of how simple or complicated the link may be, there is no guarantee that the receiver is unconditionally able to accept all of the sender's data. For example:

1. You are sending characters to a printer. To compensate for the computer's ability to send characters faster than they can be printed, the printer thoughtfully provides a few bytes of buffer storage where characters can wait their turn to be printed. When the buffer becomes full, the printer output becomes garbled.

2. Your microcomputer is reading bytes from the communications line and storing them one by one onto a floppy disk file. Even though your operating system buffers the characters for you, sooner or later it must perform a physical write to the floppy. During the eternity (in computer time) taken to write to the floppy, bytes are lost.

These two examples show the need for flow control- the

modification of the amount or rate upon the needs or responses of the receiver.[7] The modifications may be as simple as performing the data transfer at a slower data rate, or as complicated as wholesale reformatting of the outgoing data to match that of the receiver.

B.3.1 Flow Control Protocols

Almost everyone who has used a microcomputer has pressed Ctrl-S to pause a screen listing. Every time this key is pressed you have participated in flow control by signaling the computer that it is overwhelming a peripheral device (you!) with data. Hardware devices such as printers and plotters also require flow control. This often takes the form of voltage changes on the pins of the serial interface connector. This is hardware flow control. Where a physical connection between the communicating devices is impossible (such as infrared) or when hardware flow control is not supported, software flow control is necessary. That is, instead of signaling by means of control wires, they make known their intentions by sending data over the communications channel.

Most flow control measures fall into two categories.[8]

1. Procedural flow control assumes that the sender has intimate, detailed knowledge of the receiver's ordinary response to arriving data. In each case, the sender adjusts one parameter

---

[7]Joe Campbell, C Programmer's Guide To Serial Communications, Howard W. Sams and Company, 1988, p.75

[8]Ibid., p.78-79

such as the end-of-line delimiter based upon prior knowledge about the receiver. Although this can be effective, it does have its drawbacks, namely, is enough really known about the way the receiver behaves? Flow control procedures based upon timing are very unreliable because of the number of variables introduced; any of the following changes may cause a change in the receiver's timing: an increase in the number of users or jobs, installation of new device drivers, and changes in hardware. In general, purely procedural flow control techniques that work perfectly today may fail tomorrow.

2. Cooperative flow control involves a sender and receiver agreeing upon and observing a common set of rules to govern the exchange of data between them. The term usually used when applying these rules is protocol.

B.3.2 Character Protocols

The most popular character flow control protocol is known as XON/XOFF. Here, the sender and receiver assign special meaning to two characters, which are then inserted into the stream of data as flow control markers. These characters are given the functional names XON and XOFF; their actual identity varies from system to system. The most common assignment is DC3 (Control-S) for XOFF and DC1 (Control-Q) for XON.

The receiver sends the XOFF character when it wishes the sender to pause in sending data, and an XON character when it

wishes the sender to resume. (Often XOFF is referred to as the "holdoff" character, and XON as the "release" character.)

XON/XOFF is so uncomplicated that it seems foolproof as long as both the sender and receiver respect the protocol. However, problems can arise. For instance, the WordStar word processing package uses DC3's (generated with Ctrl-P Ctrl-S) as internal markers for the beginning and end of underscoring. If the system is using XON/XOFF and you try to download a document created using WordStar, it will stop transmitting every time underscoring is encountered in the document and won't continue until the operator issues a XON. Other packages may result in similar side effects.

There is one important variation to the XON/XOFF protocol: instead of defining XON as a single character, the receiver accepts any character as a signal to resume transmission. Used in an echoing environment, this variant, which is generally found only on video terminal drivers, enables a user to stop and start screen output with a single key. When a non-human receiver uses this style of XON/XOFF, however, the sender occasionally seems to ignore an XOFF. To understand why, visualize this: the sender receives the XOFF, it ceases transmission and awaits an XON. Meanwhile, after sending the XOFF, the receiver immediately receives and echoes the letter which was already in transmission. The sender regards this echo of its own letter as its "any character XON" and immediately begins to transmit. So clearly other solutions of transmission must be sought.

B.4 File Transfer Protocols

We have examined flow control at the level of single character level. A larger, far more complicated kind of protocol governs transfer of arbitrary blocks of data. Although used for a variety of applications in synchronous communications, block protocols in asynchronous communications are usually found only in programs that transfer entire files. They are referred to as File Transfer Protocols (FTP).

In virtually every asynchronous file transfer protocol used on microcomputers, the basic unit of transfer is the packet. A packet is a grouping of a variety of byte-elements or fields. Only one of the fields contains the file data; the remaining fields, known as service fields, contain the information required for the receiver to verify that the packet is error-free. The number and purpose of the control fields vary from protocol to protocol, but in general most contain a packet signature field (usually beginning with an Start of Header (SOH) byte), a packet-sequence number, a data field, and a checkvalue also known as a checksum.

B.4.1 Automatic Repeat Request (ARQ) Protocols

The most common type of packet protocol is the Automatic Repeat Request (ARQ) in which an error detected in a received

packet or an unacknowledged packet automatically results in the retransmission of that packet. There are several types of ARQ protocols; however, I shall discuss two of the most common: (1) Send-and-Wait ARQ, and (2) continuous ARQ.

During Send-and-Wait ARQ transmission, data from the file is "packetized" by surrounding it with the service fields. An entire packet is then transmitted blindly (i.e., with no flow control); the sender then waits for the receiver to acknowledge its receipt.

The receiver inputs the packets and, after verifying that the packet is in the correct sequence relative to the previous packet, computes a local checkvalue on the data portion of the packet. If the local checkvalue matches the one in the packet, the receiver acknowledges by sending an ACK; otherwise, the receiver negatively acknowledges with a NAK (both ACK and NAK are considered acknowledgments). The ACK and NAK may actually be in the form of entire packets instead of single characters. Upon receipt of an ACK, the sender transmits the next packet: if a NAK is received, the same packet is transmitted again. Transmission proceeds in this manner until the entire file has been transferred.

The diagram in Figure 7 oversimplifies the process; this is a two-way conversation and the receiver's acknowledgments are just as susceptible to damage as the packets themselves. Consider the following: the receiver inputs and verifies a packet, sends an ACK, then proceeds to input what it expects to be the next packet in the sequence. Somehow, though, the receiver's ACK never reaches

the transmitter who, after some timeout interval, retransmits the same packet. To prevent a duplicate block of data, the receiver must recognize that it has received the same block twice. It does this by ignoring the packet and then sending another ACK.

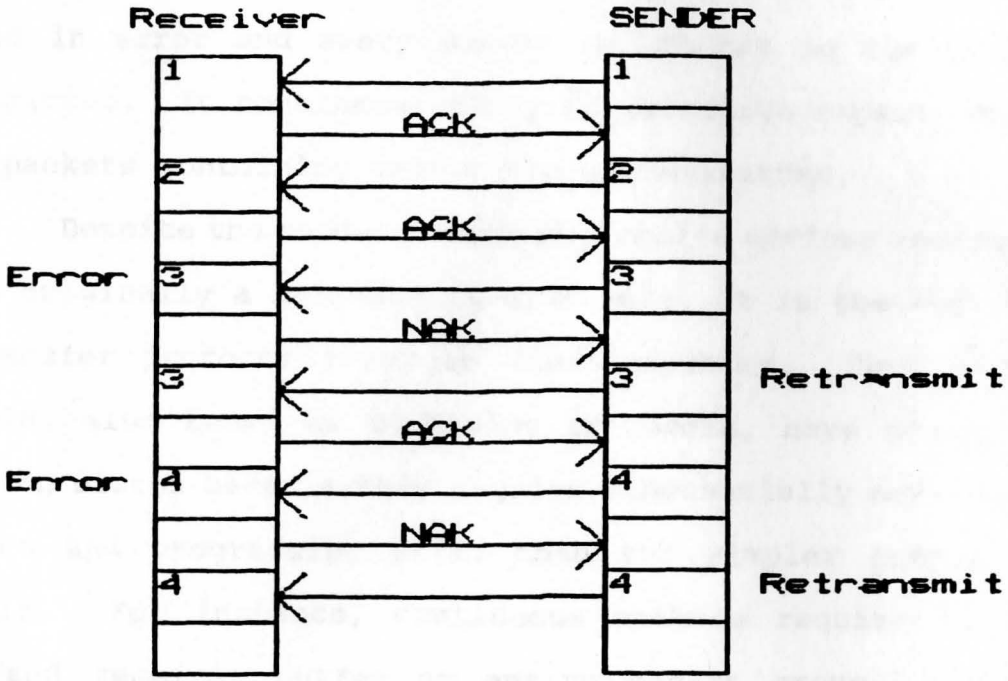


FIGURE 7. Send and Wait ARQ

In a continuous ARQ protocol, the transmitter does not pause after each packet but transmits several packets in a row (the packet group). The receiver examines each packet and, as in send-and-wait ARQ, sends an acknowledgment (ACK or NAK) based upon the content. In this case, however, the packet's number is included

along with the acknowledgment. During transmission, the sender continually examines the stream of acknowledgments returning from the receiver and keeps track of the packets that are received in error. After the entire group of packets has been transmitted, the sender then retransmits the ones that contain errors.

There are two methods for retransmitting the erroneous packets. In continuous ARQ with fallback, the first packet number received in error and every subsequent packet in the group are retransmitted. In continuous ARQ with selective repeat, only the actual packets containing errors are retransmitted.

Despite the send-and-wait protocol's obvious inefficiency (it was originally a half-duplex protocol), it is the most common file-transfer protocol found on microcomputers. Continuous ARQ protocols, also known as windowing protocols, have never become popular on micros because they require substantially more computer resources and programming skill than the simpler send-and-wait protocols. For instance, continuous methods require that both sender and receiver buffer an entire packet group (window) in memory at one time.

B.5 Packets

The number of different packet designs is unlimited, but their most obvious differences lie in the manner in which the DATA field is distinguished within the packet. There are three basic approaches: (1) marking the beginning and end of the DATA field

with control characters, (2) including the length of the DATA field in the packet, and (3) fixed length DATA field.

B.5.1 The Control Character Marked Packet

The simplest form of packet is that used for transferring strictly textual data; that is, the file is expected to contain only ASCII plain text: the alphanumeric characters plus the six control characters defined as Format Effectors (BS, HT, LF, VT, FF, and CR). The other control characters may not appear in the DATA field, but they may appear in other fields. A hypothetical version of such a packet is shown in Figure 8.

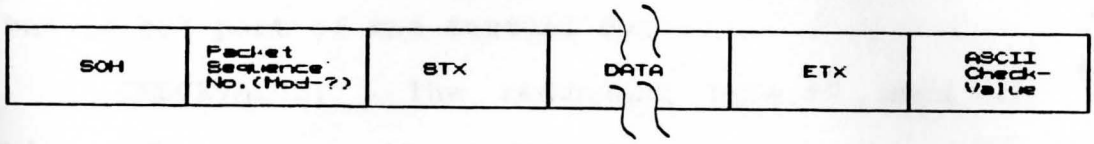


FIGURE 8. Hypothetical Packet for Transfer of Text Files

SOH: (Start of Header) This control character marks the beginning of a packet. This is the official purpose in ASCII.

Packet Sequence Number: The next byte describes the packet's position in the current transfer. Its purpose is to enable the receiver to verify that the packet received is the one expected. To achieve this goal it is not necessary to know the

packet's absolute position in the overall transfer (which may be a huge number), but merely its relative position in a limited sequence of packets. Accordingly, this field is usually limited to a single byte and, in some cases, the sequence number may be confined to a few significant bits of the field. This is expressed in the label "Packet sequence number modulo-?." In simple send-and-wait ARQ protocols, the sequence field can even be modulo-2; i.e., "this" packet or "that" packet. If all 8 bits of this field are significant, the packet number is calculated modulo-256; 6 bits are modulo-64, and so on.

STX: (Start of Text) This control character marks the beginning but is not part of the textual data.

DATA: This contains the textual data.

ETX: (End of Text) This control character marks the end but is not part of the textual data.

CHECKVALUE: The redundant byte(s) used for error checking. To preserve the ASCII character of the protocol, the checkvalue may be represented with ASCII digits.

The data in an STX/ETX marked packet may be of variable length, although the penalty of having to retransmit a very long packet means that the maximum length of the packet should be short. Packet lengths for popular protocols range from 64 to 512 bytes. Regardless of its length, the receiver knows that the data begins at the byte after the STX byte in the packet and ends with the byte before the ETX byte.

Text-only protocols are necessary in some mainframe

environments where the programmer cannot control the communications lines directly. These systems may use the high order bit for parity (or even arbitrarily omit it altogether). However, text-only protocols are not portable across operating systems because each system processes input and output differently. The STX/ETX protocol, for example, does not work on a system that discards or translates control characters.

B.5.2 Size-Field Marked Packet

When communication is between computers that have absolute control over communications lines, and this includes microcomputers, the use of a binary packet makes more sense. Since binary files may contain any 8-bit value, the DATA field cannot, as the text packet can, be marked with control characters. The alternative, as shown in Figure 9, is to include the size of the DATA field in the packet. The size field, labeled LEN, is the number of bytes in the DATA field. The number of bytes allotted to the length field limits the number of bytes that can be sent in one packet; a 1-byte length field, for example, limits the DATA field to 256 bytes.

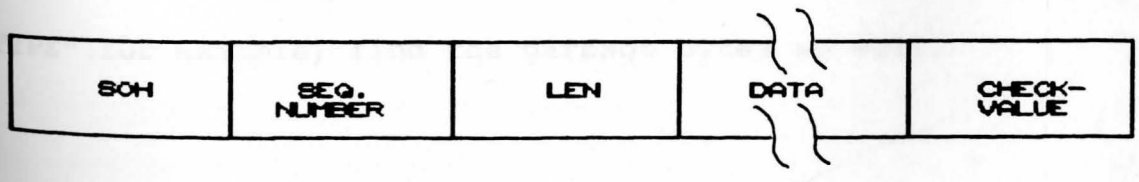


FIGURE 9. Hypothetical Packet for Transfer of Binary Files

B.5.3 The Fixed Length Data Field Packet

The third type of packet simply assumes a fixed length for the DATA field. There is one major drawback- there is no way to send a "short" packet. A short packet is necessary whenever the original file's length is not evenly divisible by the fixed block size chosen. In other words, at the end of a file transfer, there are probably not enough bytes in the file to fill an entire packet. The final packet therefore contains some non-file data: either garbage bytes or a padding byte specified in the protocol. In any case, because a file created by a fixed length protocol likely contains one or more garbage bytes at the end, it is not an exact copy of the original. This brings up the subject of invertibility. If a file is transferred from one system to another, then back again, the recovered version on the first system should be identical to the original. The destination system can alter the file during its residence there, but must reverse (invert) the changes during retransmission.

Protocols with fixed length DATA fields create inherently non-invertible files. The extra bytes at the end of the file often affect the file's utility or serviceability. Utilities that rely upon the number of bytes in a file as given in its directory entry ("TYPE" for example) find the garbage bytes as well.

APPENDIX C

MODEMS AND MODEM CONTROL

C.1 The Modem

A device that performs modulation and demodulation on a communications line is known as a modem. In the computer world the term "modem" is used almost exclusively to describe devices that operate over telephone lines; however, modems are used on many different communications lines. A great deal of data, for example, is sent between computers at radio frequencies via RTTY (radio teletype) modems. Another non-telephone modem is the short haul modem, which sends modulated tones over ordinary wire. Short haul modems are usually found where both pieces of equipment are located on the premises or where a noisy electrical environment doesn't allow the use of ordinary cables.

C.2 Bandwidth

Digital signals from devices such as teleprinters and microcomputers cannot be sent directly over all types of communication lines. Telephone lines are typically used as the transmission medium between remote microcomputers. Because a telephone line is intended to carry only human speech, which

contains frequencies in the range of 200-8000 Hz[9], its frequency response (bandwidth) is rather limited. This bandwidth limitation is not unique to telephone lines, however, but exists in varying degrees within any transmission line and in the electronic devices used in transmitters and receivers of digital data.

This bandwidth limitation enormously complicates the transmission of digital pulses over lines. In addition, noise is commonly introduced from other lines and the external environment further distorting the digital pulses. From the standpoint of circuit design, an instantaneous transition between the 1 and 0 states is ideal. In other words, the perfect digital signal consists of clean, sharp, square waves with perfectly vertical sides and perfectly flat tops. To transmit an acceptably square digital signal, the communications medium must have a significantly wider bandwidth than the frequency of the square wave itself. Otherwise, the high frequency components are stripped out and along with them the sharpness of the square waves. If the bandwidth is too narrow, then the resulting waves are not recognizably "square". At the receiver, the logic levels of the digital signal becomes ambiguous and communication fails. Figure 10 approximates how a 2000 bps signal would be deformed by progressively narrower bandwidths. Notice that the square wave becomes barely acceptable when the bandwidth is 4000 Hz. Figure 11 shows how small noise spikes may transform one logic level into another producing a data

---

[9]Joe Campbell, C Programmer's Guide To Serial Communications, Howard W. Sams and Company, 1988, p.116

error.

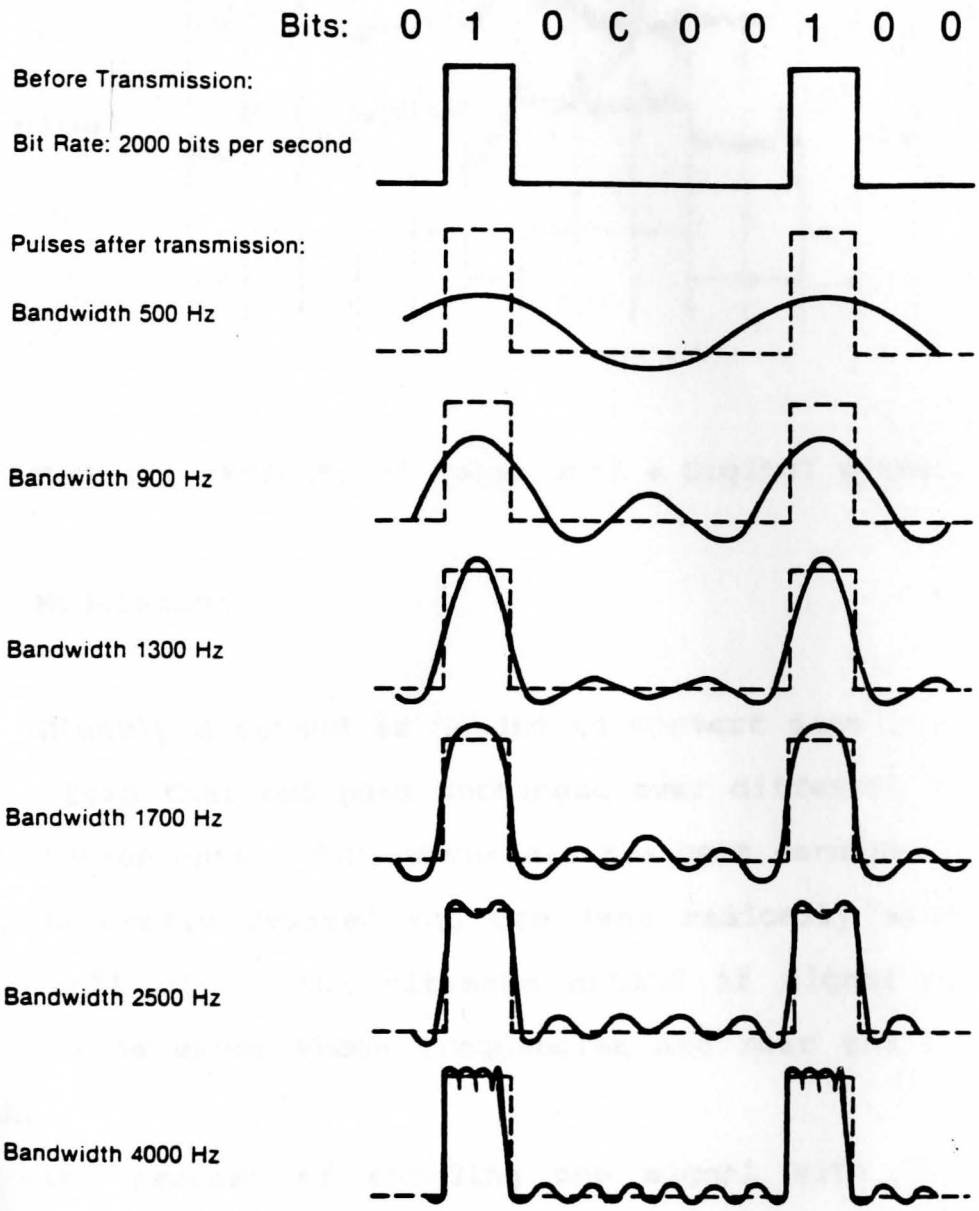


FIGURE 10. Effects of Bandwidth on Square Digital Signals

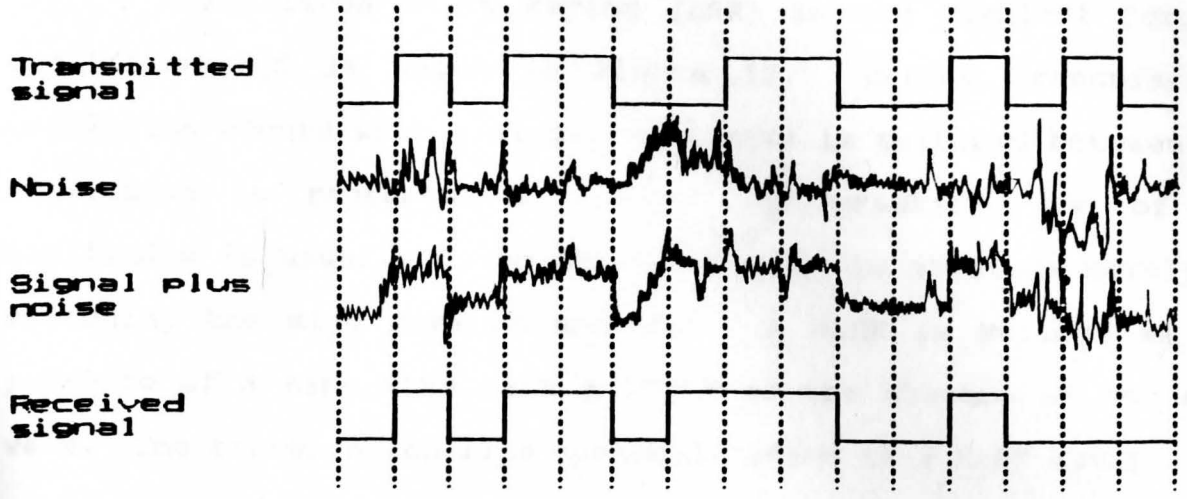


FIGURE 11. Effects of Noise upon a Digital Signal

C.3 Modulation

Clearly a method is needed to convert data from square waves to a form that can pass unchanged over different media and in noisy environments. Sine waves are the best candidate because they can be easily created and are less radically affected by frequency roll off. The ultimate method of signaling should consist of sine waves whose frequencies are near the center of bandwidth.

The process of encoding one signal with another is modulation and the recovery of the original signal is demodulation. There are several types of modulation. The three most commonly used are: amplitude shift keying (ASK), frequency shift keying (FSK), and phase shift keying (PSK).

Amplitude shift keying (ASK) is the simplest form of modulation and is shown in Figure 12. During transmission, modulation occurs when a single sine wave is switched between two amplitudes to represent 1 and 0. In practice, one of the amplitudes is usually 0, so the modulation is attained merely by switching the sign wave on and off. A MARK is defined as the presence of a sine wave, and a SPACE as the absence of the sine wave. The transmission line typically idles at a MARK state. The receiver demodulates the signal by outputting 1s and 0s as the sine wave appears and disappears.

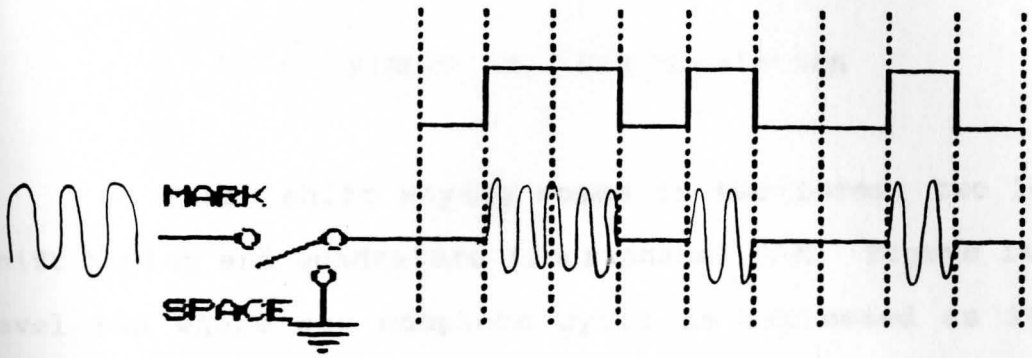


FIGURE 12. Amplitude Modulation

Frequency shift keying is becoming more popular over ASK as low noise environments become difficult to achieve in an increasingly electronic world. Whereas electrical noise changes a signal's amplitude, no known natural phenomenon changes its frequency. Much more reliable encoding can therefore be attained

by frequency modulation. Since modems need only transmit 1s and 0s, data can be represented by switching between sine waves of different frequencies. Figure 13 shows FSK modulation.

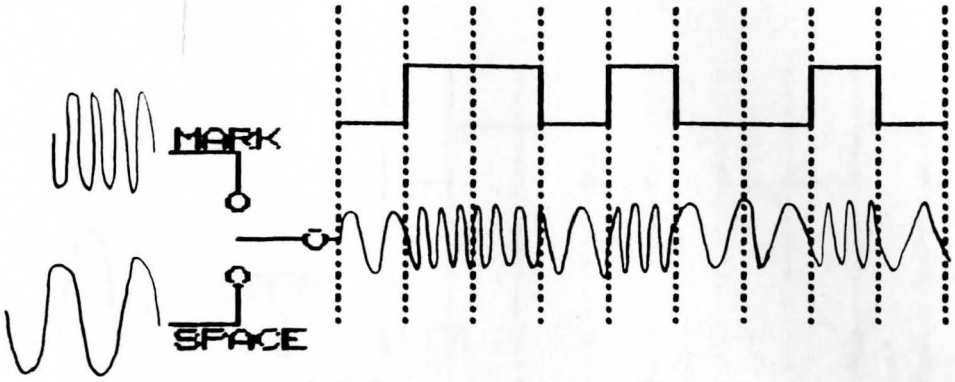


FIGURE 13. FSK Modulation

Phase shift keying comes in two forms: two level phase shift keying and quadrature (four phase) PSK. Figure 14 shows two level PSK where one complete cycle is expressed as 360°. With respect to waveform A, waveform B is said to be in phase or, stated differently, its phase angle is 0°. Waveform C, however, lags behind waveform A by 180° and its phase angle is -180°. Modulation consists of sending waveform C for a SPACE, and waveform B for a MARK. Both sender and receiver are assumed to have a local copy of waveform A, so it need not be transmitted. To demodulate the signal, the receiver adds the incoming waveform to its local copy of waveform A. If the result of this addition is 0 (C+A=0) a SPACE is decoded. Conversely, if the result is non 0 (B+A≠0) a MARK is

decoded. Quadrature phase shift keying (QPSK) is identical to the previous example except instead of encoding bits in two phase angles (0° and -180°), four phase angles are used-0°, 90°, 180°, 270°.

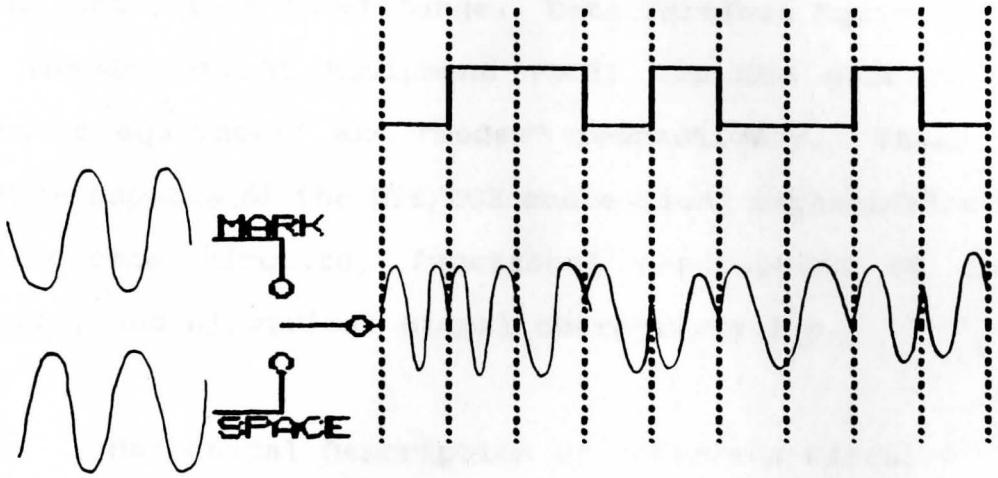


FIGURE 14. Two Level PSK

C.4 The RS-232 Standard

There are two ways to control or monitor the behavior of a modem: through hardware (wires between the computer and modem) and software (sending commands in the data stream). Formal standards for the first method are found in the Recommended Standard Number 232, Revision C from the Engineering Department of the Electronic Industries Association, better known as EIA RS-232C, or simply RS-232. There are no formal standards for controlling modems via commands in the data stream, but modems made by

manufacturers such as Hayes Microcomputer Products, Inc., have become so popular that they have become de facto microcomputer standards.

The formal name of the RS-232C is Interface between Data Terminal Equipment and Data Communication Equipment Employing Serial Binary Data Interchange. Data Terminal Equipment (DTE) and Data Communications Equipment (DCE) are the generic terms for "computer equipment" and "modem" respectively. There are three separate aspects of the DTE/DCE connection: mechanical description of interface circuits, functional description of interchange circuits, and electrical signal characteristics.

C.4.1 Mechanical Description of Interface Circuits

The RS-232 standard states that there should be two connectors- female for the DCE, and male for the DTE. There are 25 defined and assigned pin numbers on the connector. Table 2 shows these assignments. RS-232 functions are divided into data functions and control functions. The data functions are the transmitter and receiver pins 2 and 3 respectively. These are the only two pins through which data flows; the rest are control functions.

Eliminating the circuits in Table 2 that are unassigned or related exclusively to synchronous transmission leaves only the RS-232 circuits used for asynchronous I/O on microcomputers. Each of these 11 pin numbers is shown in Table 3 followed by the

abbreviation of its function (instead of the circuit name), and the direction of its action.

TABLE 2. The 25 pin assignments for RS-232

Pin	Circuit	Name
1	AA	Protective ground
2	BA	Transmitted Data
3	BB	Received Data
4	CA	Request to Send
5	CB	Clear to Send
6	CC	Data Set Ready
7	AB	Signal Ground of Common
8	CF	Data Carrier Detect
9	--	Reserved for testing
10	--	Reserved for testing
11	--	Unassigned
12	SCF	Secondary Received Line Signal Detect
13	SCB	Secondary Clear to Send
14	SBA	Secondary Transmitted Data
15	DB	Transmission Signal Element Timing
16	SBB	Secondary Received Data
17	DD	Receiver Signal Element Timing
18	--	Unassigned
19	SCA	Secondary Request to Send
20	CD	Data Terminal Ready
21	CG	Signal Quality Detector
22	CE	Ring Indicator
23	CH/CI	Data Signal Rate Detector
24	DA	Transmit Signal Element Timing
25	--	Unassigned

TABLE 3. RS-232 Pins for Asynchronous I/O

Pin	Abbreviation	Name	Direction
1	--	Protective Ground	------
2	TD	Transmitted Data	to DCE
3	RD	Received Data	to DTE
4	RTS	Request to Send	to DCE
5	CTS	Clear to Send	to DTE
6	DSR	Data Set Ready	to DTE
7	--	Signal Common	------
8	DCD	Data Carrier Detect	to DTE
20	DTR	Data Terminal Ready	to DCE
22	RI	Ring Indicator	to DTE
23	DSRD	Data Sig. Rate Det.	either

When computers implement software protocols as discussed earlier, the RS-232 interface circuits used can be minimized. The simplest connection, known as the Null Modem, is shown in Figure 15.

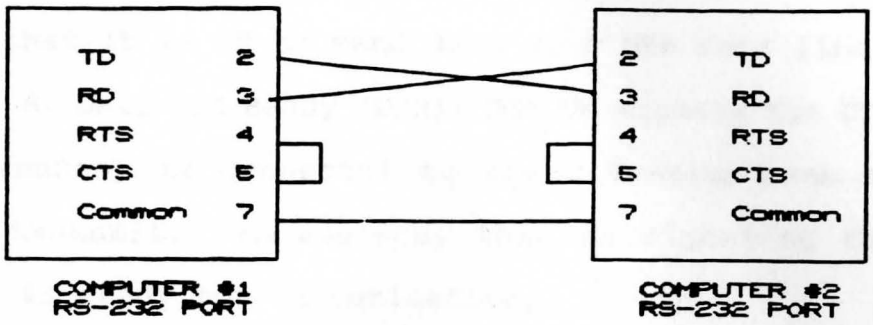


FIGURE 15. The Null Modem

C.4.2 Functional Descriptions of Interchange Circuits

1. Protective Ground: An optional circuit usually grounded to the equipment frame. It plays no part in the signaling system.

2. Transmitted Data: This is the wire on which the DTE (PC) passes characters to the DCE (modem) in the format given in Figure 6. According to the standard, data may not be passed on this circuit unless the following four signals are all ON: RTS, CTS, DSR, and DTR. When data is not being passed, this circuit is held in marking condition (high).

3. Received Data: This is the wire on which the DCE

(modem) passes characters to the DTE (PC). This circuit is held in marking condition (high) when no data is being passed.

4. Request To Send (RTS): The DTE (PC) is asking the DCE (modem) for permission to send data. The DCE (modem) will respond with a Clear To Send (CTS) if it is OK.

5. Clear To Send: The DCE responds to an RTS telling the DTE (PC) that it is OK to send data over the data line.

6. Data Set Ready (DSR): DSR ON signals the DTE (PC) that the DCE (modem) is connected to the communications channel and ready to transmit. In essence, this is signaling that the DCE equipment is ready for communications.

7. Signal Common: This is a zero volt reference signal. All other signals are positive or negative with respect to this signal.

8. Data Carrier Detect (DCD): This signal is also called Received Line Signal Detect. This is a signal from the DCE (modem) to the DTE (PC) telling the PC that it has received a suitable data carrier signal. When this signal is off, that is, the receiving modem is not detecting carrier, the Received Data circuit is held in the marking condition.

9. Data Terminal Ready (DTR): This signal is from the DTE (PC) telling the DCE (modem) that the DTE equipment is ready for communications.

10. Ring Indicator (RI): This signal is used in auto-answer modems. It is a signal from the DCE (modem) to the DTE (PC), indicating that the modem is receiving a ringing tone. This

is not used for communicating on anything other than telephone lines.

11. Data Signal Rate Detector (DSRD): If two data rates are possible, the higher of the two is represented by asserting DSRD.

C.4.3 Electrical Signal Characteristics

EIA allows speeds from 0 to an upper limit value of 20,000 bits per second. In most installations, the data rate is limited to 19,200 bps. The standard also cautions against cable lengths in excess of 50 feet unless the total cable capacitance is less than 2500 picofarads.

The RS-232 standard specifies a bipolar logic level. That is, logic levels are represented not only by the magnitude of voltage levels, but by the polarities as well. The maximum voltage permitted on any circuit is ±15 volts. The RS-232 standard actually defines four logic levels. Figure 16 shows the logic-level definitions of RS-232 for inputs and outputs. Binary logic levels for outputs are +5 to +15 and -5 to -15; voltages between +5 and -5 are undefined. Binary logic levels for inputs are +3 to +15 and -3 to -15; voltages between +3 and -3 are undefined. The different logic level from input to output is referred to as the noise margin. It also means that the interface can tolerate 2 volts of noise peak.

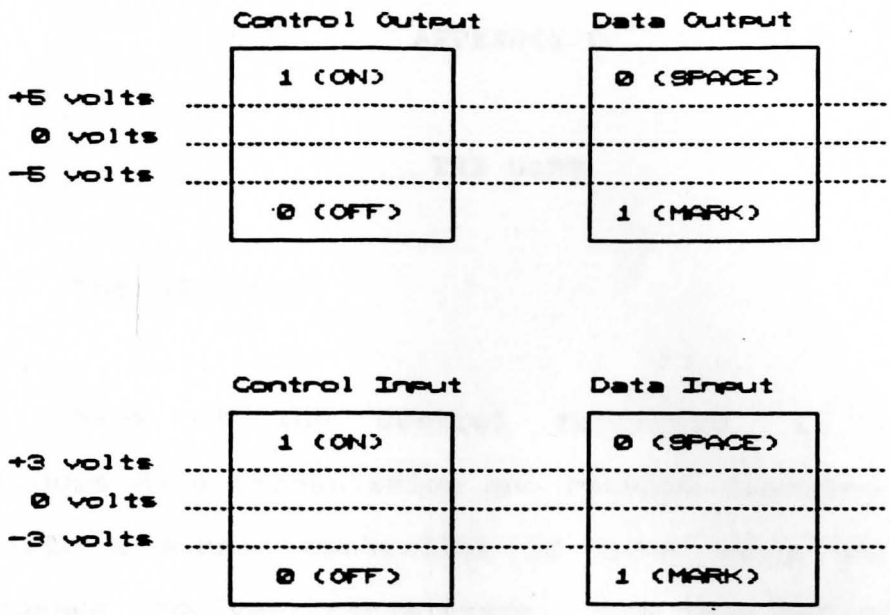


FIGURE 16. RS-232 Logic Levels

APPENDIX D

THE UART

D.1 Introduction

Many of the control functions, as well as the asynchronous data transmission and receipt discussed so far, are built into a single controller IC known as a UART (Universal Asynchronous Receiver/Transmitter). The idea behind the UART is to relieve both programmer and processor of the toil associated with asynchronous serial I/O. To receive and send data, the program simply reads and writes bytes to the UART, which appears to the processor as one or more ordinary memory locations or I/O ports. The UART's circuitry handles the details of assembling and reassembling bytes, handles the timing, and in general unburdens the processor.

D.2 The UART Transmitter

A byte to be transmitted is written to the address of the UART's transmitter where it eventually is presented to the transmission section. This section consists largely of a shift register, the control logic to load the byte into the shift

register, and one or more transmitter buffers. Figure 17[10] shows these functions. The transmitter itself consists of a parallel input, serial output shift register. The bits to be transmitted are loaded into the shift register, then shifted out on the negative transition of the transmit data clock. When all bits have been shifted out of the transmitter's shift register, the next Serial Data Unit (SDU) is loaded and the process repeats. The data bits may be loaded directly from the system data bus, but most UARTs contain a transmitter buffer, or Transmitter Holding register which forms a small queue in which data can be temporarily stored while awaiting serialization. A byte for transmission can therefore be written into the UART's holding register while the previous byte is still being clocked out of the shift register.

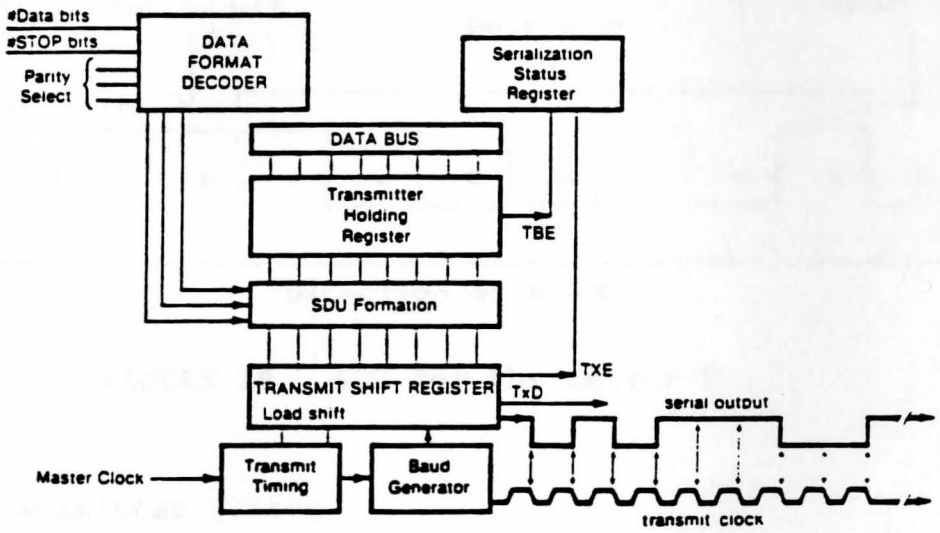


FIGURE 17. UART Transmitter Functions

[10]Joe Campbell, C Programmers's Guide To Serial Communications, Howard W. Sams and Company, 1988, p.158

D.2.1 Framing

Since a SDU must begin with a SPACE (0) bit, a 0 is automatically loaded into the first bit of the SDU. Three elements of the SDU, however, are variables: the number of STOP bits, parity, and the number of data bits. The formation of the SDU is done between the transmit buffer and the shift register. For example, Figure 18 shows how a UART programmed for 7 data bits, even parity, and 2 stop bits would build an SDU for the letter 'E'.

Notice that regardless of the format in effect, unused SDU bit positions are left-filled with 0s.

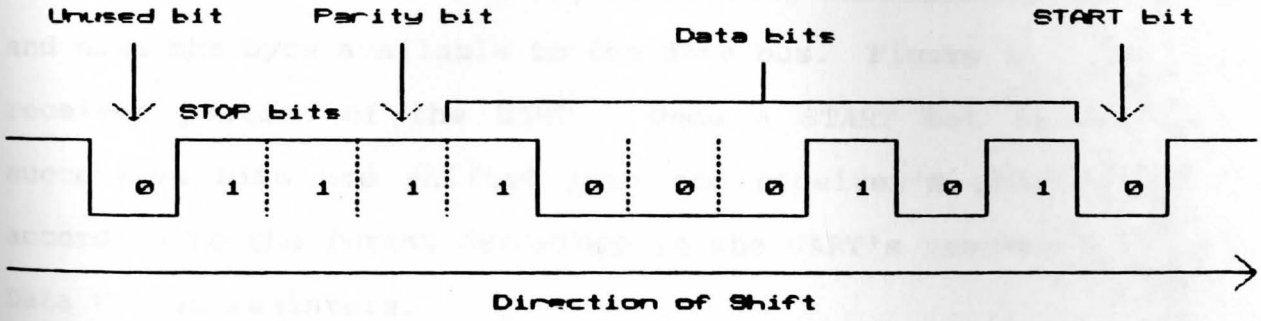


FIGURE 18. SDU for the Letter E

D.2.2 Transmitter Status

Only two items of information about the transmitter are needed to transmit data: whether or not the Transmitter Buffer is empty and whether or not the transmitter's shift register is empty.

Each of these conditions is reported through a bit in a Serialization Status register. When the data from the buffer is loaded into the transmitter, a Transmitter Buffer Empty (TBE) flag signals that the UART can accept another byte. If TBE is clear after the final bit of the SDU is clocked from the transmitter's shift register, the Transmitter Empty flag (TXE) signals that the shift register is also empty.

D.3 The UART's Receiver

A received byte is acquired by reading the address of the UART's receiver section, whose job is to construct an SDU from bits fetched from the serial input line. The UART must then extract the data byte from the surrounding formatting information in the SDU and make the byte available to the data bus. Figure 19[11] shows the receiver portion of the UART. Once a START bit is detected, successive bits are shifted into the receiver's shift register according to the format described in the UART's user-programmable Data Format registers.

---

[11]Joe Campbell, C Programmer's Guide To Serial Communications, Howard W. Sams and Company, 1988, p.160

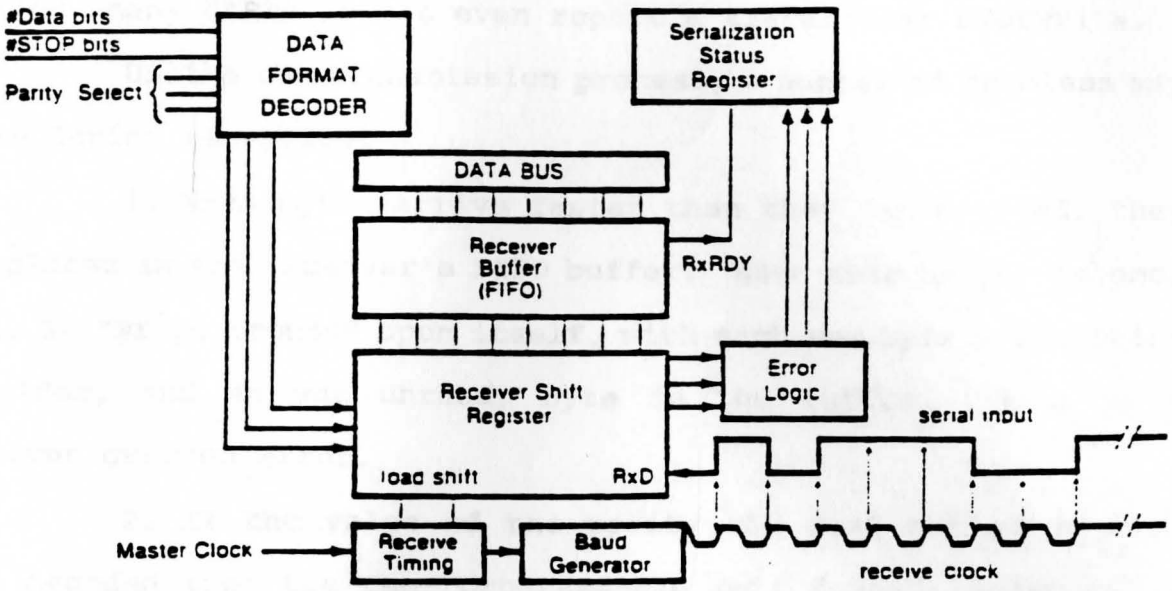


FIGURE 19. UART Receiver Functions

D.3.1 Receiver Status

When a byte has been moved into the receiver's Receiver Buffer, the RxRDY flag is set TRUE and remains TRUE until all elements of the buffer are empty. For every element in the buffer, there is a corresponding Serialization Status register.

D.3.2 Errors

Errors are possible in the transmission process. Writing

into a nonempty transmitter buffer results in a transmitter overwrite error. Under the assumption that this error is easily avoided, many UARTs do not even report a transmitter overwrite.

Unlike the transmission process, a number of problems may arise during reception.

1. When bytes arrive faster than they can be read, they are placed in the receiver's FIFO buffer. When this buffer becomes full, it "wraps around" upon itself, with each new byte overwriting an older, and as yet unread, byte in the buffer. This is a receiver overrun error.

2. If the value of the parity bit does not agree with that decoded from the user programmable Data Format registers, a parity error is reported.

3. If an invalid STOP bit is received, and if all data bits and the parity bit are 0, the serial line is assumed to have been FALSE for a time equal to one SDU, and a BREAK is reported.

4. If an invalid STOP bit is received, the UART checks if the SDU contains at least one TRUE data bit. If so, either the START bit was invalid, or succeeding bits were damaged during transmission. Since it is not possible to determine the nature of the error more precisely, the catchall framing error is reported.

All of the receiver errors just described assume that the transmitter and receiver are operating at identical baud rates and data format. A mismatch in either always generates an error. Each error or flag is mapped to a single bit in the status register. These errors can be detected by the programmer by reading the

register.

D.3.3 Receiver Timing

As discussed earlier, the purpose of the START bit is to synchronize the receiver with the transmitter at the beginning of each SDU. Until now, this synchronization, in which the receiver and transmitter operate at identical baud rates, has been assumed under ideal conditions. When the periods of the two baud rates are identical, the point at which the receiver samples the incoming data is theoretically unimportant. But since this never happens in practice, the UARTs receiver takes certain precautions to ensure that the data is indeed being sampled as close to the center of each bit as possible.

The UART requires that the frequency of the clock be much greater than that of the baud rate. A factor of 16 is typical. This enables the UART to sample data bits in an optimum way. Instead of sampling the input line at the baud rate frequency, the START bit detector samples the incoming line 16 times faster. When the leading edge of a START bit is detected, the START bit detector counts for 8 data clock cycles (one-half a bit time), then samples the bit again. If the line is still indicating a SPACE (middle of the START bit), then this it is indeed a START bit and not just noise on the line. It then begins reading bits from the line every 16 clock cycles (one full bit time). This will place the sample time as close to the middle of each following bit as possible.

Figure 20 shows a typical sampling sequence.

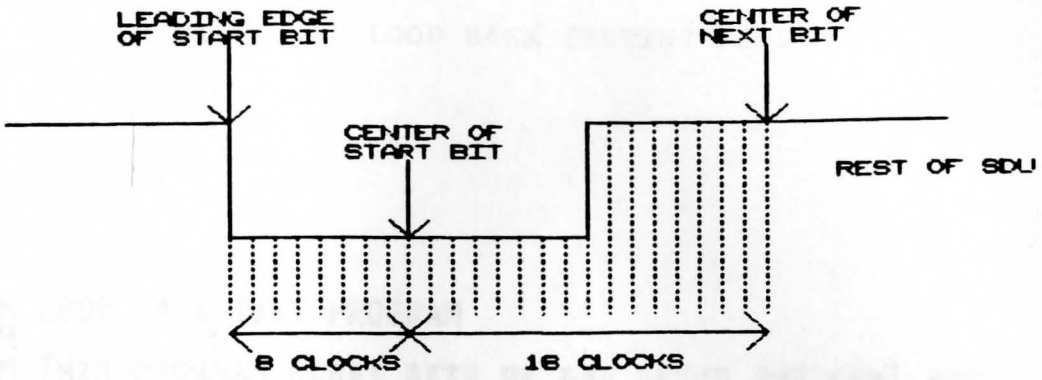


FIGURE 20. Receiver Sampling Sequence

APPENDIX E

SINGLE PC LOOP BACK TESTING PROGRAM

```
10 REM LOOP BACK TEST PROGRAM
20 REM
30 REM THIS PROGRAM FIRST SETS UP AND OPENS THE COM1 PORT.
40 REM NEXT IT ENTERS AN INFINITE LOOP THAT OUTPUTS AN A.
50 REM FINALLY IT PRINTS THE RECEIVED LETTER AND LOOPS FOREVER.
55 REM
60 OPEN "COM1:300,N,8,1,RS,DS" AS #1
70 X=1
80 WHILE X
90 PRINT #1,"A"
100 INPUT #1,Y$
110 PRINT Y$
120 WEND
130 END
```

APPENDIX F

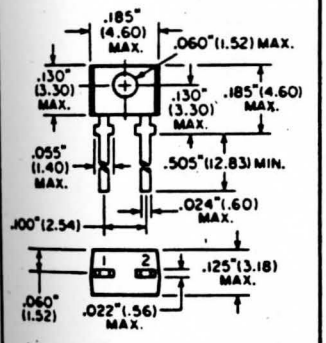
SPECIFICATION OF CHIPS USED IN THE CIRCUITS

Phototransistor Detectors

ECG Type	Description	Collector to Base Voltage BVCBO (V)	Max Collector Current I_C (mA)	Max Dark Current I_D at 25°C (nA)	Min Light Current I_L (mA)	Max Power Dissipation at 25°C P_t (mW)	Rise Time t_r (μS)	Fig. No.
ECG3031	NPN, Si, Visible and IR	80	40	20 at VCE 5V	6	200	2 Typ	P19
ECG3032	NPN, Si, Visible and IR	80	40	20 at VCE 5V	12	200	2 Typ	P20
ECG3034	NPN, Si, Visible and IR	60	100	100 at VCE 10V	2	200	—	P21
ECG3035A	NPN, Si-Darlington Amp h_{fe} = 2.0 K, Visible and IR	60	100	100 at VCE 10V	5	150	75	P18A
ECG3036	NPN, Si-Darlington, Visible and IR	40	250	100 at VCE 10V	12	250	40 Typ	P22
ECG3037	NPN, Si, Visible and IR	50	50	500 at VCE 30V	10	150	2 Typ	P23
ECG3038	NPN, Si-Darlington, Visible and IR	25	20	20 at VCE 10V	5	50	1.5 Typ	P24
ECG3120	NPN, Si, Visible and IR	20 (VCEO)	20	500 at VCE 10V	1	100	10 Max	P52
ECG3121	NPN, Si, Darlington Visible and IR	20 (VCEO)	30	500 at VCE 10V	.5	100	100 Typ	P52

Phototransistor Detector Outlines

Fig. P18A
ECG3035A



PIN 1. EMITTER
2. COLLECTOR

Fig. P19
ECG3031

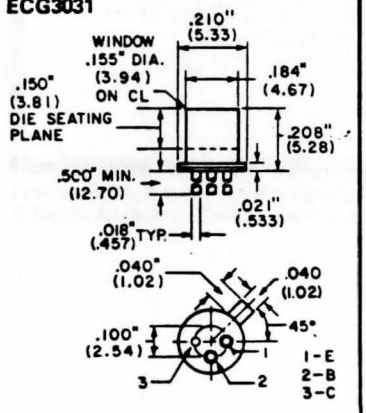


Fig. P20
ECG3032

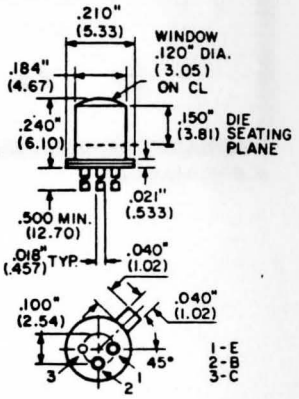
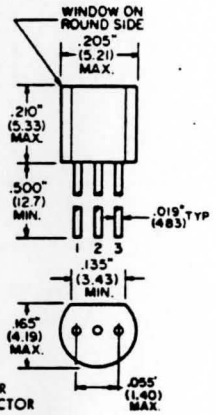


Fig. P21
ECG3034



PIN 1. EMITTER
2. COLLECTOR
3. BASE

Fig. P22
ECG3036

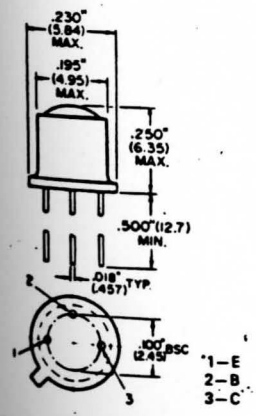
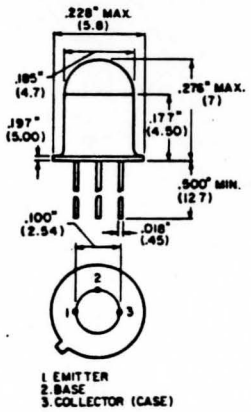
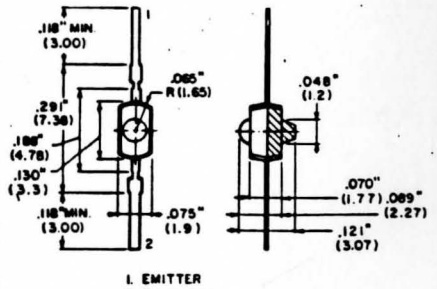


Fig. P23
ECG3037



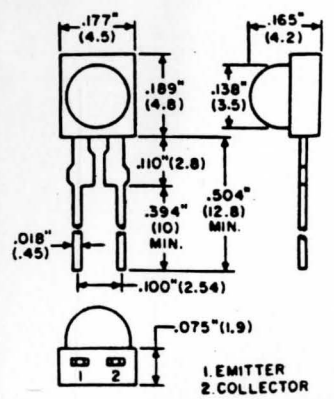
1. EMITTER
2. BASE
3. COLLECTOR (CASE)

Fig. P24
ECG3038

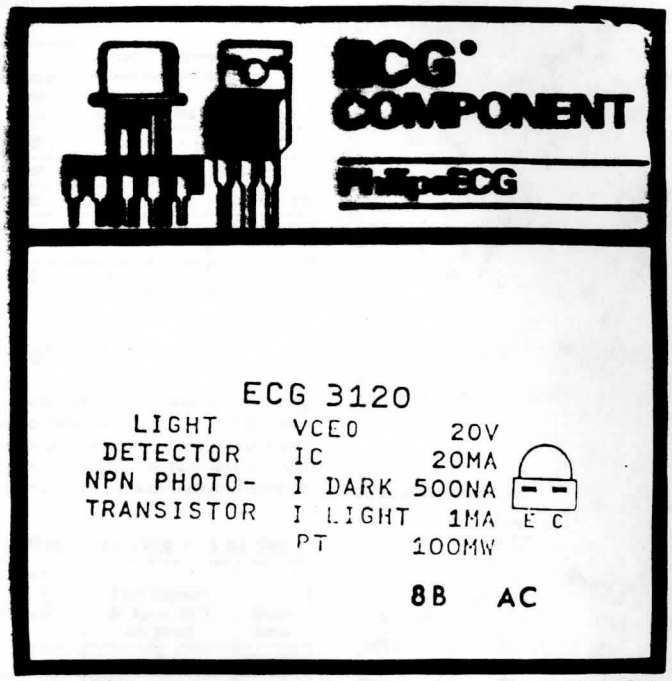


1. EMITTER
2. COLLECTOR

Fig. P52
ECG3120
ECG3121



1. EMITTER
2. COLLECTOR



Philips ECG, Inc. Waltham, MA 02254
A North American Philips Company
Printed in U.S.A.

Emitters/Detectors

Infrared Emitting Diodes

Motorola's infrared emitting diodes are made by the liquid phase epitaxial process for long life and stability. They provide high power output and quick response at 660 nm, 850 nm or 940 nm with low input drive current.

Device	Power Output μW @ I_F Typ	mA	Emission Angle Typ	Peak Emission Wavelength nm Typ	Forward Voltage @ I_F Max	mA	Case/ Style
MLED71	2500	50	60°	940	1.8	50	349-03/1
MLED76	4000	100	60°	660	2.2	60	349-03/4
MLED77	2500	100	60°	850	2	100	349-03/4
MLED81	16000	100	60°	940	1.7	100	279B-01/1
MLED930	650	100	30°	940	1.5	50	209-01/1

Silicon Photodetectors

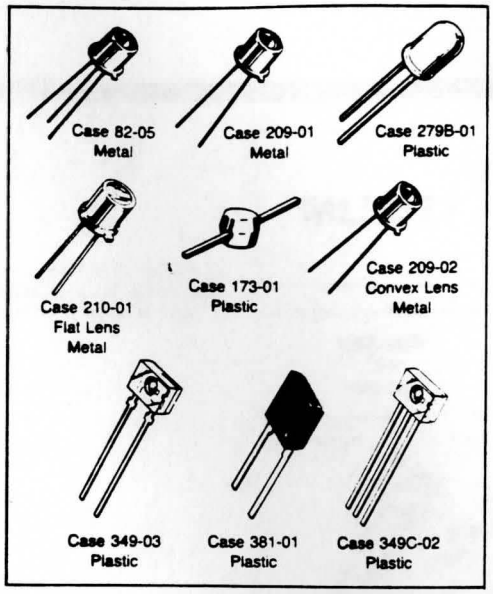
A variety of silicon photodetectors are available, varying from simple PIN diodes to complex, single chip 400 volt triac drivers. They offer choices of viewing angle and size in either economical plastic cases or rugged, hermetic metal cans. They are spectrally matched for use with Motorola infrared emitting diodes.

PIN Photodiodes — Response Time = 1 ns Typ

Device	Light Current @ V_R = 20 V, H = 5 mW/cm² μA	Dark Current @ V_R = 20 V nA (Max)	Case/ Style
MRD500	9	2	209-02/1
MRD510	2	2	210-01/1
MRD721	4	10	349-03/1
MRD821	250	60	381-01/1

Phototransistors

Device	Light Current @V_{CC} = 20, H = 5 mW/cm² mA (Typ)	$V_{(BR)CEO}$ Volts (Min)	t_r/t_f @V_{CC} = 20, I_L = 1000 μA μs (Typ)	Case/ Style
MRD150	2.2	40	2.5/4	173-01/1
MRD310	3.5	50	2/2.5	82-05/1
MRD300	8	50	2/2.5	
MRD3050	0.1 Min	30	2/2.5	
MRD3051	0.2 Min	30	2/2.5	
MRD3054	0.5 Min	30	2/2.5	
MRD3055	1.5 Min	30	2/2.5	
MRD3056	2 Min	30	2/2.5	
			t_{on}/t_{off} @V_{CC} = 5 V	
MRD701	0.5	30	10/60	349-03/2



Photodarlingtons

Device	Light Current @ V_{CC} = 5, H = 0.5 mW/cm² mA (Typ)	$V_{(BR)CEO}$ Volts (Min)	t_r/t_f @V_{CC} = 5 V μs (Typ)	Case/ Style
MRD370	10	40	15/40	82-05/1
MRD360	20	40	15/65	
MRD711	25	60	125/150	349-03/2

Photothyristors — Triac Drivers

Device	H_{FT} mW/cm² Max	$I_{T(RMS)}$ mA Max	V_{DRM} Volts Peak Min	I_{DRM} nA Typ	Case/ Style
MRD3010	5	100	250	10	82-05/3
MRD3011	2	100	250	10	

Photo Schmitt Trigger

Device	Threshold Current mA ON Max	OFF Min	$I_{F(off)}/I_{F(on)}$ Typ	V_{CC} Volts	t_r/t_f μs Typ	Case/Style
MRD750	20	1.0	0.75	3–15	0.1	349C-02/3
MRD5009	20	1.0	0.75	3–15	0.1	82-05/1

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

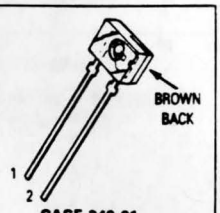
Infrared LED

MLED71

This device is designed for a wide variety of infrared applications, including keyboards, end-of-tape sensors, coin or paper handlers, and other general sensing applications. The MLED71 can be used in conjunction with any MRD700 series detector. It features high power output, using gallium arsenide technology.

- Low Cost
- Popular Case 349 Package, with Molded Lens
- Uses Stable Long-Life LED Technology
- Clear Epoxy Package

INFRARED LED 940 nm



CASE 349-01 PLASTIC

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Reverse Voltage	V_R	6	Volts
Forward Current — Continuous	I_F	60	mA
Forward Current — Peak Pulse	I_F	1	A
Total Power Dissipation @ T_A = 25°C (Note 1) Derate above 55°C	P_D	90 2	mW mW/°C
Ambient Operating Temperature Range	T_A	−40 to +100	°C
Storage Temperature	T_{stg}	−40 to − 100	°C
Lead Soldering Temperature (Note 2)	—	260	°C

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Reverse Leakage Current (V_R = 6 V)	I_R	—	0.05	100	μA
Forward Voltage (I_F = 60 mA)	V_F	—	1.3	1.5	V
Temperature Coefficient of Forward Voltage	ΔV_F	—	−1.6	—	mV/K
Capacitance (V = 0 V, f = 1 MHz)	C	—	18	—	pF

OPTICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Peak Wavelength (I_F = 60 mA)	λ_P	—	940	—	nm
Spectral Half-Power Bandwidth	$\Delta\lambda$	—	48	—	nm
Continuous Power Output (I_F = 50 mA) (Note 3)	P_O	2	2.5	—	mW
Instantaneous Power Output (I_F = 100 mA)	P_O	—	5	—	mW
Instantaneous Axial Intensity (I_F = 100 mA) (Note 4)	I_O	—	3.5	—	mW/sr
Power Half-Angle	θ	—	±30	—	°
Optical Turn-On and Turn-Off Times	t_{on}, t_{off}	—	1	—	μs

Notes: 1. Measured with device soldered into a typical printed circuit board.
2. 5 seconds max; 1/16 inch from case. Heat sink should be applied during soldering, to prevent case temperature from exceeding 100°C.
3. Measured using a Photodyne 88xLA with a #350 integrating sphere.
4. On 0° axis, with cone angle of ± 13°.

MLED71

TYPICAL CHARACTERISTICS

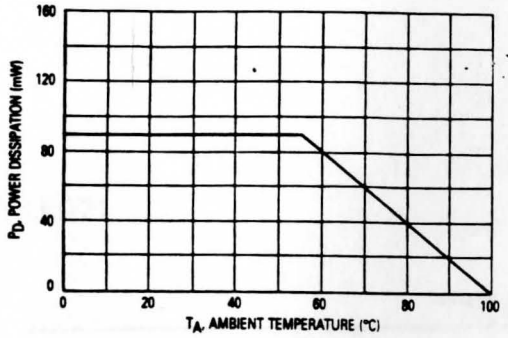


Figure 1. Power Dissipation

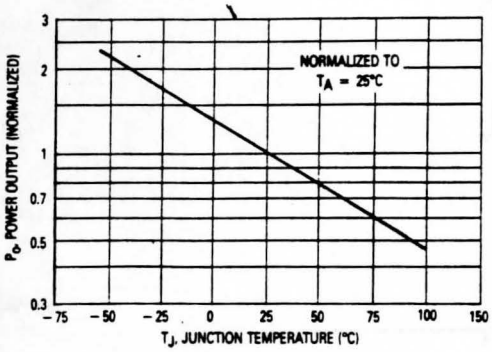


Figure 2. Instantaneous Power Output versus Ambient Temperature

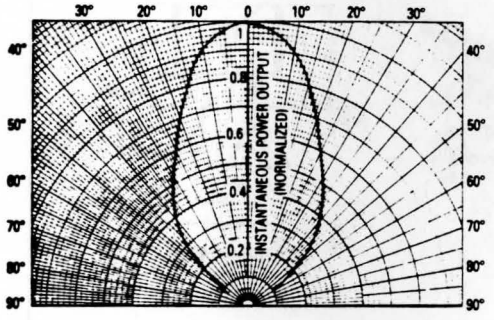


Figure 3. Spatial Radiation Pattern

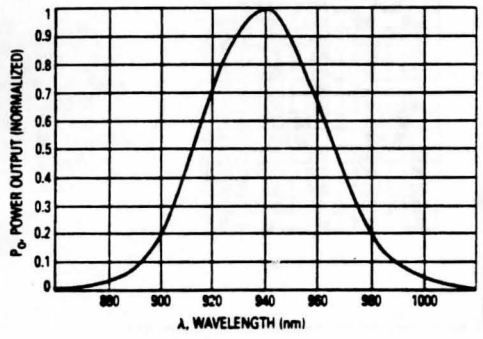


Figure 4. Relative Spectral Output

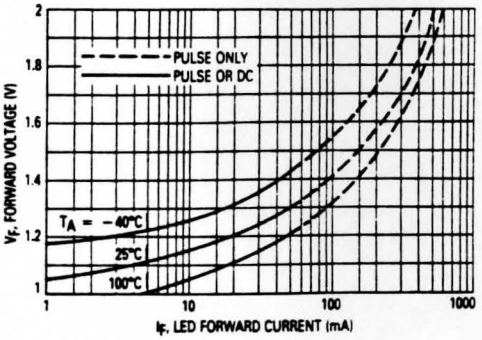


Figure 5. Forward Voltage versus Forward Current

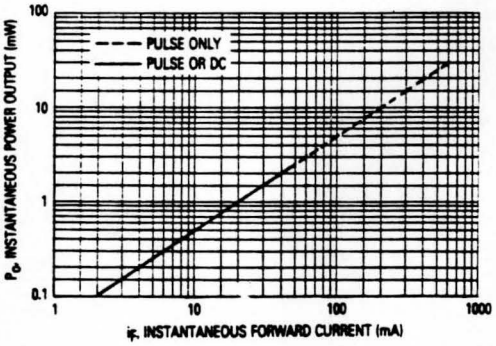
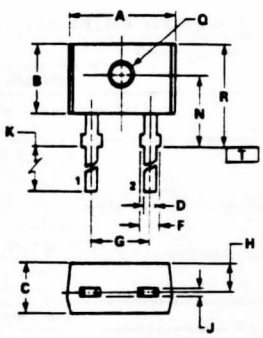


Figure 6. Instantaneous Power Output versus Forward Current

MLED71

OUTLINE DIMENSIONS

CASE 349-01
PLASTIC



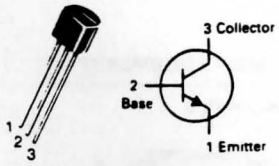
NOTES:
1. DIMENSIONS A, B AND C ARE DATUMS.
2. POSITIONAL TOLERANCE FOR D DIMENSION:
   ⌖ | 0.25 (0.010) Ⓜ | -T- | A Ⓜ | C Ⓜ |
3. POSITIONAL TOLERANCE FOR Q DIAMETER:
   ⌖ | 0.25 (0.010) Ⓜ | A Ⓜ | B Ⓜ |
4. -T- IS SEATING PLANE.
5. DIMENSIONING AND TOLERANCING PER ANSI Y14.5, 1973.

STYLE 1:
PIN 1. CATHODE
2. ANODE

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	3.43	4.80	0.135	0.185
B	2.79	3.30	0.110	0.130
C	2.03	3.18	0.080	0.125
D	0.43	0.60	0.017	0.024
F	1.14	1.40	0.045	0.055
G	2.54 BSC		0.100 BSC	
H	1.52 BSC		0.060 BSC	
J	0.23	0.56	0.009	0.022
K	12.83	19.05	0.505	0.750
N	3.05	3.30	0.120	0.130
Q	0.76	1.52	0.030	0.060
R	3.81	4.80	0.150	0.185

MPS5172

CASE 29-04, STYLE 1
TO-92 (TO-226AA)



AMPLIFIER TRANSISTOR

NPN SILICON

Refer to MPS3903 for graphs.

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	25	Vdc
Collector-Base Voltage	V_{CBO}	25	Vdc
Emitter-Base Voltage	V_{EBO}	5.0	Vdc
Collector Current — Continuous	I_C	100	mAdc
Total Device Dissipation @ T_A = 25°C Derate above 25°C	P_D	625 5.0	mW mW/°C
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	1.5 12	Watts mW/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−55 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	83.3	°C/W
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	200	°C/W

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Breakdown Voltage (I_C = 10 mAdc, I_B = 0)	$V_{(BR)CEO}$	25	—	—	Vdc
Collector Cutoff Current (V_{CB} = 25 Vdc, I_E = 0) (V_{CB} = 25 Vdc, I_E = 0, T_A = 100°C)	I_{CBO}	— —	— —	100 10	nAdc μAdc
Collector Cutoff Current (V_{CE} = 25 Vdc, V_{BE} = 0)	I_{CES}	—	—	100	nAdc
Emitter Cutoff Current (V_{BE} = 5.0 Vdc, I_C = 0)	I_{EBO}	—	—	100	nAdc
ON CHARACTERISTICS					
DC Current Gain(1) (I_C = 10 mAdc, V_{CE} = 10 Vdc)	h_{FE}	100	—	500	—
Collector-Emitter Saturation Voltage (I_C = 10 mAdc, I_B = 1.0 mAdc)	$V_{CE(sat)}$	—	—	0.25	Vdc
Base-Emitter Saturation Voltage (I_C = 10 mAdc, I_B = 1.0 mAdc)	$V_{BE(sat)}$	—	0.75	—	Vdc
Base-Emitter On Voltage (I_C = 10 mAdc, V_{CE} = 10 Vdc)	$V_{BE(on)}$	0.5	—	1.2	Vdc
SMALL SIGNAL CHARACTERISTICS					
Current-Gain — Bandwidth Product (I_C = 2.0 mAdc, V_{CE} = 5.0 Vdc)	f_T	—	120	—	MHz
Collector-Base Capacitance (V_{CB} = 0, I_E = 0, f = 1.0 MHz)	C_{cb}	1.6	—	10	pF
Small Signal Current Gain (I_C = 10 mAdc, V_{CE} = 10 Vdc, f = 1.0 kHz)	h_{fe}	100	—	750	—

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

Signetics

MC1488
Quad Line Driver

Product Specification

Linear Products

DESCRIPTION

The MC1488 is a quad line driver which converts standard DTL/TTL input logic levels through one stage of inversion to output levels which meet EIA Standard No. RS-232C and CCITT Recommendation V.24.

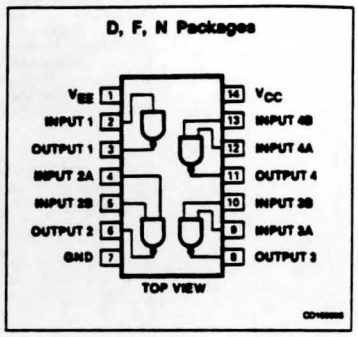
FEATURES

- Current limited output: ± 10mA Typ
- Power-off source impedance: 300Ω min
- Simple slew rate control with external capacitor
- Flexible operating supply range
- Inputs are DTL/TTL compatible

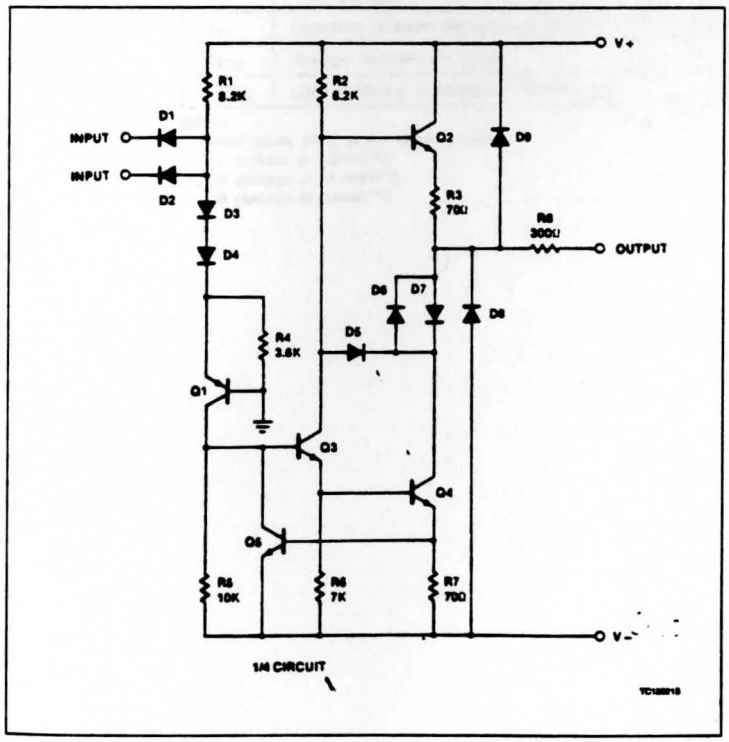
APPLICATIONS

- Computer port driver
- Digital transmission over long lines
- Slew rate control
- TTL/DTL to MOS translation

PIN CONFIGURATION



CIRCUIT SCHEMATIC



Quad Line Driver

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
14-Pin Plastic SO	0 to +75°C	MC1488D
14-Pin Plastic DIP	0 to +75°C	MC1488N
14-Pin Ceramic DIP	0 to +75°C	MC1488F

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage V+	+15	V
	V–	–15	V
V_{IN}	Input voltage	$-15 \leq V_{IN} \leq 7.0$	V
V_{OUT}	Output voltage	±15	V
P_D	Maximum power dissipation, T_A = 25°C (still-air)[1] F package N package D package	 1190 1420 1040	 mW mW mW
T_A	Operating ambient temperature range	0 to +75	°C
T_{STG}	Storage temperature range	–65 to +150	°C
T_{SOLD}	Lead soldering temperature (10sec max)	300	°C

NOTE:

1. Derate above 25°C, at the following rates:
   F package at 9.5mW/°C.
   N package at 11.4mW/°C.
   D package at 8.3mW/°C.

DC AND AC ELECTRICAL CHARACTERISTICS $V+ = +9.0V \pm 1\%$, $V- = -9.0V \pm 1\%$, $T_A = 0°C$ to $+75°C$, unless otherwise specified. All typicals are for $V+ = 9.0V$, $V- = -9.0V$, and $T_A = 25°C$[1].

SYMBOL	PARAMETER	TEST CONDITIONS		LIMITS			UNIT
				Min	Typ	Max	
V_{IH} V_{IL}	Logic "0" input current Logic "1" input current	$V_{IN} = 0V$ $V_{IN} = +5.0V$			-1.0 0.005	-1.6 10.0	mA μA
V_{OH}	High level output voltage	$R_L = 3.0k\Omega$ $V_{IN} = 0.8V$	$V+ = 9.0V$ $V- = -9.0V$	6.0	7.0		V
			$V+ = 13.2V$ $V- = -13.2V$	9.0	10.5		V
V_{OL}	Low level output voltage	$R_L = 3.0k\Omega$ $V_{IN} = 1.9V$	$V+ = 9.0V$ $V- = -9.0V$	-6.0	-6.8		V
			$V+ = 13.2V$ $V- = -13.2V$	-9.0	-10.5		V
I_{SC+}	High level output short-circuit current	$V_{OUT} = 0V$ $V_{IN} = 0.8V$		-6.0	-10.0	-12.0	mA
I_{SC-}	Low level output short-circuit current	$V_{OUT} = 0V$ $V_{IN} = 1.9V$		5.0	10.0	12.0	mA
R_{OUT}	Output resistance	$V+ = V- = 0V$ $V_{OUT} = \pm 2V$		300			Ω
$I+$	Positive supply current (output open)	$V_{IN} = 1.9V$	$V+ = 9.0V, V- = -9.0V$ $V+ = 12V, V- = -12V$ $V+ = 15V, V- = -15V$		15.0 19.0 25.0	20.0 25.0 34.0	mA mA mA
		$V_{IN} = 0.8V$	$V+ = 9.0V, V- = -9.0V$ $V+ = 12V, V- = -12V$ $V+ = 15V, V- = -15V$		4.5 5.5 8.0	6.0 7.0 12.0	mA mA mA
$I-$	Negative supply current (output open)	$V_{IN} = 1.9V$	$V+ = 9.0V, V- = -9.0V$ $V+ = 12V, V- = -12V$ $V+ = 15V, V- = -15V$		-13.0 -18.0 -25.0	-17.0 -23.0 -34.0	mA mA mA
		$V_{IN} = 0.8V$	$V+ = 9.0V, V- = -9.0V$ $V+ = 12V, V- = -12V$ $V+ = 15V, V- = -15V$		-1 -1 -0.01	-15 -15 -2.5	μA μA mA
P_D	Maximum power dissipation, $T_A = 25°C$ (still-air)[2] F package N package D package					1190 1420 1040	mW mW mW
t_{PD1}	Propagation delay to "1"	$R_L = 3.0k\Omega$, $C_L = 15pF$, $T_A = 25°C$			275	560	ns
t_{PD0}	Propagation delay to "0"	$R_L = 3.0k\Omega$, $C_L = 15pF$, $T_A = 25°C$			70	175	ns
t_R	Rise time	$R_L = 3.0k\Omega$, $C_L = 15pF$, $T_A = 25°C$			75	100	ns
t_F	Fall time	$R_L = 3.0k\Omega$, $C_L = 15pF$, $T_A = 25°C$			40	75	ns

NOTES:

1. Voltage values shown are with respect to network ground terminal. Positive current is defined as current into the referenced pin.
2. Derate above 25°C, at the following rates:
   F package at 9.5mW/°C.
   N package at 11.4mW/°C.
   D package at 8.3mW/°C.

Signetics

MC1489/MC1489A
Quad Line Receivers

Product Specification

Linear Products

DESCRIPTION

The MC1489/MC1489A are quad line receivers designed to interface data terminal equipment with data communications equipment. They are constructed on a single monolithic silicon chip. These devices satisfy the specifications of EIA standard No. RS-232C.

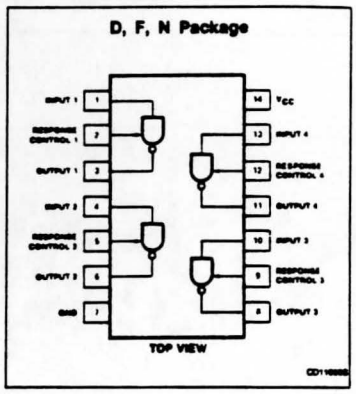
FEATURES

- Four totally separate receivers per package
- Programmable threshold
- Built-in input threshold hysteresis
- "Fail safe" operating mode
- Inputs withstand ±30V

APPLICATIONS

- Computer port inputs
- Modems
- Eliminating noise in digital circuitry
- MOS-to-TTL/DTL translation

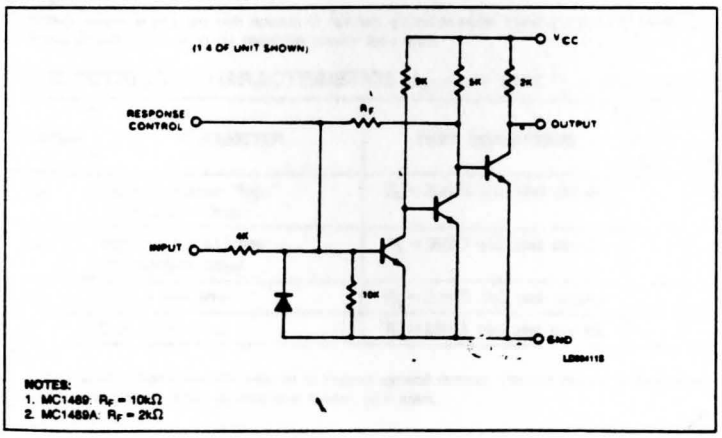
PIN CONFIGURATION



ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
14-Pin Plastic DIP	0 to +70°C	MC1489N
14-Pin Plastic DIP	0 to +70°C	MC1489AN
14-Pin Cerdip	0 to +70°C	MC1489F
14-Pin Cerdip	0 to +70°C	MC1489AF
14-Pin Plastic SO	0 to +70°C	MC1489D
14-Pin Plastic SO	0 to +70°C	MC1489AD

EQUIVALENT SCHEMATIC

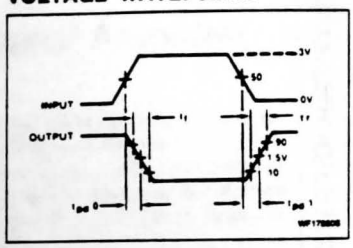


ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Power supply voltage	10	V
V_{IN}	Input voltage range	±30	V
I_{OUT}	Output load current	20	mA
P_D	Maximum power dissipation, T_A = 25°C (still-air)[1]		
	F package	1190	mW
	N package	1420	mW
	D package	1040	mW
T_A	Operating temperature range	0 to +75	°C
T_{STG}	Storage temperature range	−65 to +150	°C

NOTE:
1. Derate above 25°C, at the following rates:
   F package at 9.5mW/°C
   N package at 11.4mW/°C
   D package at 8.3mW/°C

VOLTAGE WAVEFORMS



DC ELECTRICAL CHARACTERISTICS V_{CC} = 5.0V ±1%, 0°C ≤ T_A ≤ +75°C, unless otherwise specified.[1, 2]

SYMBOL	PARAMETER	TEST CONDITIONS	MC1489			MC1489A			UNIT
			Min	Typ	Max	Min	Typ	Max	
V_{IH}	Input high threshold voltage	T_A = 25°C, V_{OUT} ≤ 0.45V, I_{OUT} = 10mA	1.0		1.5	1.75		2.25	V
V_{IL}	Input low threshold voltage	T_A = 25°C, V_{OUT} ≥ 2.5V, I_{OUT} = −0.5mA	0.75		1.25	0.75		1.25	V
I_{IN}	Input current	V_{IN} = +25V V_{IN} = −25V V_{IN} = +3V V_{IN} = −3V	+3.6 −3.6 +0.43 −0.43	+5.6 −5.6 +0.53 −0.53	+8.3 −8.3	+3.6 −3.6 +0.43 −0.43	+5.6 −5.6 +0.53 −0.53	+8.3 −8.3	mA
V_{OH}	Output high voltage	V_{IN} = 0.75V, I_{OUT} = −0.5mA	2.6	3.8	5.0	2.6	3.8	5.0	V
		Input = Open, I_{OUT} = −0.5mA	2.6	3.8	5.0	2.6	3.8	5.0	V
V_{OL}	Output low voltage	V_{IN} = 3.0V, I_{OUT} = 10mA		0.33	0.45		0.33	0.45	V
I_{CC}	Output short-circuit current	V_{IN} = 0.75V		3.0			3.0		mA
	Supply current	V_{IN} = 5.0V		20	26		20	26	mA
P_D	Power dissipation	V_{IN} = 5.0V		100	130		100	130	mW

NOTES:
1. Voltage values shown are with respect to network ground terminal. Positive current is defined as current into the referenced pin.
2. These specifications apply for response control pin = open.

AC ELECTRICAL CHARACTERISTICS V_{CC} = 5.0V ±1%, T_A = 25°C, unless otherwise specified.[1, 2]

SYMBOL	PARAMETER	TEST CONDITIONS	MC1489			MC1489A			UNIT
			Min	Typ	Max	Min	Typ	Max	
t_{PD1}	Input to output "high" Propagation delay	R_L = 3.9kΩ (AC test circuit)		25	85		25	85	ns
t_{PD0}	Input to output "low" Propagation delay	R_L = 390Ω (AC test circuit)		20	50		20	50	ns
t_R	Output rise time	R_L = 3.9kΩ (AC test circuit)		110	175		110	175	ns
t_F	Output fall time	R_L = 390Ω (AC test circuit)		9	20		9	20	ns

NOTES:
1. Voltage values shown are with respect to network ground terminal. Positive current is defined as current into the referenced pin.
2. These specifications apply for response control pin = open.

National Semiconductor Corporation

LM741/LM741A/LM741C/LM741E Operational Amplifier

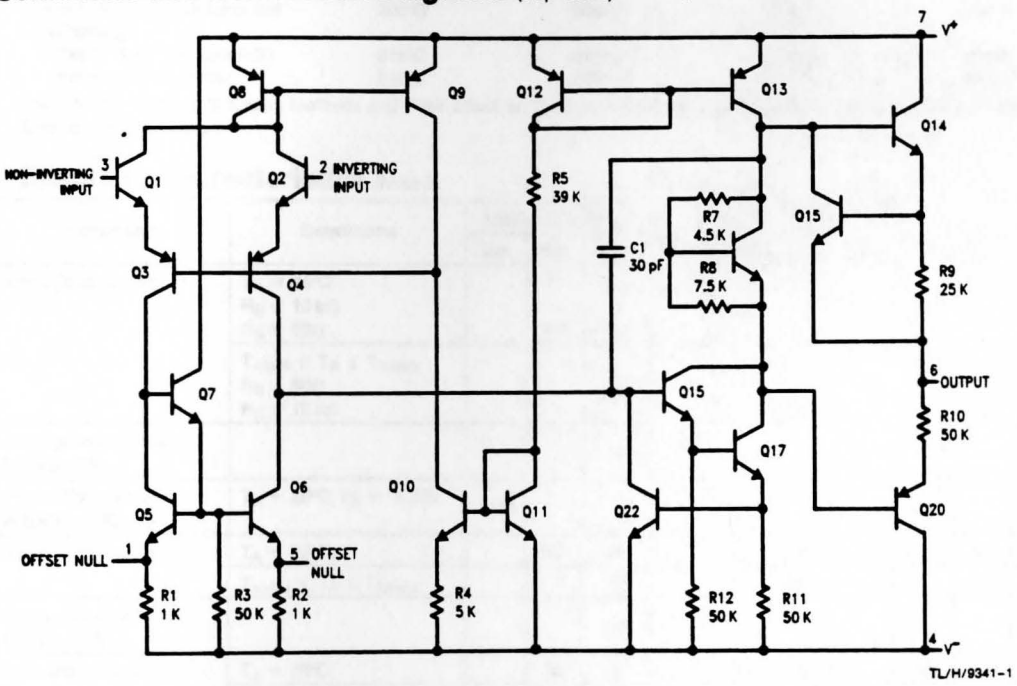
General Description

The LM741 series are general purpose operational amplifiers which feature improved performance over industry standards like the LM709. They are direct, plug-in replacements for the 709C, LM201, MC1439 and 748 in most applications.

The amplifiers offer many features which make their application nearly foolproof: overload protection on the input and output, no latch-up when the common mode range is exceeded, as well as freedom from oscillations.

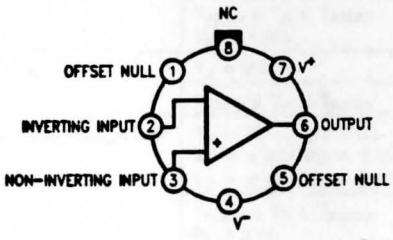
The LM741C/LM741E are identical to the LM741/LM741A except that the LM741C/LM741E have their performance guaranteed over a 0°C to +70°C temperature range, instead of −55°C to +125°C.

Schematic and Connection Diagrams (Top Views)



TL/H/9341-1

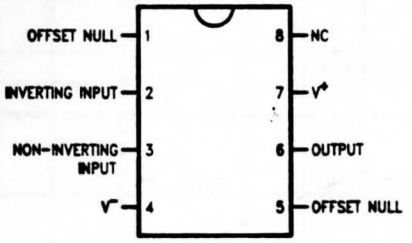
Metal Can Package



TL/H/9341-2

Order Number LM741H, LM741AH, LM741CH or LM741EH
See NS Package Number H08C

Dual-In-Line or S.O. Package



TL/H/9341-3

Order Number LM741CJ, LM741CM, LM741CN or LM741EN
See NS Package Number J08A, M08A or N08E

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/Distributors for availability and specifications.
(Note 5)

	LM741A	LM741E	LM741	LM741C
Supply Voltage	±22V	±22V	±22V	±18V
Power Dissipation (Note 1)	500 mW	500 mW	500 mW	500 mW
Differential Input Voltage	±30V	±30V	±30V	±30V
Input Voltage (Note 2)	±15V	±15V	±15V	±15V
Output Short Circuit Duration	Indefinite	Indefinite	Indefinite	Indefinite
Operating Temperature Range	−55°C to +125°C	0°C to +70°C	−55°C to +125°C	0°C to +70°C
Storage Temperature Range	−65°C to +150°C	−65°C to +150°C	−65°C to +150°C	−65°C to +150°C
Junction Temperature	150°C	100°C	150°C	100°C
Soldering Information				
N-Package (10 seconds)	260°C	260°C	260°C	260°C
J- or H-Package (10 seconds)	300°C	300°C	300°C	300°C
M-Package				
Vapor Phase (60 seconds)	215°C	215°C	215°C	215°C
Infrared (15 seconds)	215°C	215°C	215°C	215°C

See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" (Appendix D) for other methods of soldering surface mount devices.

Electrical Characteristics (Note 3)

Parameter	Conditions	LM741A/LM741E			LM741			LM741C			Units
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage	T_A = 25°C $R_S \le 10\ k\Omega$ $R_S \le 50\Omega$		 0.8	 3.0		1.0	5.0		2.0	6.0	mV mV
	$T_{AMIN} \le T_A \le T_{AMAX}$ $R_S \le 50\Omega$ $R_S \le 10\ k\Omega$			4.0			 6.0			 7.5	mV mV
Average Input Offset Voltage Drift				15							µV/°C
Input Offset Voltage Adjustment Range	T_A = 25°C, V_S = ±20V	±10				±15			±15		mV
Input Offset Current	T_A = 25°C		3.0	30		20	200		20	200	nA
	$T_{AMIN} \le T_A \le T_{AMAX}$			70		85	500			300	nA
Average Input Offset Current Drift				0.5							nA/°C
Input Bias Current	T_A = 25°C		30	80		80	500		80	500	nA
	$T_{AMIN} \le T_A \le T_{AMAX}$			0.210			1.5			0.8	µA
Input Resistance	T_A = 25°C, V_S = ±20V	1.0	6.0		0.3	2.0		0.3	2.0		MΩ
	$T_{AMIN} \le T_A \le T_{AMAX}$, V_S = ±20V	0.5									MΩ
Input Voltage Range	T_A = 25°C							±12	±13		V
	$T_{AMIN} \le T_A \le T_{AMAX}$				±12	±13					V
Large Signal Voltage Gain	T_A = 25°C, $R_L \ge 2\ k\Omega$ V_S = ±20V, V_O = ±15V V_S = ±15V, V_O = ±10V	50			 50	 200		 20	 200		V/mV V/mV
	$T_{AMIN} \le T_A \le T_{AMAX}$, $R_L \ge 2\ k\Omega$, V_S = ±20V, V_O = ±15V V_S = ±15V, V_O = ±10V V_S = ±5V, V_O = ±2V	 32 10			 25			 15			 V/mV V/mV V/mV

Electrical Characteristics (Note 3) (Continued)

Parameter	Conditions	LM741A/LM741E			LM741			LM741C			Units
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Output Voltage Swing	$V_S = \pm 20V$										
	$R_L \geq 10\ k\Omega$	±16									V
	$R_L \geq 2\ k\Omega$	±15									V
	$V_S = \pm 15V$										
	$R_L \geq 10\ k\Omega$				±12	±14		±12	±14		V
	$R_L \geq 2\ k\Omega$				±10	±13		±10	±13		V
Output Short Circuit Current	$T_A = 25°C$	10	25	35		25			25		mA
	$T_{AMIN} \leq T_A \leq T_{AMAX}$	10		40							mA
Common-Mode Rejection Ratio	$T_{AMIN} \leq T_A \leq T_{AMAX}$										
	$R_S \leq 10\ k\Omega$, $V_{CM} = \pm 12V$				70	90		70	90		dB
	$R_S \leq 50\ k\Omega$, $V_{CM} = \pm 12V$	80	95								dB
Supply Voltage Rejection Ratio	$T_{AMIN} \leq T_A \leq T_{AMAX}$, $V_S = \pm 20V$ to $V_S = \pm 5V$										
	$R_S \leq 50\Omega$	86	96								dB
	$R_S \leq 10\ k\Omega$				77	96		77	96		dB
Transient Response	$T_A = 25°C$, Unity Gain										
Rise Time			0.25	0.8		0.3			0.3		µs
Overshoot			6.0	20		5			5		%
Bandwidth (Note 4)	$T_A = 25°C$	0.437	1.5								MHz
Slew Rate	$T_A = 25°C$, Unity Gain	0.3	0.7			0.5			0.5		V/µs
Supply Current	$T_A = 25°C$					1.7	2.8		1.7	2.8	mA
Power Consumption	$T_A = 25°C$										
	$V_S = \pm 20V$		80	150							mW
	$V_S = \pm 15V$					50	85		50	85	mW
LM741A	$V_S = \pm 20V$										
	$T_A = T_{AMIN}$			165							mW
	$T_A = T_{AMAX}$			135							mW
LM741E	$V_S = \pm 20V$										
	$T_A = T_{AMIN}$			150							mW
	$T_A = T_{AMAX}$			150							mW
LM741	$V_S = \pm 15V$										
	$T_A = T_{AMIN}$					60	100				mW
	$T_A = T_{AMAX}$					45	75				mW

Note 1: For operation at elevated temperatures, these devices must be derated based on thermal resistance, and T_j max. (listed under "Absolute Maximum Ratings"). $T_j = T_A + (\theta_{jA} P_D)$.

Thermal Resistance	Cerdip (J)	DIP (N)	TO-5 (H)	SO-8 (M)
θ_{jA} (Junction to Ambient)	100°C/W	100°C/W	150°C/W	195°C/W
θ_{jC} (Junction to Case)	N/A	N/A	80°C/W	N/A

Note 2: For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.

Note 3: Unless otherwise specified, these specifications apply for $V_S = \pm 15V$, $-55°C \leq T_A \leq +125°C$ (LM741/LM741A). For the LM741C/LM741E, these specifications are limited to $0°C \leq T_A \leq +70°C$.

Note 4: Calculated value from: BW (MHz) = 0.35/Rise Time(µs).

Note 5: For military specifications see RETS741X for LM741 and RETS741AX for LM741A.

National Semiconductor Corporation

LM139/239/339, LM139A/239A/339A, LM2901, LM3302 Low Power Low Offset Voltage Quad Comparators

General Description

The LM139 series consists of four independent precision voltage comparators with an offset voltage specification as low as 2 mV max for all four comparators. These were designed specifically to operate from a single power supply over a wide range of voltages. Operation from split power supplies is also possible and the low power supply current drain is independent of the magnitude of the power supply voltage. These comparators also have a unique characteristic in that the input common-mode voltage range includes ground, even though operated from a single power supply voltage.

Application areas include limit comparators, simple analog to digital converters; pulse, squarewave and time delay generators; wide range VCO; MOS clock timers; multivibrators and high voltage digital logic gates. The LM139 series was designed to directly interface with TTL and CMOS. When operated from both plus and minus power supplies, they will directly interface with MOS logic— where the low power drain of the LM339 is a distinct advantage over standard comparators.

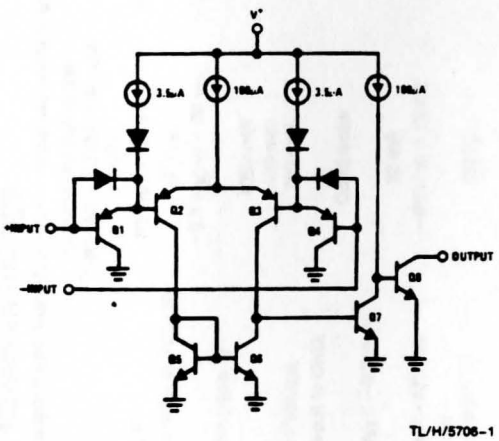
Advantages

- High precision comparators
- Reduced V_{OS} drift over temperature
- Eliminates need for dual supplies
- Allows sensing near GND
- Compatible with all forms of logic
- Power drain suitable for battery operation

Features

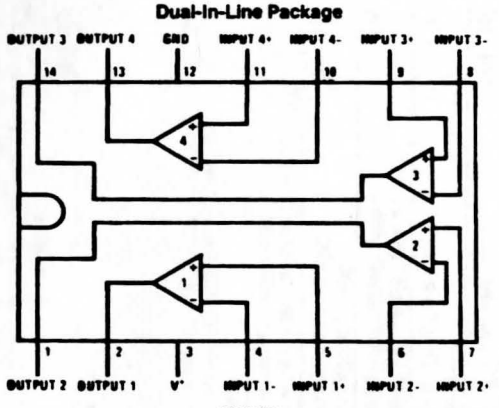
- Wide single supply voltage range of dual supplies
  - LM139 series, 2 V_{DC} to 36 V_{DC} or
  - LM139A series, LM2901 ±1 V_{DC} to ±18 V_{DC}
  - LM3302 2 V_{DC} to 28 V_{DC} or ±1 V_{DC} to ±14 V_{DC}
- Very low supply current drain (0.8 mA) — independent of supply voltage (2 mW/comparator at +5 V_{DC})
- Low input biasing current 25 nA
- Low input offset current ±5 nA
- and offset voltage ±3 mV
- Input common-mode voltage range includes GND
- Differential input voltage range equal to the power supply voltage
- Low output saturation voltage 250 mV at 4 mA
- Output voltage compatible with TTL, DTL, ECL, MOS and CMOS logic systems

Schematic and Connection Diagrams



TL/H/5706–1

Dual-In-Line Package



TOP VIEW

TL/H/5706–2

Order Number LM139J, LM139AJ, LM239J, LM239AJ, LM339J, LM339AJ, LM2901J or LM3302J
See NS Package Number J14A
Order Number LM339AM, LM339M or LM2901M
See NS Package Number M14A
Order Number LM339N, LM339AN, LM2901N or LM3302N
See NS Package Number N14A

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/Distributors for availability and specifications.(Note 10)

	LM139/LM239/LM339 LM139A/LM239A/LM339A LM2901	LM3302
Supply Voltage, V^+	36 V_{DC} or ±18 V_{DC}	28 V_{DC} or ±14 V_{DC}
Differential Input Voltage (Note 8)	36 V_{DC}	28 V_{DC}
Input Voltage	−0.3 V_{DC} to +36 V_{DC}	−0.3 V_{DC} to +28 V_{DC}
Power Dissipation (Note 1)		
Molded DIP	1050 mW	1050 mW
Cavity DIP	1190 mW	
Small Outline Package	760 mW	
Output Short-Circuit to GND, (Note 2)	Continuous	Continuous
Input Current ($V_{IN} < -0.3$ V_{DC}), (Note 3)	50 mA	50 mA
Storage Temperature Range	−65°C to +150°C	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	260°C	260°C

	LM139/LM239/LM339 LM139A/LM239A/LM339A LM2901	LM3302
Operating Temperature Range		−40°C to +85°C
LM339/LM339A	0°C to +70°C	
LM239/LM239A	−25°C to +85°C	
LM2901	−40°C to +85°C	
LM139/LM139A	−55°C to +125°C	
Soldering Information		
Dual-In-Line Package		
Soldering (10 seconds)	260°C	260°C
Small Outline Package		
Vapor Phase (60 seconds)	215°C	215°C
Infrared (15 seconds)	220°C	220°C

See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering surface mount devices.

ESD rating to be determined.

Electrical Characteristics ($V^+ = 5$ V_{DC}, T_A = 25°C, unless otherwise stated)

Parameter	Conditions	LM139A			LM239A, LM339A			LM139			LM239, LM339			LM2901			LM3302			Units
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage	(Note 9)		±1.0	±2.0		±1.0	±2.0		±2.0	±5.0		±2.0	±5.0		±2.0	±7.0		±3	±20	mV_{DC}
Input Bias Current	$I_{IN(+)}$ or $I_{IN(-)}$ with Output in Linear Range, (Note 5), $V_{CM} = 0V$		25	100		25	250		25	100		25	250		25	250		25	500	nA_{DC}
Input Offset Current	$I_{IN(+)} - I_{IN(-)}$, $V_{CM} = 0V$		±3.0	±25		±5.0	±50		±3.0	±25		±5.0	±50		±5	±50		±3	±100	nA_{DC}
Input Common-Mode Voltage Range	$V^+ = 30$ V_{DC} (LM3302, $V^+ = 28$ V_{DC}) (Note 6)	0		$V^+ - 1.5$	0		$V^+ - 1.5$	0		$V^+ - 1.5$	0		$V^+ - 1.5$	0		$V^+ - 1.5$	0		$V^+ - 1.5$	V_{DC}
Supply Current	$R_L = \infty$ on all Comparators,		0.8	2.0		0.8	2.0		0.8	2.0		0.8	2.0		0.8	2.0		0.8	2.0	mA_{DC}
	$R_L = \infty$, $V^+ = 36V$, (LM3302, $V^+ = 28$ V_{DC})					1.0	2.5		1.0	2.5		1.0	2.5		1.0	2.5		1.0	2.5	mA_{DC}
Voltage Gain	$R_L \geq 15$ kΩ, $V^+ = 15$ V_{DC}, $V_o = 1$ V_{DC} to 11 V_{DC}	50	200		50	200		50	200		50	200		25	100		2	30		V/mV
Large Signal Response Time	V_{IN} = TTL Logic Swing, V_{REF} = 1.4 V_{DC}, $V_{RL} = 5$ V_{DC}, $R_L = 5.1$ kΩ,		300			300			300			300			300			300		ns
Response Time	$V_{RL} = 5$ V_{DC}, $R_L = 5.1$ kΩ, (Note 7)		1.3			1.3			1.3			1.3			1.3			1.3		µs
Output Sink Current	$V_{IN(-)} = 1$ V_{DC}, $V_{IN(+)} = 0$, $V_O \geq 1.5$ V_{DC}	6.0	16		6.0	16		6.0	16		6.0	16		6.0	16		6.0	16		mA_{DC}

Electrical Characteristics ($V^+ = 5\ V_{DC}$, T_A = 25°C, unless otherwise stated) (Continued)

Parameter	Conditions	LM139A			LM239A, LM339A			LM139			LM239, LM339			LM2901			LM3302			Units
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Saturation Voltage	$V_{IN(-)} = 1\ V_{DC}$, $V_{IN(+)} = 0$, $I_{SINK} \leq 4$ mA		250	400		250	400		250	400		250	400		250	400		250	500	mV_{DC}
Output Leakage Current	$V_{IN(+)} = 1\ V_{DC}$, $V_{IN(-)} = 0$, $V_O = 5\ V_{DC}$		0.1			0.1			0.1			0.1			0.1			0.1		nA_{DC}

Electrical Characteristics ($V^+ = 5.0\ V_{DC}$, Note 4)

Parameter	Conditions	LM139A			LM239A, LM339A			LM139			LM239, LM339			LM2901			LM3302			Units
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage	(Note 9)			±4.0			±4.0			±9.0			±9.0		±9	±15			±40	mV_{DC}
Input Offset Current	$I_{IN(+)} - I_{IN(-)}$, $V_{CM} = 0V$			±100			±150			±100			±150		±50	±200			±300	nA_{DC}
Input Bias Current	$I_{IN(+)}$ or $I_{IN(-)}$ with Output in Linear Range, $V_{CM} = 0V$ (Note 5)			300			400			300			400		200	500			1000	nA_{DC}
Input Common-Mode Voltage Range	$V^+ = 30\ V_{DC}$ (LM3302, $V^+ = 28\ V_{DC}$) (Note 6)	0		$V^+ - 2.0$	0		$V^+ - 2.0$	0		$V^+ - 2.0$			$V^+ - 2.0$	0		$V^+ - 2.0$	0		$V^+ - 2.0$	V_{DC}
Saturation Voltage	$V_{IN(-)} = 1\ V_{DC}$, $V_{IN(+)} = 0$, $I_{SINK} \leq 4$ mA			700			700			700			700		400	700			700	mV_{DC}
Output Leakage Current	$V_{IN(+)} = 1\ V_{DC}$, $V_{IN(-)} = 0$, $V_O = 30\ V_{DC}$, (LM3302, $V_O = 28\ V_{DC}$)			1.0			1.0			1.0			1.0			1.0			1.0	μA_{DC}
Differential Input Voltage	Keep all V_{IN}'s $\geq 0\ V_{DC}$ (or V^-, if used), (Note 8)			36			36			36			36			36			28	V_{DC}

Note 1: For operating at high temperatures, the LM339/LM339A, LM2901, LM3302 must be derated based on a 125°C maximum junction temperature and a thermal resistance of 95°C/W which applies for the device soldered in a printed circuit board, operating in a still air ambient. The LM239 and LM139 must be derated based on a 150°C maximum junction temperature. The low bias dissipation and the "ON-OFF" characteristic of the outputs keeps the chip dissipation very small ($P_D \leq 100$ mW), provided the output transistors are allowed to saturate.

Note 2: Short circuits from the output to V^+ can cause excessive heating and eventual destruction. When considering short circuits to ground, the maximum output current is approximately 20 mA independent of the magnitude of V^+.

Note 3: This input current will only exist when the voltage at any of the input leads is driven negative. It is due to the collector-base junction of the input PNP transistors becoming forward biased and thereby acting as input diode clamps. In addition to this diode action, there is also lateral NPN parasitic transistor action on the IC chip. This transistor action can cause the output voltages of the comparators to go to the V^+ voltage level (or to ground for a large overdrive) for the time duration that an input is driven negative. This is not destructive and normal output states will re-establish when the input voltage, which was negative, again returns to a valve greater than $-0.3\ V_{DC}$ (at 25°)C.

Note 4: These specifications are limited to $-55°C \leq T_A \leq +125°C$, for the LM139/LM139A. With the LM239/LM239A, all temperature specifications are limited to $-25°C \leq T_A \leq +85°C$, the LM339/LM339A temperature specifications are limited to $0°C \leq T_A \leq +70°C$, and the LM2901, LM3302 temperature range is $-40°C \leq T_A \leq +85°C$.

Note 5: The direction of the input current is out of the IC due to the PNP input stage. This current is essentially constant, independent of the state of the output so no loading change exists on the reference or input lines.

Note 6: The input common-mode voltage or either input signal voltage should not be allowed to go negative by more than 0.3V. The upper end of the common-mode voltage range is $V^+ - 1.5V$ at 25°C, but either or both inputs can go to $+30\ V_{DC}$ without damage (25V for LM3302), independent of the magnitude of V^+.

Note 7: The response time specified is a 100 mV input step with 5 mV overdrive. For larger overdrive signals 300 ns can be obtained, see typical performance characteristics section.

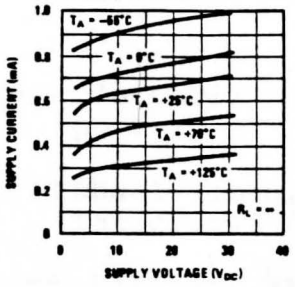
Note 8: Positive excursions of input voltage may exceed the power supply level. As long as the other voltage remains within the common-mode range, the comparator will provide a proper output state. The low input voltage state must not be less than $-0.3\ V_{DC}$ (or 0.3 V_{DC} below the magnitude of the negative power supply, if used) (at 25°C).

Note 9: At output switch point, $V_O \cong 1.4\ V_{DC}$, $R_S = 0\Omega$ with V^+ from $5\ V_{DC}$ to $30\ V_{DC}$; and over the full input common-mode range (0 V_{DC} to $V^+ - 1.5\ V_{DC}$), at 25°C. For LM3302, V^+ from $5\ V_{DC}$ to $28\ V_{DC}$.

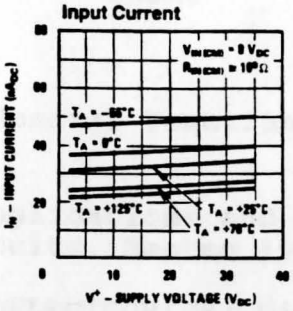
Note 10: Refer to RETS139AX for LM139AJ military specifications and to RETS139X for LM139J military specifications.

Typical Performance Characteristics LM139/LM239/LM339, LM139A/LM239A/LM339A, LM3302

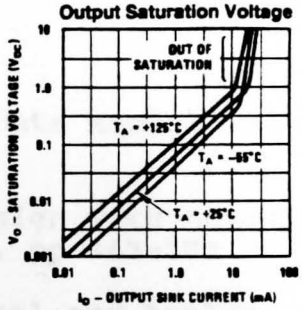
Supply Current



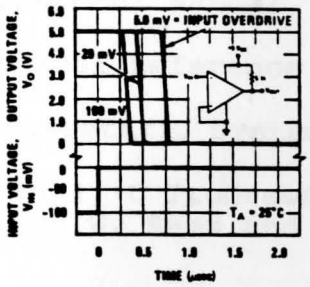
Input Current



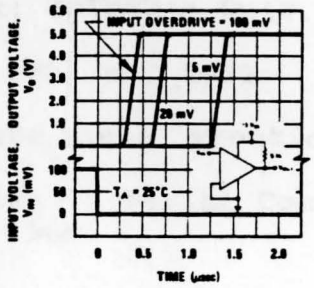
Output Saturation Voltage



Response Time for Various Input Overdrives—Negative Transition



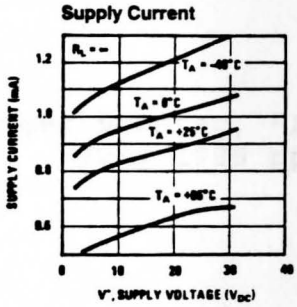
Response Time for Various Input Overdrives—Positive Transition



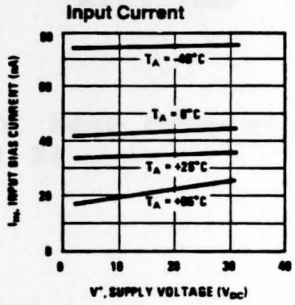
TL/H/5706–6

Typical Performance Characteristics LM2901

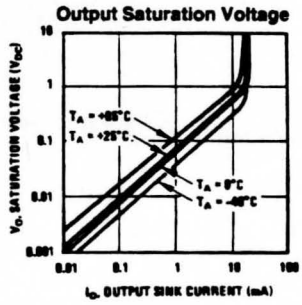
Supply Current



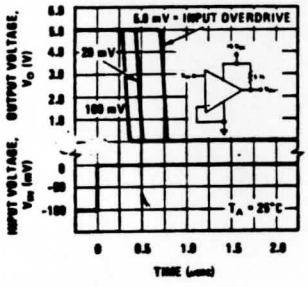
Input Current



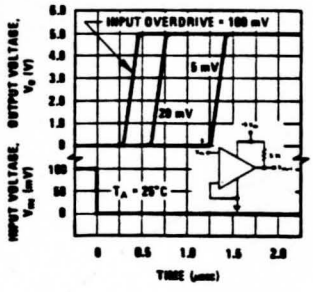
Output Saturation Voltage



Response Time for Various Input Overdrives-Negative Transition



Response Time for Various Input Overdrives-Positive Transition



TL/H/5706–7

REFERENCE

Books

Motorola CMOS/NMOS Special Functions Data Manual 1988, pp 7-10

J. Michael Jacob, Applications and Design with Analog Integrated Circuits, Reston 1982, pp 363-373

Jacob Millman, MICROELECTRONICS: Digital and Analog Circuits and Systems, McGraw-Hill, 1979, pp 350-351.

Kermit Protocol Manual, New York: Columbia Univ. 1984.

IBM Technical Reference Manual, rev. ed. 1983.

T. J. Biggerstaff, Systems Software Tools, Prentice Hall 1986.

Joe Campbell, C Programmer's Guide To Serial Communications, Howard W. Sams and Company 1988.

Articles

Roger Sonntag, "Light Beam Communicator", Radio Electronics, July 1989 pp 31-34