

MODELING, ANALYSIS, SIMULATION AND MEASUREMENTS
OF A FLY-BACK MULTI-LOOP CONTROL SWITCHING MODE POWER SUPPLY

by

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ABSTRACT

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Modeling, analysis, simulation and the measurements of a fly-back switching mode power supply employing multiple loop control are presented. The objectives are to examine the small-signal dynamic performances and to provide an adequate measurement method for the fly-back switching mode power supply which is operated in continuous MMF mode at a constant frequency.

To gain insights to the performance characteristics of the power supply, the power supply is modeled according to the three basic functional blocks: fly-back power stage, error processor, and pulse width modulator. After the small-signal model of each block are assembled, the audio-susceptibility, output impedance, and system loop gain characteristics are simulated. Finally, an adequate measurement method, digital modulation technique, is introduced and the experimental verifications of the system loop gain are presented.

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LIST OF SYMBOLS

SYMBOL	DEFINITION
A/D	Analog to digital converter
A(s)	Open-loop gain of an operational amplifier
A _x , A _y	Gains
C	Control output
C ₁ - C ₃	Capacitors or capacitance
d(t)	Instantaneous value of the duty cycle
$\tilde{d}(t)$	Time-varying component of the duty cycle
D	Steady state value of the duty cycle
D'	D' = 1 - D
dx	Digital forward signal in the loop gain measurement
dx*	Delayed digital forward signal for measurement
dy	Digital returned signal in the loop gain measurement
dy*	Delayed digital returned signal for measurement
dy _A , dy _B	Push-pull inputs to the digital modulator
dz	Injected digital disturbance in the loop gain measurement
E	Error output
EP	Error processor
E _r	Reference voltage source
ESR	Equivalent series resistance of a capacitor
F _C	Transfer function of the current feedback loop
F _{D1} , F _{D2}	Elements of dynamic matrix related to duty cycle
F _M	Transfer function of the pulse width modulator
F _V	Transfer function of the voltage feedback loop

G	Forward path gain
G_A	Audio-susceptibility characteristics
GQ	Circuit parameter
H	Feedback path gain
$\tilde{i}_o(t)$	Small-signal component of the output current
$i_o(t)$	Instantaneous value of the output current
$i_p(t)$	Instantaneous value of the current in the primary winding of a inductor
$\tilde{i}_p(t)$	Small-signal component of i_p
$i_s(t)$	Instantaneous value of the current in the secondary winding of a inductor
K	Constant
KCL	Kirchoff's current law
KVL	Kirchoff's voltage law
L_e	Inductance
LISA	Computer program package, Linear System Analysis, developed by IBM
L_p	Primary inductance
L_s	Secondary inductance
LSI	Large scale integration
MMF	Magnetomotive force
MOSFET	Metal oxide semiconductor field effect transistor
n	Turns ratio of a current transformer
N_p	Turns of the primary windings
N_s	Turns of the secondary windings
PWM	Pulse width modulation
R	Reference input
R_N, R_e	Resistors or equivalent resistance
R_C	ESR of a capacitor

R_L	Load resistor
R_P	DC resistance in the primary winding of a inductor
R_S	DC resistance in the secondary winding of an inductor
R_{SW}	Load resistor of a current transformer
S_N, S_F	Slopes
T	System loop gain
T_{off}, T_{F1}	Turn-off interval
T_{on}	Turn-on interval
T_p	Period
\underline{U}	Input vector (steady state)
\underline{u}	Input vector
\tilde{v}_a, \tilde{v}_b	Small-signal voltage at node A and node B respective to common
$v_C(t)$	Instantaneous value of the capacitor voltage
$v_i(t)$	Instantaneous value of the input voltage
$\tilde{v}_i(t)$	Small-signal component of the input voltage
V_i	DC component of the input voltage
V_O	DC output voltage
$\tilde{v}_O(t)$	Small-signal component of the output voltage
$v_S(t)$	Voltage induced in the secondary winding of an inductor
$v_{sw}(t)$	Voltage output in a current transformer with load resistor
$v_t(t)$	Threshold voltage
$v_x(t)$	Output voltage of the error processor
V_x	Analog forward signal in the loop gain measurement
V_y	Analog returned signal in the loop gain measurement
V_z	Injected analog disturbance in the loop gain measurement

ω_n	Circuit parameter or natural frequency
\underline{x}	State variable
\tilde{x}	Time-varying component of x
\dot{x}	dx/dt
$\dot{\tilde{x}}$	$d\tilde{x}/dt$
\underline{y}	Output vector
Z_X, Z_Y	Impedance
Z_O	Output impedance
ϕ	Magnetic flux
ζ	Circuit parameter or damping factor
Δ	Characteristic equation of the fly-back power stage

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CHAPTER 1

INTRODUCTION

Switching mode power supplies [1] have gained widespread use recently. Because of their high efficiency, small size and weight, they are replacing the conventional linear power supply in both industrial applications and consumer products. To reduce the size, weight and power dissipation of LSI equipments, particularly in microprocessor based units and television, most designers are turning to switching mode power supplies. Increased volume production, particularly of semiconductors and special magnetic material, have reduced the price of switching mode power supply to the point that their advantages are now available to all users.

Fundamentally, the switching mode power supply is a DC/DC converter. The basic fly-back configuration of a DC/DC converter is shown in Figure 1. The energy exchange takes place in the fly-back DC/DC converter in the following fashion. While the switch is closed, a current flows through the inductor, L , and stores the energy in the magnetic field. As the switch is open, the stored energy in the magnetic field is discharged into the capacitor and load resistor, transforming energy from the input to the output. The transformer coupled version of the basic fly-back configuration is shown in Figure 2. This version provides several important advantages, particularly in

applications where primary power is 120VAC or 230VAC. First, the transformer provides input/output isolation required for off-line power supplies and removes the polarity restriction of the input/output in Figure 1. Also, multiple outputs at various voltage are easily obtained with multiple secondary windings.

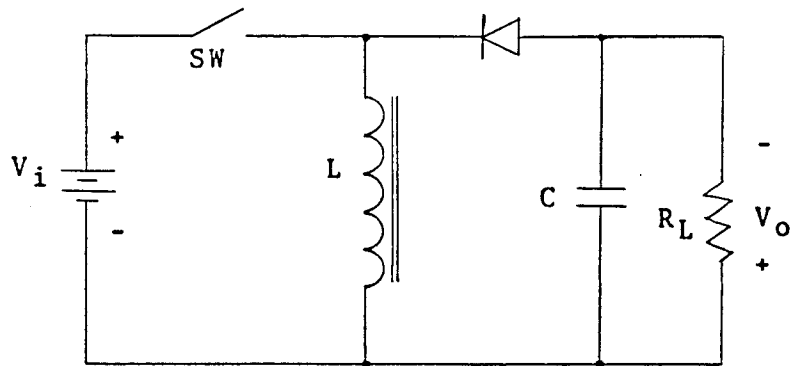


Figure 1. Basic Configuration of a Fly-back DC/DC Converter

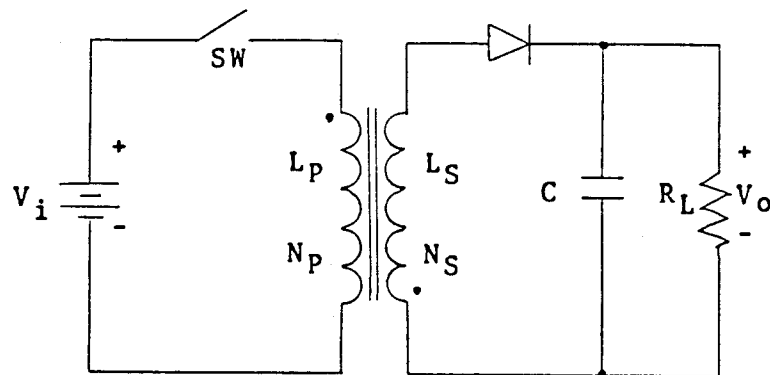


Figure 2. Transformer Coupled Version of a Fly-back DC/DC Converter

Due to the finite flux capacity of the inductive element, a DC/DC converter must be oscillatory in nature.

The oscillation is achieved by cyclically operating the power switch of the converter in the conduction and the non-conduction state. Consequently, the converter control system must be able to accept an analog signal obtained from the sensing circuit and reference and convert it into discrete time intervals for controlling the conduction and non-conduction of the power switch. The electrical performance characteristics of interest to a converter designer include stability as well as the converter output response to a step and sinusoidal disturbances, both from the line and the load.

The conventional single loop control power supply senses the capacitor state variable in the form of an output capacitor voltage to serve as the control signal. Illustrated in Figure 3 is a fly-back switching power supply employing multiple loop control. In addition to the capacitor voltage sensing loop, a second loop sensing the inductor current is present. The total sensing of the states associated with the LC section provides the power supply with excellent static and dynamic stabilities. In addition, the frequency response shaping can become grossly ineffective due to variations of power or control component parameters resulting from tolerance, environments, aging and operating condition.

In Figure 3, the control is implemented by sensing the following quantities: the output voltage of the converter, v_o , or the output capacitor voltage, and the instantaneous current through the power switch, i_p , or the

inductor current. The duty cycle signal is terminated by the threshold detector when the switching current ascends and intersects the floating threshold voltage, v_x , which is determined by subtracting v_o from the reference voltage, E_r . This threshold detector thus provides inherent transistor peak current protection and limits the electrical stresses in power components as well.

Presented in this thesis are the modeling, analysis, simulation, and measurement of the above described system in Figure 3, which contains three basic functional blocks: a fly-back power stage, an error processor, and a pulse width modulator. The modeling and analysis approaches applied to each block are listed below:

- (1) Fly-back power stage: State space averaging technique [2] and state space representation are used to develop the model of three inputs with two outputs for the fly-back power stage. After perturbation, linearization and the Laplace transformation are taken, a small-signal model and a set of transfer functions are obtained.
- (2) Error processor: Deriving the input/output model of error processor by KCL is straightforward.
- (3) Pulse width modulator: The describing function technique [3] and Fourier series are used to derive the model of the pulse width modulator.

The small-signal model of Figure 3 is derived as shown in Figure 4. The small-signal model has the following features:

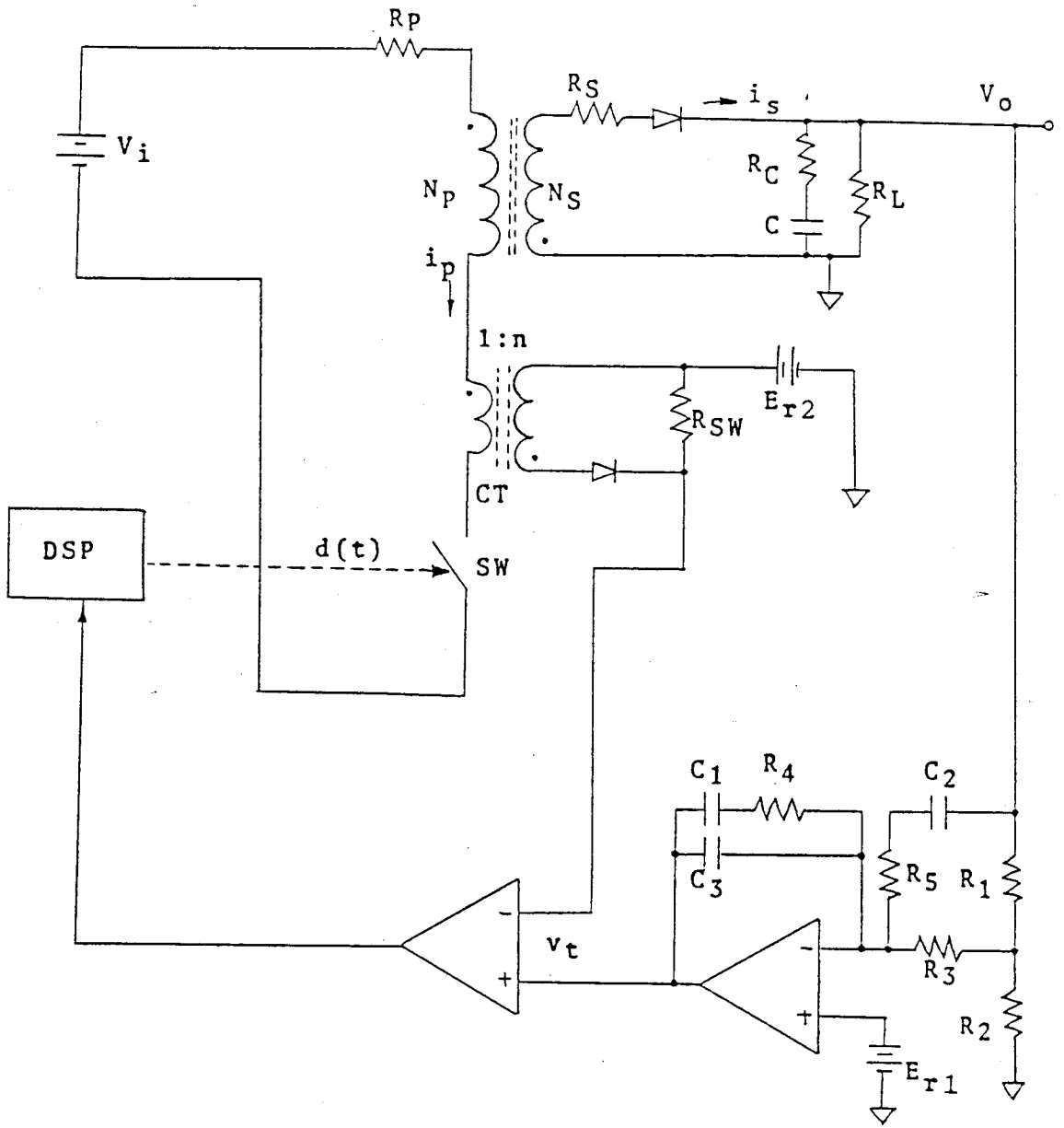
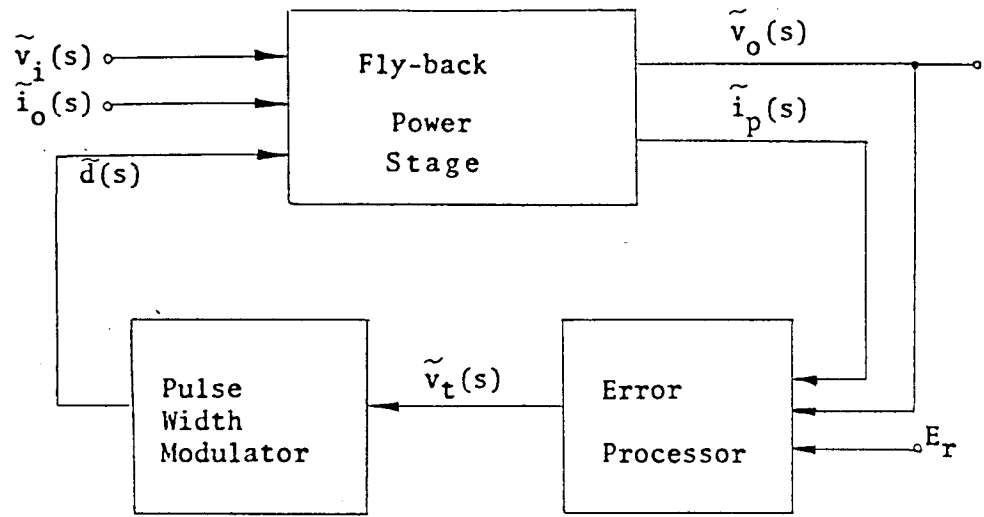
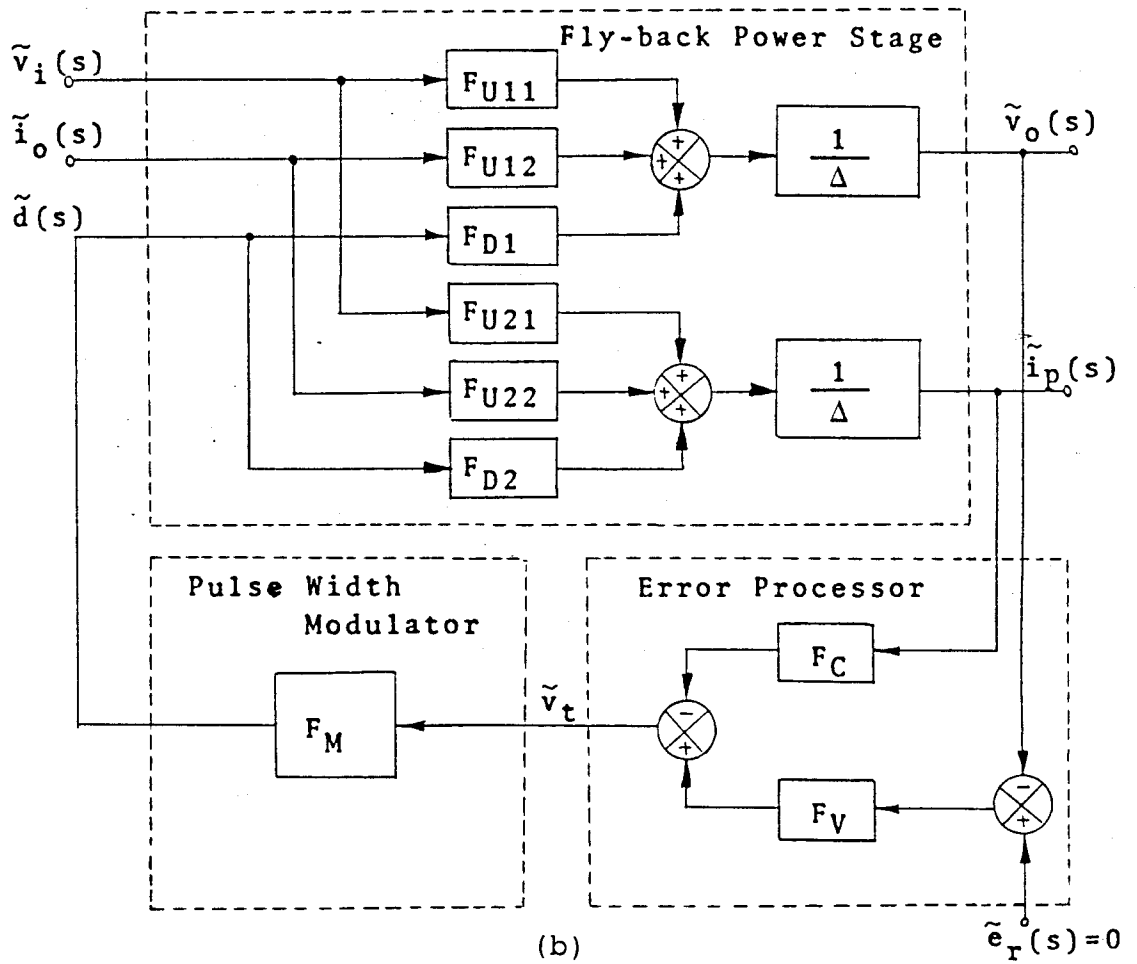


Figure 3. Circuit Schematic of a Two-loop Control Fly-back Switching Mode Power Supply



(a)



(b)

Figure 4. Two-loop Control Fly-back Switching Mode Power Supply. (a) Simplified Functional Blocks, (b) Small-signal Model

(a) The fly-back power stage has three inputs and two outputs. The three inputs are:

Line disturbance \tilde{v}_i

Load disturbance \tilde{i}_o

Duty cycle disturbance \tilde{d}

The two outputs are:

The output voltage \tilde{v}_o

The switching current \tilde{i}_p

(b) The error processor senses the two modulation signals, \tilde{i}_p and \tilde{v}_o . The transfer function F_V represents the gain of the voltage control loop and compensation network. The F_C represents the gain of the current control loop.

(c) The pulse width modulator is represented by a "single-input single-output" model, F_M .

Employing the above described small-signal model, one can readily examine the following performance characteristics:

(1) The system loop gain characteristics

$$T = \frac{1}{\Delta} F_M (F_V F_{D1} + F_C F_{D2}) \quad (1)$$

The system loop gain characteristics T is used to examine the relative stability of the system.

(2) The audio-susceptibility characteristics $G_A = \tilde{v}_o / \tilde{v}_i$

(3) The output impedance characteristics $Z_O = \tilde{v}_o / \tilde{i}_o$

Although the above described small-signal model is a linear system, examining the performance characteristics without a computer becomes a tedious and time consuming

task. Therefore, computer simulation or the study of the dynamic response of mathematical models using the electronic computer has become a standard tool in engineering. Many computer program packages designed to solve linear equations and transfer functions are now available. Among those packages for such an approach is the "LISA 360 A Program for Linear System Analysis (LISA 360)" [4], a well-known computer program package developed by IBM. The LISA 360 program package can be used to compute the following solutions:

- (a) Pole and zero locations
- (b) Time response to a step or a sinusoidal inputs
- (c) Bode response over a range of frequencies
- (d) Sensitivity of a function to component variations at a given frequency

From computer simulation, the information about performance characteristics of this power supply can be obtained.

Finally, a real circuit shown in Figure 5 has been constructed for demonstration purposes. Also, a digital modulation scheme for loop gain measurements is presented. The measurements of the system loop gains of the actual circuit were performed to verify the small-signal model.

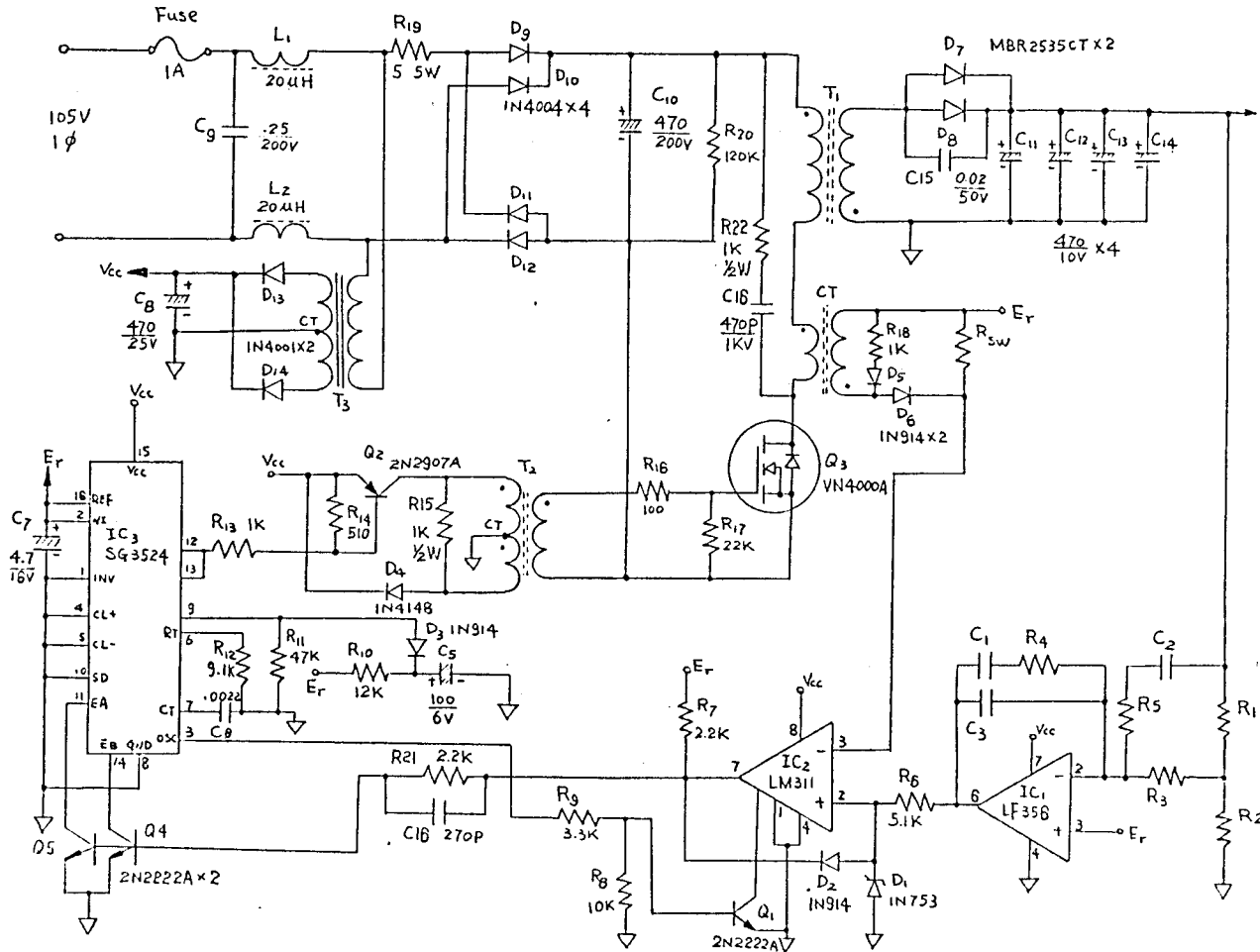


Figure 5. Complete Schematic Diagram of a Fly-back, Multiple Loop Control, Switching Mode Power Supply

CHAPTER 2

CURRENT-FEEDBACK FLY-BACK POWER STAGE MODEL

2.1 Power Circuit Description

The function of the power supply is to process and transfer electric power from an unregulated input V_i to a regulated output V_o . Fundamentally, the power stage of a power supply is a DC/DC converter. The output voltage of the two-winding fly-back converter as shown in Figure 6 can be either greater than or less than the input voltage, depending on the duty cycle of the switch and the turns ratio of the storage inductor. The magnetically-coupled windings, provided by the energy-storage inductor, allows for input/output isolation and multiple outputs. In addition, proper choice of the inductor's turns ratio also can alleviate the difficulty of implementing the extreme duty cycle condition due to wide ranges of input and output voltages.

The energy exchange takes place in the power stage in the following fashion. The state of the duty cycle $d(t)$ determines the instantaneous position of the switch. The high level state of the signal $d(t)$ indicates conduction, and the low-level state determines the off-time, or off-state, of the power switch. During T_{on} a voltage approximately equal to $V_i(t)$ (neglecting the losses due to the parasitic resistance in the primary windings) is established across N_p which causes a current $i_p(t)$ to increase as illustrated in Figure 6.

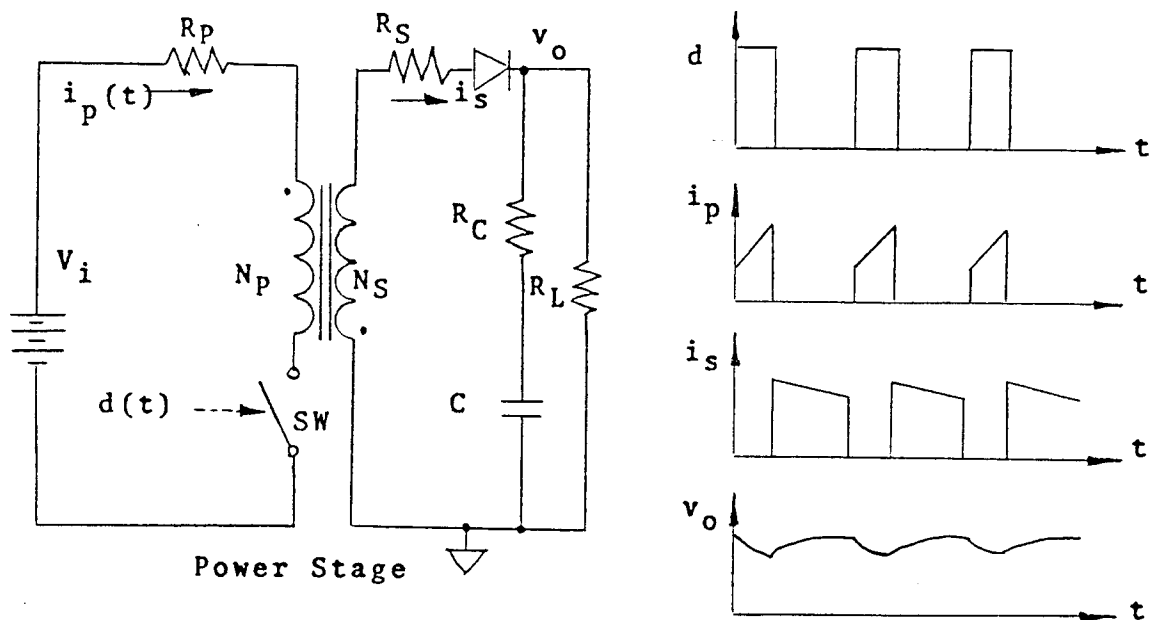


Figure 6. DC/DC Two-winding Fly-back Converter

Simultaneously, a voltage $V_s(t)$ is induced across N_s by transformer action, but no current conduction takes place because of the reverse biased diode. As the off-time, T_{off} is initiated, the energy associated with N_p is transferred to N_s by an ampere-turn redistribution. As a result, the current $i_p(t)$ is reduced to zero and $i_s(t)$ is forced to a magnitude needed to maintain a continuous MMF flow through the inductor. The output voltage in Figure 6 is kept nearly constant due to the large capacitive filter at the output which absorbs the pulsating current $i_s(t)$ and delivers an almost DC current, i_o , to the load.

2.2 Analytical Implementation

The nondissipative, switched DC/DC converter is nonlinear in nature. The basic DC/DC voltage conversion is achieved by repetitive switching between a number of linear networks consisting of switches and diodes. The number of linear networks in one switching cycle is determined by the mode of operation of the inductor's magnetomotive force, MMF. If the MMF is continuous as shown in Figure 7, the power stage model has two linear networks. For a

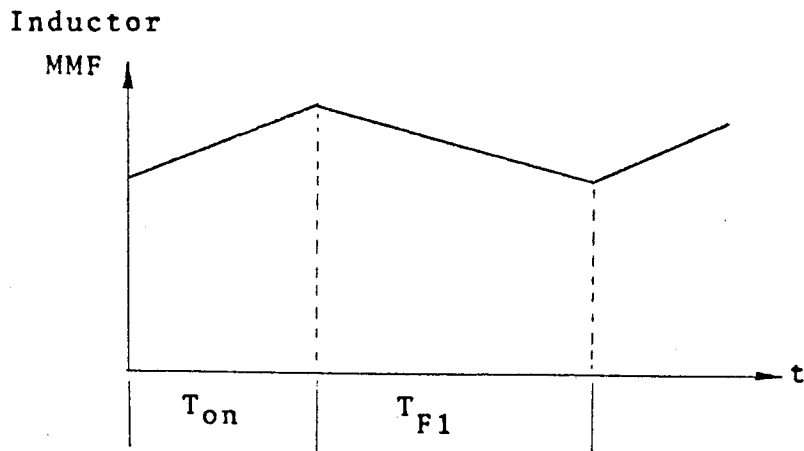


Figure 7. MMF in Continuous Operation Mode

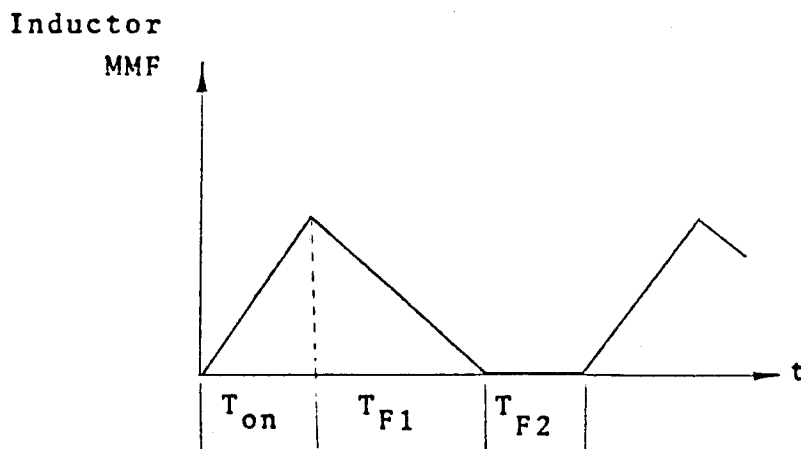


Figure 8. MMF in Discontinuous Operation Mode

discontinuous inductor MMF operation as shown in Figure 8, the power stage model has three linear networks

Each linear circuit model is described by a set of linear state space equations. For the current feedback fly-back power stage, the state variables are customarily the magnetic flux, ϕ , and the capacitor voltage, v_c . The total number of storage elements determines the order of the system.

2.2.1 State Space Averaging Technique

To derive a linear model for the power stage, the averaging technique is used. Employing the continuous operation mode, the power stage is modeled by two intervals of operation, T_{on} and T_{F1} , respectively.

$$\begin{array}{ll} (1) \text{ interval } T_{on} & (2) \text{ interval } T_{F1} \\ \dot{\underline{x}} = A1 \underline{x} + B1 \underline{u} & \dot{\underline{x}} = A2 \underline{x} + B2 \underline{u} \end{array} \quad (2)$$

$$\underline{y} = C1 \underline{x} + E1 \underline{u} \qquad \underline{y} = C2 \underline{x} + E2 \underline{u} \quad (3)$$

The principle of the average method is to replace the state description of the two linear circuits by a single state-space description which represents the approximate behavior of the system through one cycle of operation. Taking the average of both intervals and summing the results yields the following linear equation for a continuous system:

$$\dot{\underline{x}} = d (A1 \underline{x} + B1 \underline{u}) + d' (A2 \underline{x} + B2 \underline{u}) \quad (4)$$

$$\underline{y} = d (C1 \underline{x} + E1 \underline{u}) + d' (C2 \underline{x} + E2 \underline{u}) \quad (5)$$

$$d = \frac{T_{on}}{T_p} \qquad d' = \frac{T_{F1}}{T_p}$$

where T_p is the period of the switching cycle.

The basic requirement for the average method is that the effective filter corner frequency of the switching converter must be much lower than the switching frequency.

The linear time-varying equations can be rewritten in the following form:

$$\dot{\underline{x}} = A \underline{x} + B \underline{u} \quad (6)$$

$$\underline{y} = C \underline{x} + E \underline{u} \quad (7)$$

where $A = d A1 + d' A2$, $B = d B1 + d' B2$, $C = d C1 + d' C2$
 $E = d E1 + d' E2$.

2.2.2 Perturbation

To study the small-signal behavior, the time-varying equations are perturbed. The introduction of input variations and duty cycle variations in turn perturb the output and state vectors. The perturbed input vectors are:

$$\underline{u} = \underline{U} + \underline{\tilde{u}} \qquad \underline{d} = \underline{D} + \underline{\tilde{d}}$$

where U and D are the steady-state values. These perturbations in turn lead to the following equations:

$$\underline{x} = \underline{X} + \underline{\tilde{x}} \qquad \dot{\underline{\tilde{x}}} = \underline{\tilde{x}} \qquad \underline{y} = \underline{Y} + \underline{\tilde{y}}$$

where \underline{x} and \underline{y} are the steady-state values.

Let $f(\underline{x}, \underline{u}, d) = \dot{\underline{x}} = A \underline{x} + B \underline{u}$, and recall Taylor's series:

$$\begin{aligned}
 f(\underline{x}, \underline{u}, d) = & f(\underline{X}, \underline{U}, D) + f_{\underline{x}}(\underline{X}, \underline{U}, D) \tilde{x} + f_{\underline{u}}(\underline{X}, \underline{U}, D) \tilde{u} + \\
 & f_{\underline{d}}(\underline{X}, \underline{U}, D) \tilde{d} + 1/2 [f_{\underline{xx}}(\underline{X}, \underline{U}, D) \tilde{x}^2 + \\
 & f_{\underline{uu}}(\underline{X}, \underline{U}, D) \tilde{u}^2 + f_{\underline{dd}}(\underline{X}, \underline{U}, D) \tilde{d}^2 + \\
 & 2f_{\underline{xu}}(\underline{X}, \underline{U}, D) \tilde{x} \tilde{u} + 2f_{\underline{ud}}(\underline{X}, \underline{U}, D) \tilde{u} \tilde{d} + \\
 & 2f_{\underline{xd}}(\underline{X}, \underline{U}, D) \tilde{x} \tilde{d}] + \text{high order terms}
 \end{aligned} \tag{8}$$

Comparing equation (4) to equation (8), we note that $f_{\underline{xx}}$, $f_{\underline{uu}}$, $f_{\underline{dd}}$, and $f_{\underline{xu}}$ are zero. The basic equation for the model becomes:

$$\begin{aligned}
 \dot{\underline{x}} = & A\underline{x} + B\underline{u} + A \tilde{x} + B \tilde{u} + [(A1 - A2) \underline{x} + (B1 - B2) \underline{u}] \tilde{d} + \\
 & [(A1 - A2) \tilde{x} + (B1 - B2) \tilde{u}] \tilde{d}
 \end{aligned} \tag{9}$$

With the corresponding perturbations substituted into the output equation, the output equation becomes:

$$\begin{aligned}
 \underline{y} + \tilde{y} = & C\underline{x} + E\underline{u} + C\tilde{x} + E\tilde{u} + [(C1 - C2) \underline{x} + (E1 - E2) \underline{u}] \tilde{d} + \\
 & [(C1 - C2) \tilde{x} + (E1 - E2) \tilde{u}] \tilde{d}
 \end{aligned} \tag{10}$$

The perturbed state-space description is nonlinear owing to the presence of the product of two time-dependent quantities \tilde{x} and \tilde{d} .

2.2.3 Linearization

Since the ac variations are very small in magnitude compared to their steady-state value, the following small-signal approximations can be made:

$$\frac{\tilde{u}}{U} \ll 1 ; \quad \frac{\tilde{x}}{X} \ll 1 ; \quad \frac{\tilde{y}}{Y} \ll 1$$

Using the above approximations, the nonlinear second order terms in both the basic model and the output equations can be neglected, resulting in a system of linear equations. Separating the steady-state (dc) and dynamic (ac) parts, the final equations representing the state space model are ascertained. The equations based on the steady-state (dc) model follow:

$$\underline{X} = -A^{-1} B \underline{U} \quad (11)$$

$$\underline{Y} = C \underline{X} + E \underline{U} = C (-A^{-1} B \underline{U}) + E \underline{U} = (E - CA^{-1} B) \underline{U} \quad (12)$$

For the linear dynamic case:

$$\dot{\underline{x}} = \underline{A} \underline{x} + \underline{B} \underline{u} + [(A1 - A2) \underline{x} + (B1 - B2) \underline{u}] \tilde{d} \quad (13)$$

$$\underline{y} = \underline{C} \underline{x} + \underline{E} \underline{u} + [(C1 - C2) \underline{x} + (E1 - E2) \underline{u}] \tilde{d} \quad (14)$$

2.2.4 Transfer Function For Small-Signal Analysis

For the small-signal analysis, there are particular input/output relations needed to construct the basic

building blocks that are necessary to describe the power stage completely.

In order to find the input/output transfer function, one assumes the duty-cycle variation is zero. Then, the previous linear equations can be simplified as follows:

$$\dot{\underline{\tilde{x}}} = \underline{\tilde{A}}\underline{\tilde{x}} + \underline{\tilde{B}}\underline{\tilde{u}} ; \quad \underline{\tilde{y}} = \underline{\tilde{C}}\underline{\tilde{x}} + \underline{\tilde{E}}\underline{\tilde{u}} \quad (15)$$

Taking the Laplace transformation of the above equations, the following relations are obtained:

$$s\underline{\tilde{x}}(s) - \underline{\tilde{x}}(0) = \underline{\tilde{A}}\underline{\tilde{x}}(s) + \underline{\tilde{B}}\underline{\tilde{u}}(s) \quad (16)$$

Let $\underline{\tilde{x}}(0) = 0$, then

$$\underline{\tilde{x}}(s) = [sI - \underline{\tilde{A}}]^{-1} \underline{\tilde{B}}\underline{\tilde{u}}(s) \quad (17)$$

$$\begin{aligned} \underline{\tilde{y}}(s) &= \underline{\tilde{C}} [sI - \underline{\tilde{A}}]^{-1} \underline{\tilde{B}}\underline{\tilde{u}}(s) + \underline{\tilde{E}}\underline{\tilde{u}}(s) \\ &= [\underline{\tilde{C}} (sI - \underline{\tilde{A}})^{-1} \underline{\tilde{B}} + \underline{\tilde{E}}] \underline{\tilde{u}}(s) \end{aligned} \quad (18)$$

In order to find the duty cycle/output transfer function, one assumes the input variation is zero. Then, the linear dynamic equations become:

$$\dot{\underline{\tilde{x}}} = \underline{\tilde{A}}\underline{\tilde{x}} + [(\underline{\tilde{A}}_1 - \underline{\tilde{A}}_2)\underline{\tilde{x}} + (\underline{\tilde{B}}_1 - \underline{\tilde{B}}_2)\underline{\tilde{u}}] \underline{\tilde{d}} \quad (19)$$

$$\underline{\tilde{y}} = \underline{\tilde{C}}\underline{\tilde{x}} + [(\underline{\tilde{C}}_1 - \underline{\tilde{C}}_2)\underline{\tilde{x}} + (\underline{\tilde{E}}_1 - \underline{\tilde{E}}_2)\underline{\tilde{u}}] \underline{\tilde{d}} \quad (20)$$

Taking the Laplace transformation of the above equations, the following relations are obtained:

$$\underline{\tilde{x}}(s) - \underline{\tilde{x}}(0) = A\underline{\tilde{x}}(s) + [(A1 - A2)\underline{X} + (B1 - B2)U] \underline{\tilde{d}}(s) \quad (21)$$

$$\underline{\tilde{y}}(s) = C\underline{\tilde{x}}(s) + [(C1 - C2)\underline{X} + (E1 - E2)U] \underline{\tilde{d}}(s) \quad (22)$$

Let $\underline{\tilde{x}}(0) = 0$, and the resulting state-variable $\underline{\tilde{x}}$ to duty-cycle modulation $\underline{\tilde{d}}$ and output $\underline{\tilde{y}}$ to duty-cycle modulation $\underline{\tilde{d}}$ are:

$$\frac{\underline{\tilde{x}}(s)}{\underline{\tilde{d}}(s)} = (sI - A)^{-1} [(A1 - A2)\underline{X} + (B1 - B2)U] \quad (23)$$

$$\frac{\underline{\tilde{y}}(s)}{\underline{\tilde{d}}(s)} = C (sI - A)^{-1} [(A1 - A2)\underline{X} + (B1 - B2)U] + [(C1 - C2)\underline{X} + (E1 - E2)U] \quad (24)$$

These transfer functions will be used as building blocks to construct the power stage transfer functions presented in the following sections.

2.3 Power Stage Model

The objective of the power stage model is to develop a group of transfer functions that describe the low frequency behavior of the switching circuit. The model is comprised of three inputs and two outputs. The three inputs are the supply voltage, v_i , the output current, i_o , and the duty-cycle, d . The two outputs are the output voltage, v_o ,

and the switching current, i_p .

For the two winding fly-back power stage shown in Figure 9 (a), two equivalent linear circuit models for the continuous operation mode are shown in Figure 9 (b) and (c). The power stage model contains an ideal switch and a diode. The storage inductor is composed of a primary winding and a secondary winding with inductance L_p and L_s respectively. Also described by the model is the winding resistance, R_p and R_s . The output filter is represented by a capacitance and an equivalent series resistance, R_C . A current source, i_o , is employed to represent a disturbance injected into the converter from the load.

The power stage contains two energy storage elements; therefore, the state variables for both linear equivalent circuits are the magnetic flux, ϕ , and the capacitor voltage, v_C . The magnetic flux links the primary and secondary windings together.

During the interval T_{on} , the power stage is described by the following equations:

$$\dot{\underline{x}} = A1 \underline{x} + B1 \underline{u} \quad \underline{y} = C1 \underline{x} + E1 \underline{u} \quad (25)$$

where $\underline{x} = [\phi \ v_C]^T$, $\underline{u} = [v_i \ i_o]^T$, $\underline{y} = [v_o \ i_p]^T$

$$A1 = \begin{bmatrix} R_p & & & \\ -\frac{R_p}{L_p} & & 0 & \\ & & 1 & \\ 0 & -\frac{1}{(R_C + R_L)C} & & \end{bmatrix} \quad B1 = \begin{bmatrix} & & & \\ & & & \\ \frac{1}{N_p} & & 0 & \\ & & R_L & \\ 0 & & & -\frac{1}{(R_C + R_L)C} \end{bmatrix}$$

$$C1 = \begin{bmatrix} 0 & R_L \\ N_p & R_C + R_L \\ L_p & 0 \end{bmatrix} \quad E1 = \begin{bmatrix} 0 & R_C // R_L \\ 0 & 0 \end{bmatrix}$$

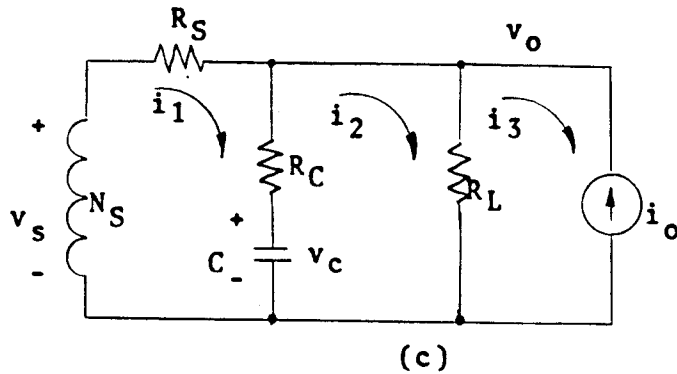
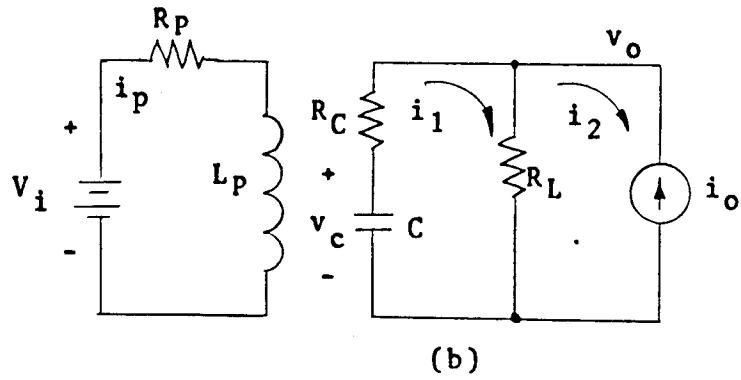
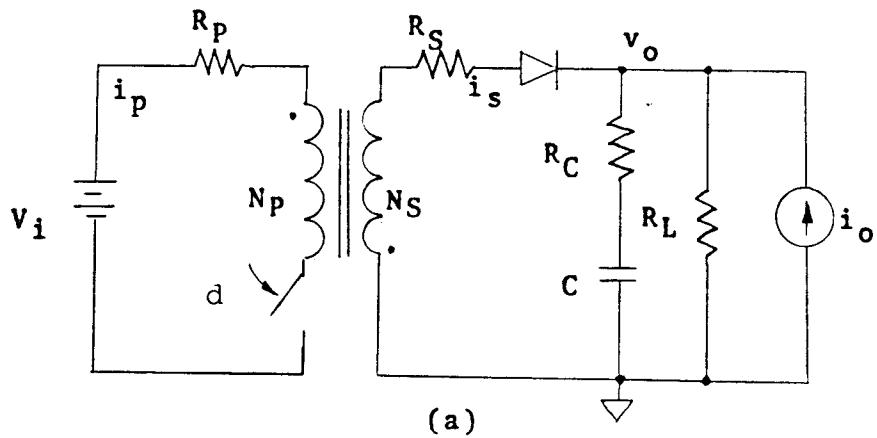


Figure 9. Two Winding Fly-back Power stage (a) Two Winding Fly-back Power Stage. (b) Equivalent Circuit Model During T_{on} . (c) Equivalent Circuit Model During T_{off}

During the interval T_{F1} the power stage is described by the following equations:

$$\dot{\underline{x}} = A2 \underline{x} + B2 \underline{u} \quad \underline{y} = C2 \underline{x} + E2 \underline{u} \quad (26)$$

where

$$A2 = \begin{bmatrix} R_S + (R_C // R_L) & R_L & 1 \\ \hline L_S & R_C + R_L & N_S \\ R_L & N_S & -1 & 1 \\ \hline R_C + R_L & L_S C & R_C + R_L & C \end{bmatrix}$$

$$B2 = \begin{bmatrix} 0 & -R_C // R_L & \frac{1}{N_S} \\ 0 & R_C & 1 \\ & R_C + R_L & C \end{bmatrix}$$

$$C2 = \begin{bmatrix} (R_C // R_L) & \frac{N_S}{L_S} & R_L \\ 0 & 0 & R_C + R_L \end{bmatrix}$$

$$E2 = \begin{bmatrix} 0 & R_C // R_L \\ 0 & 0 \end{bmatrix}$$

Appendix A shows the derivation of equations (25) and (26) representing the two equivalent linear models used to describe the power stage during the times T_{On} and T_{Fl} .

2.3.1 Average Model

Continuing the process to characterize the small-signal model needed to describe the dynamic behavior, the average model for the power stage is:

$$\dot{\underline{x}} = A \underline{x} + B \underline{u} \qquad \underline{y} = C \underline{x} + E \underline{u} \qquad (27)$$

$$A = \begin{bmatrix} \frac{-DR_P}{L_P} - D' \left[\frac{R_S + (R_C // R_L)}{L_S} \right] & \frac{-D' (R_C // R_L)}{N_S R_C} \\ \frac{D' (R_C // R_L)}{R_C L_S C} & \frac{-D}{(R_C + R_L) C} - \frac{D'}{(R_C + R_L) C} \end{bmatrix}$$

$$B = \begin{bmatrix} \frac{D}{N_P} & \frac{-D'}{N_S} \cdot (R_C // R_L) \\ 0 & \frac{D (R_C // R_L)}{R_C C} + \frac{D' (R_C // R_L)}{R_C C} \end{bmatrix}$$

$$C = \begin{bmatrix} \frac{D' N_S (R_C // R_L)}{L_S} & \frac{D (R_C // R_L)}{R_C} + \frac{D' (R_C // R_L)}{R_C} \\ \frac{D N_P}{L_P} & 0 \end{bmatrix}$$

$$E = \begin{bmatrix} 0 & (R_C // R_L) \\ 0 & 0 \end{bmatrix}$$

where D is the steady-state duty cycle and $D' = 1 - D$.

To simplify our matrix expressions, assume

- (1) $R_C \ll R_L$ so that $R_C // R_L \approx R_C$
 $R_C + R_L \approx R_L$
- (2) $\frac{R_P}{L_P} \approx \frac{R_S}{L_S}$

Also by definition the following conditions are used.

$$L_e = \frac{L_S}{D'^2} \qquad R_e = \frac{R_S}{D'^2}$$

$$\omega_o^2 = \frac{1}{L_e C} \qquad D = T_{on} / T_p$$

where T_p is the switching period.

$$\zeta = (\omega_o/2) [(L_e/R_L) + (R_e + R_C/D') C] \quad (28)$$

Applying these simplifications the average model equations become:

$$A = \begin{bmatrix} \frac{-R_S - D'R_C}{L_e (D')^2} & -\frac{D'}{N_S} \\ \frac{N_S \omega_o^2}{D'} & \frac{-1}{R_L C} \end{bmatrix} \qquad B = \begin{bmatrix} \frac{D}{N_P} & \frac{-D'R_C}{N_S} \\ 0 & 1/C \end{bmatrix}$$

$$C = \begin{bmatrix} \frac{N_S R_C}{L_e D'} & 1 \\ \frac{D N_P}{L_P} & 0 \end{bmatrix} \quad E = \begin{bmatrix} 0 & R_C \\ 0 & 0 \end{bmatrix}$$

2.3.2 Linearized Power Stage Model

The line voltage variation, \tilde{v}_i , duty cycle variation, \tilde{d} , and output current source disturbance, \tilde{i}_o , are introduced into the circuit such that

$$\begin{aligned} v_i &= V_i + \tilde{v}_i & d &= D + \tilde{d} \\ i_o &= 0 + \tilde{i}_o & d' &= D' - \tilde{d} \end{aligned}$$

where V_i is the DC input voltage, and D and D' are the steady-state on-time and off-time duty cycle.

Employing the small-signal approximations as described previously, a linear system of equations is obtained as follows:

Steady-state (dc) model equation:

$$\begin{aligned} \underline{y} &= [V_o \quad I_p]^T = (E - CA \quad B)^{-1} \underline{u} \\ &= \begin{bmatrix} DN_S & D^2 L_e \\ \text{-----} & \text{-----} \\ D' N_P & L_P R_L \end{bmatrix}^T \cdot V_i \end{aligned} \quad (29)$$

The input/output transfer function: (assuming the duty cycle variation is zero.)

$$\tilde{y}(s) = [\tilde{v}_o(s) \quad \tilde{i}_p(s)]^T = [C (sI - A)^{-1} B + E] \tilde{u}(s) \quad (30)$$

$$= \frac{\begin{bmatrix} \frac{N_S w_o^2 D}{D' N_P} (s R_C C + 1) & R_C (s^2 + z_1 s + w_o^2 z_2) \\ \frac{D^2}{L_P} (s + \frac{1}{R_L C}) & \frac{-DD' N_P}{L_P N_S C} (s R_C C + 1) \end{bmatrix} \begin{bmatrix} v_i(s) \\ i_o(s) \end{bmatrix}}{s^2 + 2\zeta w_o s + w_o^2}$$

where $z_1 = 2 w_o + 1/(R_C C) - (R_C/L_e)$, $z_2 = (R_e/R_C) + (D/D')$

Duty cycle/output transfer function: (assuming the input variation is zero.)

$$\begin{aligned} \tilde{y}(s)/\tilde{d}(s) &= C(sI-A)^{-1} [(A1-A2)\underline{X} + (B1-B2)\underline{U}] + \\ & [(C1-C2)\underline{X} + (E1-E2)\underline{U}] \end{aligned} \quad (31)$$

$$= \frac{V_o \left[\begin{aligned} & \frac{w_o^2}{DD'} (s R_C C + 1) \cdot \left\{ 1 - \frac{D}{R_L (s R_C C + 1)} \left[\frac{R_C}{w_o^2} s^2 + \left(\frac{2R_C \zeta}{w_o} + L_e \right) s + \left(R_e + \frac{R_C}{D'} \right) \right] \right\} \\ & \frac{N_S}{N_P R_L} \left\{ \frac{1}{CL_S} (s R_L C + 1 + D) + \frac{1}{D'} (s^2 + 2\zeta w_o s + w_o^2) \right\} \end{aligned} \right]}{s^2 + 2\zeta w_o s + w_o^2}$$

For detailed derivations of the transfer functions, refer to Appendix B.

Further simplifications are made by letting $\Delta = s^2 + 2\zeta\omega_0s + \omega_0^2$ and then forming the gain expressions. For the input/output transfer functions, the gain block in matrix form is given below:

$$\underline{\tilde{y}}(s) = \frac{1}{\Delta} \begin{bmatrix} F_{U11} & F_{U12} \\ F_{U21} & F_{U22} \end{bmatrix} \begin{bmatrix} \tilde{v}_i(s) \\ \tilde{i}_o(s) \end{bmatrix} \quad (32)$$

For the duty cycle/output transfer function, the matrix simplification expression is given below:

$$\underline{\tilde{y}}(s) = \frac{1}{\Delta} \begin{bmatrix} F_{D1} \\ F_{D2} \end{bmatrix} \tilde{d}(s) \quad (33)$$

The block diagram for the small-signal model of the fly-back power stage is shown in Figure 10.

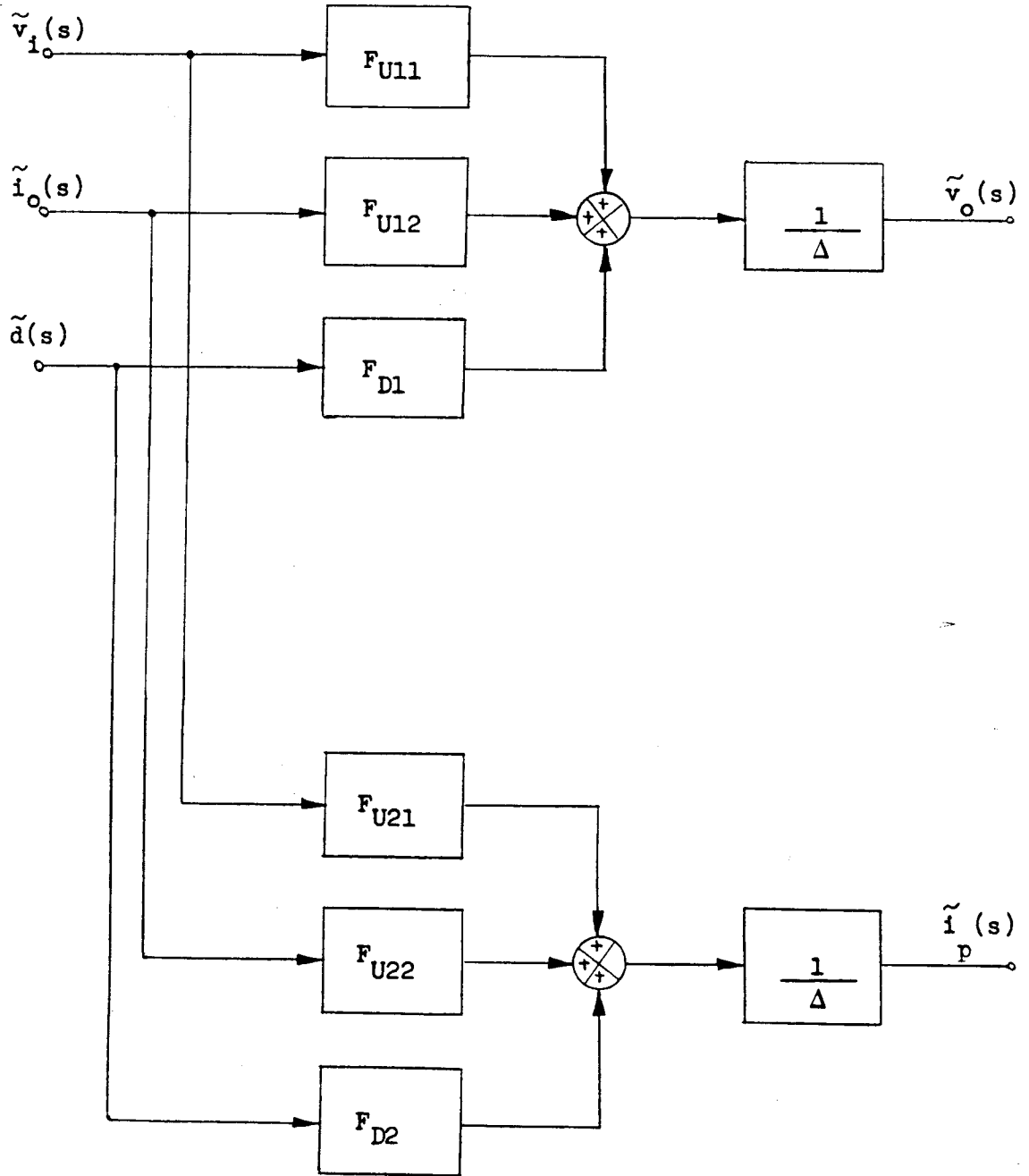


Figure 10. Block Diagram of Fly-back Power Stage

CHAPTER 3

ERROR PROCESSOR MODEL

3.1 Introduction

The error processor, EP, is a feedback compensation network. It processes multiple input control signals derived from the power stage, and delivers the required analog information to the pulse-width modulator. The analog signal error processor employed in the present analysis is shown in Figure 11. From a small-signal viewpoint, the error processor is a linear network consisting of two control loops. The signals sensed in these two loops are the converter output voltage, v_o , and the primary winding current of inductor, i_p .

The sensed v_o is processed by an error amplifier with reference, E_r , to generate a voltage error signal, v_x . The voltage error signal, after processing through an integral-plus-lead/lag compensation network, establishes the threshold level for the switching current signal derived from the current sensing loop [5]. The integral-plus-lead/lag compensation network is employed to shape the frequency response to improve the system stability and dynamic response.

The current loop which senses the drain current of the power MOSFET serves two functions. The first function is to transform the primary winding current into a proportional voltage signal. Then, this signal, v_{sw} , is

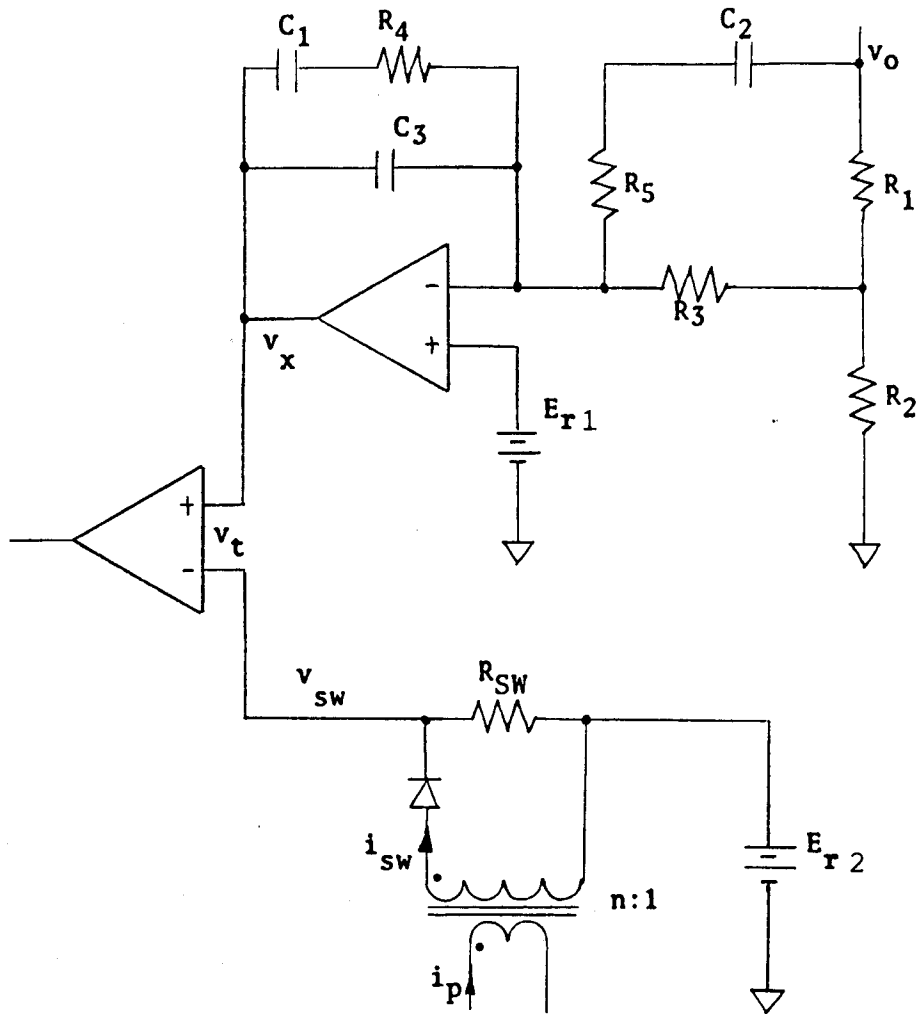


Figure 11. Error Processor

compared with v_x and results in a control that turns off the power switch when v_{sw} equals to v_x . The second function of the current loop is to derive the low frequency modulation signal or error signal for additional loop compensation.

3.2 Voltage and Current Loop Gains

As stated earlier, the current loop contains two types of information. One is the large amplitude switching

current waveform which is used to implement the analog to digital conversion. Such a function is considered a part of the pulse width modulator instead of the error processor. The second type of information contained in the current loop is the small amplitude low-frequency modulation signal, similar to the modulation signal sensed by the voltage loop. This information is brought together with the error signal from the voltage loop and compensation network to provide the total state feedback compensation for improved stability and dynamic response. For the purpose of modeling of the error processor, the large amplitude switching current information should be extracted from the current loop and be incorporated into the pulse width modulator.

In order to model the whole power supply by the three functional blocks: power stage, error processor, and pulse width modulator, the pulse width modulator should take the combined error signal from the error processor output and convert it into duty cycle signal. Furthermore, to implement such a "single-input single-output" pulse width modulator model, various error signals derived from the multiple feedback paths should be combined to form a composite error signal containing error information from voltage, current, and compensation loops.

For reasons mentioned above, the original error processor circuit is modified to that of Figure 12. Figure 12 is a functional equivalent to the original circuit shown in Figure 11. In Figure 12, the noninverting input, v_t , of

the threshold detector contains error signals from all feedback loops. The error voltage, v_t , is the output of the multiple loop error processor and also serves as the input to the pulse width modulator.

In performing the small-signal analysis of the network shown in Figure 12, the reference E_r is replaced by

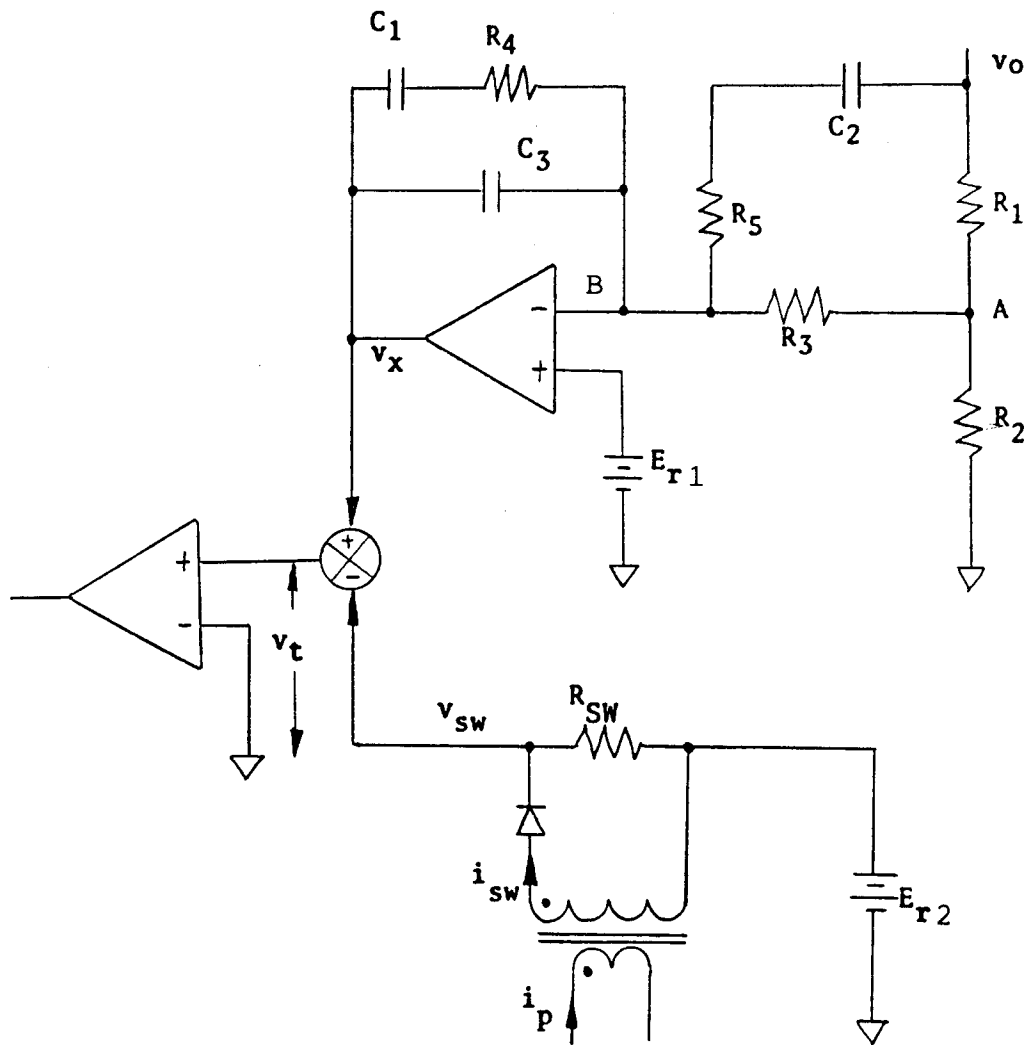


Figure 12. Equivalent Analytical Circuit of an Error Processor

a short-circuit. Applying KCL at node A yields the following equation:

$$\tilde{v}_a [(1/R_1) + (1/R_2) + (1/R_3)] = (\tilde{v}_o / R_1) + (\tilde{v}_b / R_3) \quad (34)$$

where \tilde{v}_a is the voltage across R_2 , \tilde{v}_b is the differential input voltage of the operational amplifier, and v_o is the output voltage.

Applying KCL at node B yields the following equation:

$$\begin{aligned} \tilde{v}_b [(1/Z_X) + (1/R_3) + sC_3 + (1/Z_Y)] = & \tilde{v}_x (sC_3 + 1/Z_X) + \\ & (\tilde{v}_a / R_3) + (\tilde{v}_o / Z_Y) \end{aligned} \quad (35)$$

where $Z_X = R_4 + (1/sC_1)$, and $Z_Y = R_5 + (1/sC_2)$.

The open-loop response of the operational amplifier is $A(s)$, then

$$\tilde{v}_x = -A(s) \tilde{v}_b \quad (36)$$

where $A(s) = -K / [1 + (s/w_n)]$

Substituting the above equation into the KCL equations at node A and node B results in the following set of equations:

$$\tilde{v}_a [(1/R_1) + (1/R_2) + (1/R_3)] = (\tilde{v}_o / R_1) - \tilde{v}_x [1 / (A(s)R_3)] \quad (37)$$

$$\begin{aligned} -\tilde{v}_x [(1/A(s)) (1/Z_X + 1/R_3 + sC_3 + 1/Z_Y) + (1/Z_X + sC_3)] \\ = (\tilde{v}_a / R_3) + (\tilde{v}_o / Z_Y) \end{aligned} \quad (38)$$

Eliminate the node voltages, \tilde{v}_a and \tilde{v}_b , by simultaneously solving the above two equations for \tilde{v}_o and \tilde{v}_x . The single expression generated in terms of \tilde{v}_o and \tilde{v}_x yields:

$$\begin{aligned} -\tilde{v}_x [(1/A(s)) (1/Z_X + 1/R_3 + sC_3 + 1/Z_Y) + (sC_3 + 1/Z_X)] \\ = (\tilde{v}_o/R_1R_3)(1/R_X) - [\tilde{v}_x/(A(s)R_3^2R_X)] + (\tilde{v}_o/Z_Y) \end{aligned} \quad (39)$$

where $R_X = 1/R_1 + 1/R_2 + 1/R_3$. Then,

$$\begin{aligned} -\tilde{v}_x \{ [(1/A(s)) (1/Z_X + 1/R_3 + sC_3 + 1/Z_Y)] - \\ [1/(A(s)R_3^2R_X)] \} = \tilde{v}_o \{ [1/(R_1R_3R_X)] + (1/Z_Y) \} \end{aligned} \quad (40)$$

Since the expressions for voltage and current loops are low frequency models, the operational amplifier gain is $A(s) = -K$. With a very large K , the above equation can be simplified to the following form:

$$\tilde{v}_x = -\tilde{v}_o \{ [1/(R_1R_3R_X)] + (1/Z_Y) \} / (sC_3 + 1/Z_X) \quad (41)$$

The current loop is described by the following:

$$\tilde{i}_{sw} = \tilde{i}_p/n \quad (42)$$

where n is the turns ratio of the current transformer.

$$\tilde{v}_{sw} = \tilde{i}_{sw} R_{sw} = \tilde{i}_p (R_{sw}/n) \quad (43)$$

From Figure 12 the following equation is derived:

$$\tilde{v}_t = \tilde{v}_x - \tilde{v}_{sw}$$

Then,

$$\tilde{v}_t = -\tilde{v}_o \frac{ \{ [1/(R_1 R_3 R_X)] + (1/Z_Y) \} }{ [sC_3 + (1/Z_X)] } - \tilde{i}_p (R_{SW}/n) \quad (44)$$

The voltage loop gain for the error processor is defined by the following:

$$F_V = \left. \frac{-\tilde{v}_t}{\tilde{v}_o} \right|_{\tilde{i}_p = 0}$$

$$= \frac{1}{s(C_1 + C_3)} \cdot \left[\frac{1 + sR_4 C_1}{1 + sR_4 \left(\frac{C_1 C_3}{C_1 + C_3} \right)} \right] \cdot \left[\frac{1 + sC_2 \left(\frac{R_5 GQ + 1}{GQ} \right)}{(1 + sR_5 C_2)} \right] \cdot GQ \quad (45)$$

where $GQ = 1 / \{ [1 + (R_3/R_1) + (R_3/R_2)] R_1 \}$

The current loop gain is given by the following:

$$F_C = \left. \frac{-\tilde{v}_t}{\tilde{i}_p} \right|_{\tilde{v}_o = 0}$$

$$= R_{SW}/n \quad (46)$$

Figure 13 illustrates the error processor block diagram.

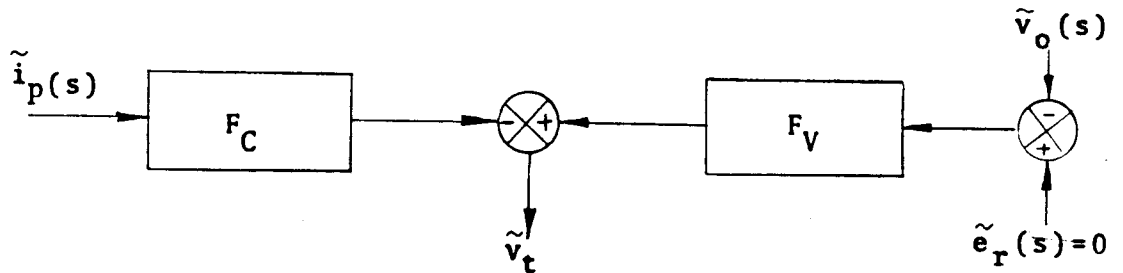


Figure 13. Error Processor Block Diagram

CHAPTER 4

PULSE WIDTH MODULATOR

4.1 Pulse Width Modulator Description

The pulse width modulator converts the analog error signal from the output of the error processor into a modulated pulse train in order to provide proper duty cycle control of the power switch. The pulse width modulator analyzed in this chapter utilizes a constant frequency duty cycle control.

A simplified block diagram of the pulse width modulator is shown in Figure 14. This pulse width modulator is compounded by the unconventional circuit implementation of the threshold detector. In the conventional design, the threshold detector is implemented with a fixed threshold voltage input and the other containing the error information. In this pulse width modulator, both inputs to the threshold detector contain error signals or modulation signals. The two inputs of the threshold detector are v_x and v_{sw} . The v_x is a floating threshold level proportional to the difference between the desired output and the measured quantity.

Using the constant frequency duty cycle control shown in Figure 14, the clock initiates the on-time and the intersection of v_{sw} and v_x marks the termination of the T_{on} interval. During the on-time interval, the slope of v_{sw} rises almost linearly with a slope S_N . The length of the

subsequent off time is determined by the next clock signal of the predetermined interval ($T_{\text{on}} + T_{\text{F1}}$).

4.2 Small-Signal Model

To investigate the small signal behavior of the pulse width modulator, an analytical model is developed by using the describing function technique.

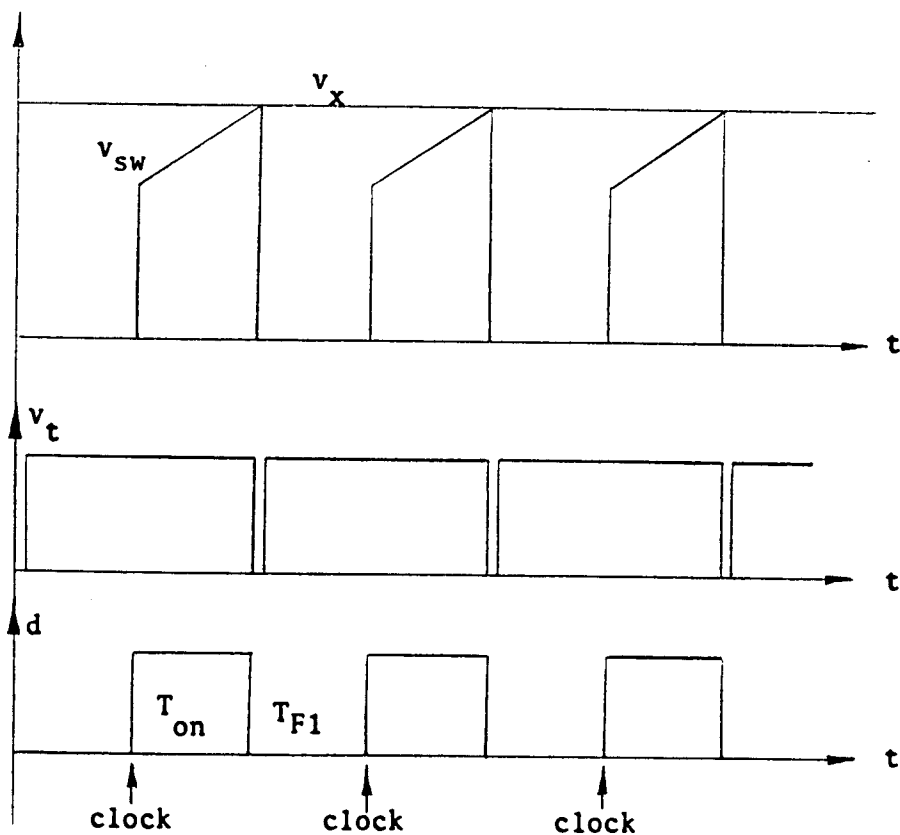
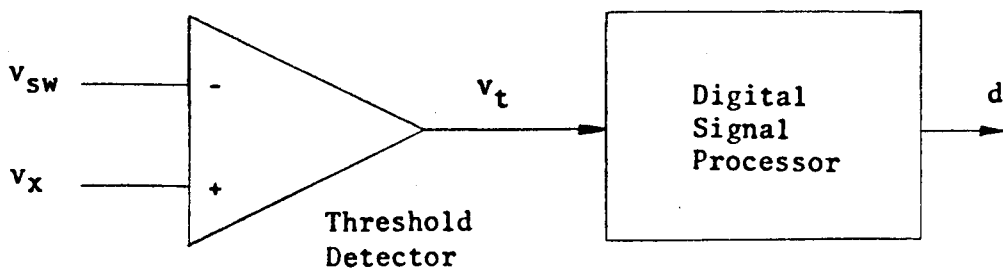


Figure 14. Pulse Width Modulator Without Disturbance

Figure 15 shows the block diagram of the analytical model at steady-state without a low frequency disturbance. When v_{sw} is greater than v_x , T_{F1} commence. S_N is the rising slope of the switching current signal v_{sw} during the T_{On} interval. S_F is the falling slope determined by the secondary current of the two winding inductor reflected back to the primary during the T_{F1} interval.

The slopes S_N and S_F can be defined by the parameters of the power stage and current sensing loop. During T_{On} interval,

$$V_i = i_p R_p + L_p (di_p/dt) \quad (47)$$

then,

$$(di_p/dt) = (V_i - i_p R_p) / L_p \quad (48)$$

The magnitude of $i_p R_p$ is much less than V_i , hence

$$(di_p/dt) \approx V_i / L_p \quad (49)$$

The current transformer used to sense the switching current reduces the sensing current by a 1:n of the turns ratio in the following expression:

$$(di_{sw}/dt) = V_i / (n L_p) \quad (50)$$

The signal v_{sw} to the threshold detector is a voltage proportional to the current passing through R_{sw} ; therefore,

$$S_N = (di_{sw}/dt) R_{sw} = (V_i R_{sw}) / (n L_p) \quad (51)$$

Because of the steady state, the initial and final values of the inductor current for each switching cycle must be equal.

Integrating the inductor voltage with time over one switching period should be zero. In other words, $S_N T_{on}$

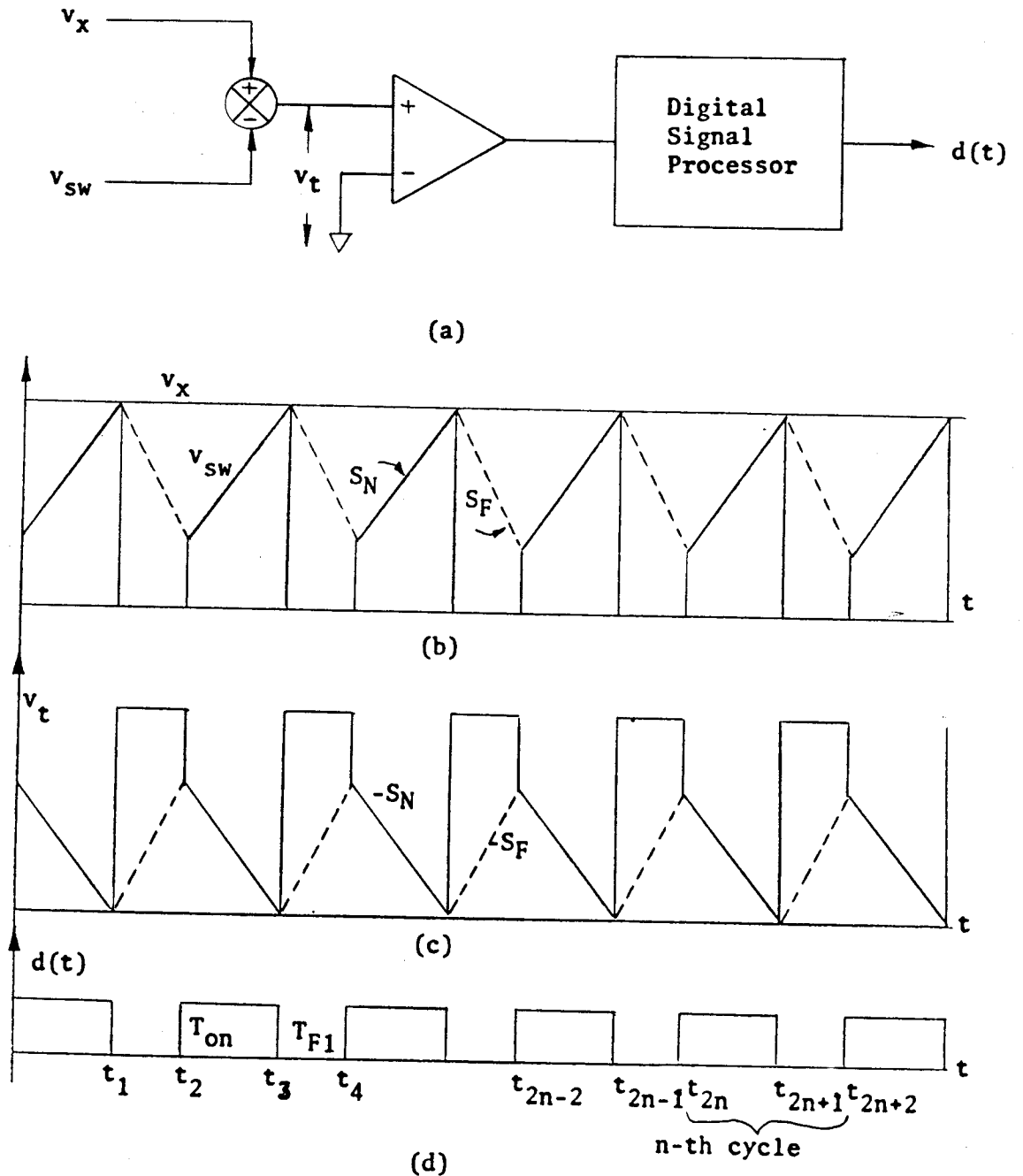


Figure 15. Unperturbed Analytical Pulse Width Modulator Waveforms

equals $-S_F T_{F1}$. This relationship is so-called volt-second balance on the inductor [6]. Thus,

$$- S_F = (T_{On} S_N) / T_{F1} = (T_{On} / T_{F1}) (V_i R_{SW}) / (n L_P) \quad (52)$$

Figure 16 shows the equivalent circuit waveforms for the perturbed case. The small signal disturbance is represented by an ac generator placed in the voltage loop as shown in Figure 16(a). For the perturbed case, the magnitude of the low frequency ac signal is assumed to be sufficiently small and S_N and S_F are considered constant and unaffected by the disturbance.

The development of Figure 16(b) is as follows: given a slope S_N determined by parameters of power stage and current sensing loop and an initial starting value with a dc value large enough to guarantee continuous operation mode. From the starting point, a line is drawn with the slope S_N . At the intersection of the perturbed v_x and the switching current information v_{sw} , T_{F1} begins. The next T_{On} will be initiated when the next clock comes, and the switching cycle repeats. The initial point for the next cycle is determined by subtracting the magnitude $S_F T_{F1}$ from v_x at that particular point in time. From the new initial values, the above process is repeated.

Figure 16(c) shows the input v_t to the analytical threshold detector. Using the relation $v_t = v_x - v_{sw}$, the waveforms in Figure 16(d) are developed and illustrated for the perturbed duty cycle.

A set of equations are developed for the darkened

trajectory v_t' of Figure 16(c). v_t' is used because the trajectory describes the low frequency modulation affecting the modulator gain. The additional information in v_t that

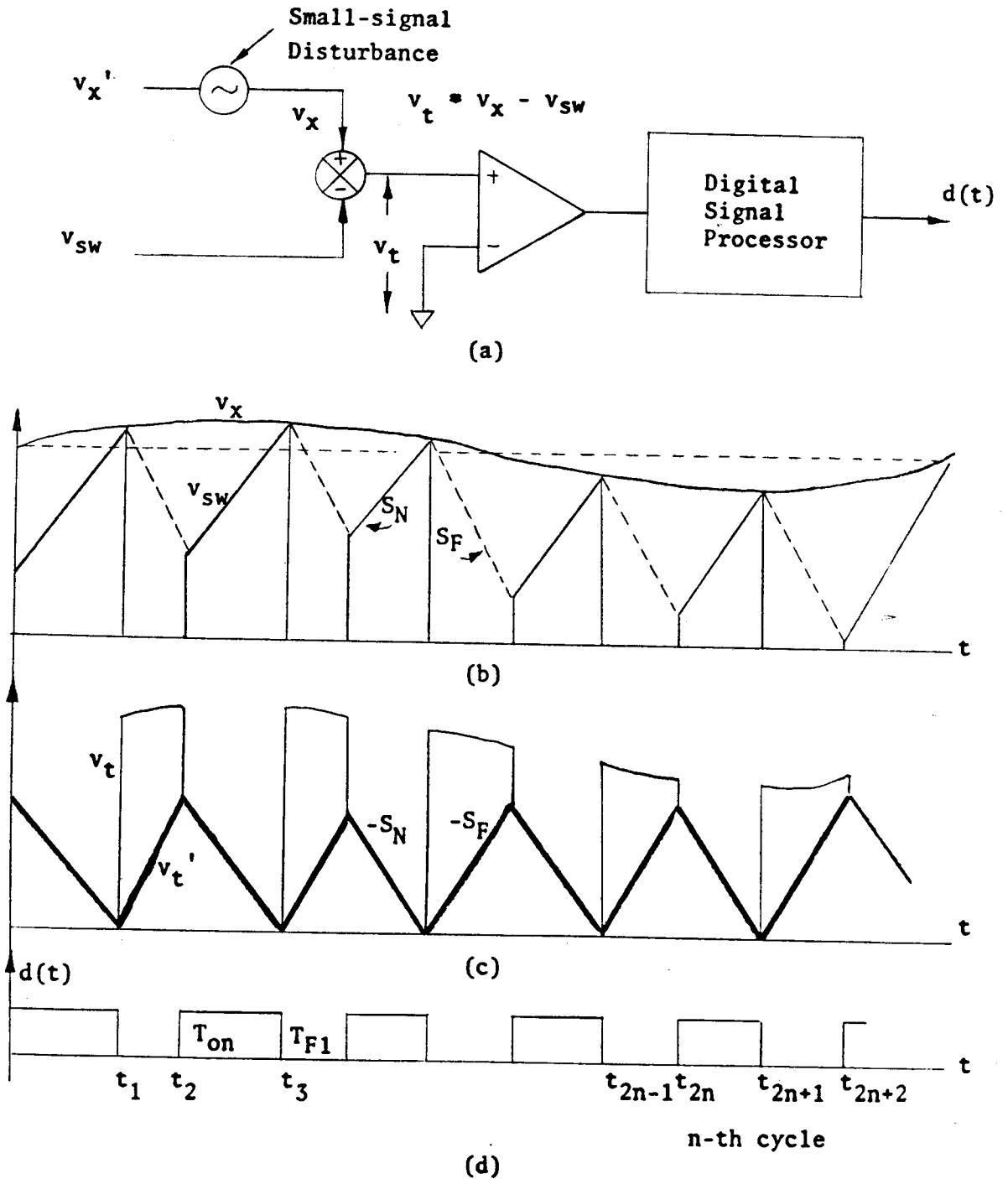


Figure 16. Perturbed Analytical Pulse Width Modulator Waveforms

deals with the dc component of the switching waveform of the converter is not relevant in the modulation of the duty cycle signal; therefore, it has no contribution to the modulator small-signal gain.

4.3 Transfer Function of Pulse Width Modulator

The output of the pulse width modulator, which contains a series of pulses of equal amplitude but sinusoidally-varying pulse widths, will have a low frequency content corresponding to the small-signal disturbance frequency. The output of the pulse width modulator can be expressed in a Fourier series in the form:

$$d(t) = D + a_1 \sin \omega t + b_1 \cos \omega t + \dots \quad (53)$$

The input of the pulse width modulator can also be expressed in a Fourier series in the form:

$$v_t'(t) = V + c_1 \sin \omega t + d_1 \cos \omega t + \dots \quad (54)$$

Because the low frequency contents of $v_t'(t)$ and $d(t)$ are of concern, the describing function F_M of the pulse width modulator is defined as:

$$F_M = \frac{\tilde{d}(t)}{\tilde{v}_t'(t)} = \frac{(a_1^2 + b_1^2)^{1/2}}{(c_1^2 + d_1^2)^{1/2}} \frac{\sin [\omega t + (\tan^{-1} b_1/a_1)]}{\sin [\omega t + (\tan^{-1} d_1/c_1)]} \quad (55)$$

The resultant waveform v_t' is a function of S_N and S_F and the sinusoidal disturbance $A \sin \omega t$. During the interval T_{on} at the n -th cycle $\{ t_{2n}, t_{2n+2} \}$, v_t' yields the

following equation:

$$v_t'(t) = |S_N| (t_{2n+1} - t) + A \sin \omega t - A \sin \omega t_{2n+1} \quad (56)$$

During the interval T_{F1} at the $n-1$ cycle, v_t' results in the following:

$$v_t'(t) = |S_F| (t - t_{2n-1}) + A \sin \omega t - A \sin \omega t_{2n-1} \quad (57)$$

The switching period, T_p , can be found from the following development. Evaluating the above equations, $v_t'(t)$, at $t = t_{2n}$ gives the following:

$$v_t'(t_{2n}) = |S_F| (t_{2n} - t_{2n-1}) + A \sin \omega t_{2n} - A \sin \omega t_{2n-1} \quad (58)$$

and

$$v_t'(t_{2n}) = |S_N| (t_{2n+1} - t_{2n}) + A \sin \omega t_{2n} - A \sin \omega t_{2n+1} \quad (59)$$

Then,

$$|S_F| T_{F1} + A \sin \omega t_{2n} - A \sin \omega t_{2n-1} = |S_N| (T_p - T_{F1}) + A \sin \omega t_{2n} - A \sin \omega t_{2n+1} \quad (60)$$

where $T_{F1} = t_{2n} - t_{2n-1}$, $T_p = t_{2n+1} - t_{2n-1}$, $(t_{2n+1} - t_{2n}) = (T_p - T_{F1})$

Therefore,

$$(|S_F| + |S_N|) T_{F1} - |S_N| T_p = -2A \sin \omega (T_p/2) \cos \omega (t_{2n-1} + T_p/2) \quad (61)$$

Making use of the fact that ωT_p is very small,

$$\sin \omega (T_p/2) \approx \omega (T_p/2) \quad (62)$$

$$\cos \omega (t_{2n-1} + T_p/2) \approx \cos \omega t_{2n-1} \quad (63)$$

Thus,

$$(|S_F| + |S_N|) T_{F1} = T_p (|S_N| - A \omega \cos \omega t_{2n-1}) \quad (64)$$

$$T_p = [(|S_F| + |S_N|)T_{F1}] / [|S_N| - A w \cos wt_{2n-1}] \quad (65)$$

4.3.1 Derivation of Coefficients a_1 and b_1

The coefficient b_1 can be derived as:

$$\begin{aligned} b_1 &= w/\pi \int_0^{2\pi} d(t) \cos wt \, dt \\ &= w/\pi \left(\int_0^{t_1} \cos wt \, dt + \int_{t_2}^{t_3} \cos wt \, dt + \dots \right) \\ &= 1/\pi [\sin wt_1 + \sin wt_3 - \sin wt_2 + \dots \\ &\quad + \sin wt_{2n+1} - \sin wt_{2n} + \dots] \\ &= 1/\pi \sum_{n=0}^N B_{2n+1} \end{aligned} \quad (66)$$

where

$$\begin{aligned} B_{2n+1} &= \sin wt_{2n+1} - \sin wt_{2n} \\ &= 2 \cos [w(t_{2n+1} + t_{2n})/2] \sin [w(t_{2n+1} - t_{2n})/2] \\ &= 2 \cos [w(t_{2n-1} + (T_p + T_{F1})/2)] \sin [w(T_p - T_{F1})/2] \end{aligned} \quad (67)$$

Making use of the fact that wT_p is very small,

$$\sin [w(T_p - T_{F1})/2] \approx w(T_p - T_{F1})/2 \quad (68)$$

$$\cos [w(t_{2n-1} + (T_p + T_{F1})/2)] \approx \cos wt_{2n-1} \quad (69)$$

Thus,

$$\begin{aligned} B_{2n+1} &\approx w(T_p - T_{F1}) \cos wt_{2n-1} \\ &= w/T_p [(T_p - T_{F1}) \cos wt_{2n-1}] T_p \end{aligned} \quad (70)$$

Therefore,

$$b_1 = 1/\pi \left\{ \sum_{n=0}^N w/T_p [(T_p - T_{F1}) \cos wt_{2n-1}] T_p \right\} \quad (71)$$

With T_p small compared to the modulation period, $2\pi/w$, b_1 can be expressed as follows:

$$b_1 = \frac{1}{\pi} \int_0^{2\pi/w} w [1 - (T_{F1}/T_p)] \cos wt \, dt \quad (72)$$

Since $T_p = [(|S_F| + |S_N|)T_{F1}] / [|S_N| - Aw \cos wt_{2n-1}]$, hence

$$\begin{aligned} b_1 &= \frac{1}{\pi} \int_0^{2\pi/w} w \left[1 - \frac{T_{F1} [|S_N| - Aw \cos wt]}{[(|S_F| + |S_N|) T_{F1}]} \right] \cos wt \, dt \\ &= \frac{w}{\pi} \int_0^{2\pi/w} \{ [A w (\cos wt)^2] / [|S_F| + |S_N|] \} dt \\ &= \{ (A w^2) / [2 (|S_F| + |S_N|)] \} \int_0^{2\pi/w} (\cos 2wt + 1) \, dt \\ &= (A w) / (|S_F| + |S_N|) \end{aligned} \quad (73)$$

The coefficient a_1 can be derived as:

$$\begin{aligned} a_1 &= \frac{w}{\pi} \int_0^{2\pi} d(t) \sin wt \, dt \\ &= \frac{w}{\pi} \left(\int_0^{t_1} \sin wt \, dt + \int_{t_2}^{t_3} \sin wt \, dt + \dots \right) \\ &= \frac{1}{\pi} [1 - \cos wt_1 + \cos wt_2 - \cos wt_3 + \dots] \\ &= \frac{1}{\pi} \sum_{n=0}^N A_{2n+1} \end{aligned} \quad (74)$$

where

$$\begin{aligned} A_{2n+1} &= \cos wt_{2n} - \cos wt_{2n+1} \\ &= 2 \sin [w(t_{2n} + t_{2n+1})/2] \sin [w(t_{2n+1} - t_{2n})/2] \\ &= 2 \sin [w(t_{2n-1} + (T_p + T_{F1})/2)] \sin [w(T_p - T_{F1})/2] \end{aligned} \quad (75)$$

Making use of the fact that wT_p is very small,

$$\sin [w(T_p - T_{F1})/2] \approx w(T_p - T_{F1})/2 \quad (76)$$

$$\sin [w(t_{2n-1} + (T_p + T_{F1})/2)] \approx \sin wt_{2n-1} \quad (77)$$

Thus,

$$\begin{aligned} A_{2n+1} &\approx w (T_p - T_{F1}) \sin wt_{2n-1} \\ &= (w/T_p) [(T_p - T_{F1}) \sin wt_{2n-1}] T_p \end{aligned} \quad (78)$$

Therefore,

$$a_1 = 1/\pi \sum_{n=0}^N \{ (w/T_p) [(T_p - T_{F1}) \sin wt_{2n-1}] T_p \} \quad (79)$$

With T_p small compared to the modulation period, $2\pi/w$, a_1 can be expressed as follows:

$$a_1 = 1/\pi \int_0^{2\pi/w} w [1 - (T_{F1}/T_p)] \sin wt \, dt \quad (80)$$

Since $T_p = [(|S_F| + |S_N|)T_{F1}] / [|S_N| - A w \cos wt_{2n-1}]$, hence

$$\begin{aligned} a_1 &= 1/\pi \int_0^{2\pi/w} w \left[1 - \frac{T_{F1} [|S_N| - A w \cos wt]}{(|S_F| + |S_N|)T_{F1}} \right] \sin wt \, dt \\ &= w/\pi \int_0^{2\pi/w} [(A w) / (|S_F| + |S_N|)] \cos wt \sin wt \, dt \\ &= 0 \end{aligned} \quad (81)$$

4.3.2 Derivation of Coefficient c_1 and d_1

From Figure 16, one has v_t' at $t = t_{2n}$ as:

$$v_t'(t_{2n}) = |S_F| T_{F1} - A \sin wt_{2n-1} + A \sin wt_{2n}$$

$$= |S_F|T_{F1} + 2A \cos [w(t_{2n} + t_{2n-1})/2] \sin wT_{F1}/2 \quad (82)$$

Since $wT_{F1}/2$ is very small,

$$\sin wT_{F1}/2 \approx wT_{F1}/2 \quad (83)$$

Thus,

$$v_t' \approx |S_F|T_{F1} + A w T_{F1} \cos w[t_{2n-1} + (T_{F1}/2)] \quad (84)$$

From the above equation, the fundamental of the small-signal average of v_t' can be taken.

$$\tilde{v}_t' \approx 1/2 A w T_{F1} \cos [w (t + T_{F1}/2)] \quad (85)$$

The describing function F_M for the pulse width modulator is:

$$F_M = \frac{\tilde{d}(t)}{\tilde{v}_t'} = \frac{(a_1^2 + b_1^2)^{1/2}}{\tilde{v}_t'} \sin \{wt + [\tan^{-1}(b_1/a_1)]\} \quad (86)$$

Substituting for a_1 , b_1 and \tilde{v}_t' into the equation F_M , the gain of the pulse width modulator is:

$$F_M = \frac{2 \sin [wt + \pi/2]}{(|S_N| + |S_F|)T_{F1} \cos [w (t + T_{F1}/2)]} \quad (87)$$

Since w is the angular frequency of the low-frequency modulation and T_{F1} is the off-time period of the switch, thus

$$wT_{F1}/2 \ll 1$$

and

$$\frac{\sin [wt + \pi/2]}{\cos [w (t + T_{F1})]} = \frac{\cos wt}{\cos [w (t + T_{F1})]} \approx 1 \quad (88)$$

$$F_M \approx 2 / [(|S_N| + |S_F|) T_{F1}] \quad (89)$$

Because

$$|S_N| = \frac{V_i R_{SW}}{n L_p} \quad (90)$$

$$|S_F| = \frac{T_{On} V_i R_{SW}}{T_{F1} n L_p} \quad (91)$$

Therefore,

$$F_M \approx \frac{2 n L_p}{V_i R_{SW} T_p} \quad (92)$$

Figure 17 is the block diagram for the small-signal gain from the composite error signal, \tilde{v}_t , to the pulse width modulator output, \tilde{d} .

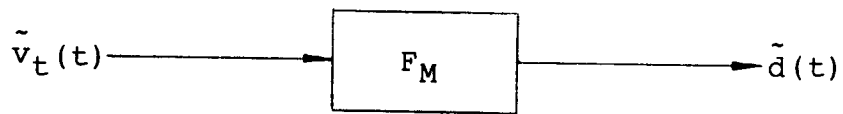


Figure 17. Pulse Width Modulator Block

CHAPTER 5

SIMULATION

5.1 Introduction

Simulation of a physical system is a standard analysis tool used in the evaluation of hardware design prior to actual construction. Even though the small-signal model or a mathematic model of a system is developed, examining the performance characteristics of that system without a computer becomes a tedious and time consuming task. In the case of the complicated model, calculations by hand are impossible.

Because the small-signal model of this fly-back switching power supply is derived by using s-plane or Laplace transform techniques, this model can be expressed by a set of linear transfer functions or linear equations. Many computer program packages designed to solve any linear equations and transfer functions are available now. Among those packages for solving such a problem is "LISA 360 A Program for Linear System Analysis (LISA 360)", a well-known computer program package developed by IBM. The LISA 360 program package can be used to compute the following solutions:

- (a) Pole and zero locations
- (b) Time response to a step or sinusoidal inputs
- (c) Bode response over a range of frequencies
- (d) Sensitivity of a function to component variations

at a given frequency

A LISA 360 program has been coded to examine the following performance characteristics of this power supply model:

- (1) The audio-susceptibility characteristics $G_A = \tilde{v}_O / \tilde{v}_i$
- (2) The output impedance characteristics $Z_O = \tilde{v}_O / \tilde{i}_O$
- (3) The system loop gain characteristics [7]

$$T = \frac{1}{\Delta} F_M (F_V F_{D1} + F_C F_{D2}) \quad (93)$$

The system loop gain characteristics T are used to examine the relative stability of the system.

5.2 Simulations of Audio-Susceptibility and Output Impedance

Audio-susceptibility [8] is the closed-loop, input/output response for the switching power supply. The audio-susceptibility characteristic is used to evaluate the rejection ratio of the propagation of a sinusoidal disturbance from the input voltage to the output voltage. The audio-susceptibility is defined as:

$$G_A = \tilde{v}_O / \tilde{v}_i \quad (94)$$

The output impedance is employed to measure the dynamic performance of a switching power supply subjected to sinusoidal load disturbance. A switching power supply with zero output impedance represents an ideal voltage source. The output impedance of the switching power supply is defined as:

$$Z_O = \tilde{v}_O / \tilde{i}_O \quad (95)$$

In linear systems, the output impedance is often used to analyze transient response. When a switching power supply is subjected to a small step-change of the load, the output voltage normally only varies slightly.

5.2.1 Equation Formulations

Many methods can be used to set up the describing equations of the small-signal model of this switching power supply. One of the equation formulations, which LISA 360 program package uses, is the "matrix" option. According to the input language of LISA 360, the system equations should be written in the following form if the "matrix" option is used.

$$W(s) Y(s) = U(s) \quad (96)$$

where $W(s)$ is the nodal admittance matrix or the system dynamics, $Y(s)$ is the unknown node-voltage or output vector, and $U(s)$ is the vector of sources plus initial conditions.

From the previous chapters, the fly-back power stage, error processor, and pulse width modulator small-signal model can be incorporated into a closed-loop block diagram as shown in Figure 18. The input-output equations are derived as follows:

$$\tilde{Y}(s) = \left\{ \begin{bmatrix} F_{U11} & F_{U12} \\ F_{U21} & F_{U22} \end{bmatrix} \begin{bmatrix} \tilde{v}_i(s) \\ \tilde{i}_o(s) \end{bmatrix} + \begin{bmatrix} F_{D1} \\ F_{D2} \end{bmatrix} \tilde{d}(s) \right\} \frac{1}{\Delta} = \begin{bmatrix} \tilde{v}_o(s) \\ \tilde{i}_p(s) \end{bmatrix} \quad (97)$$

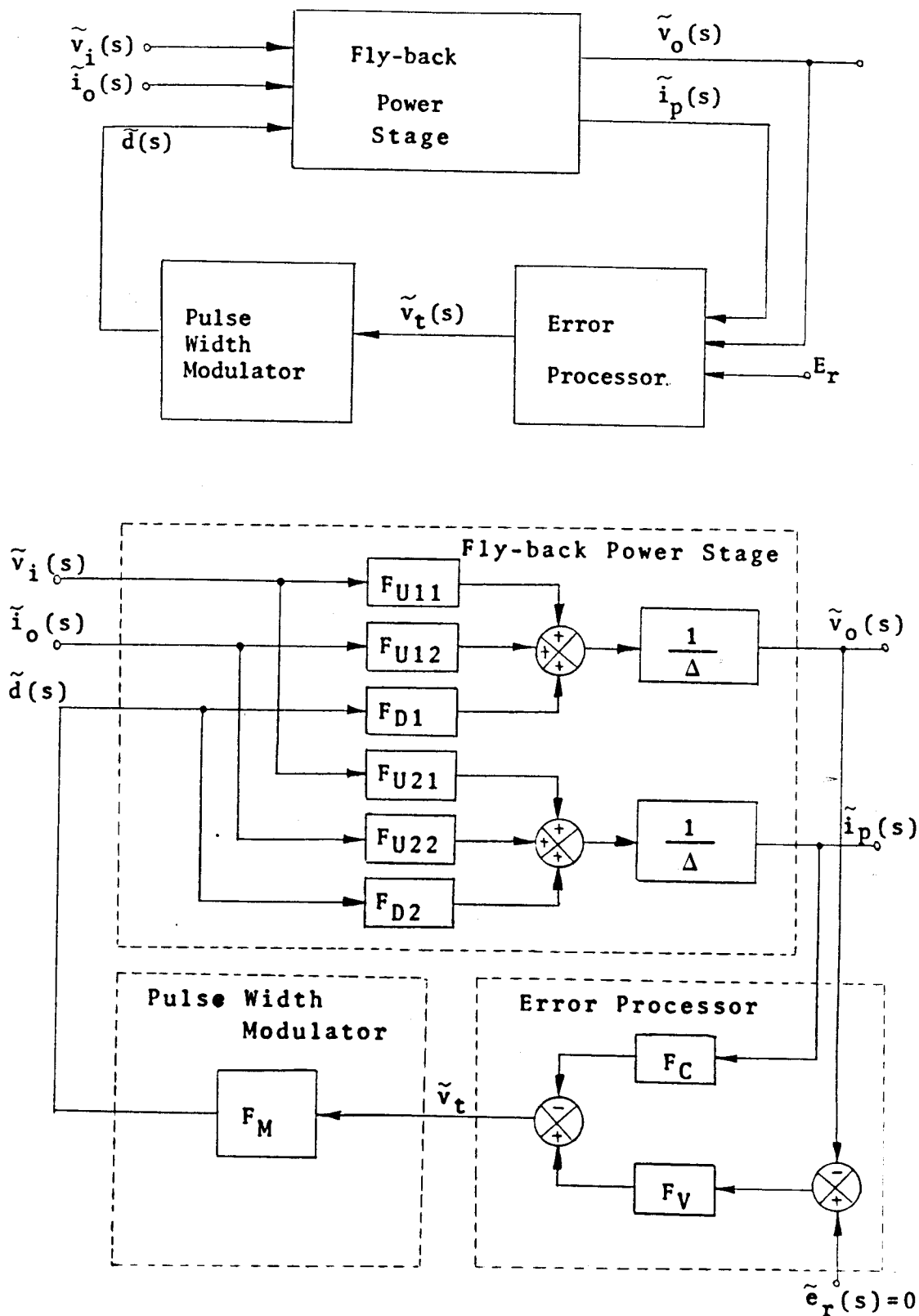


Figure 18. Small-signal Block Diagram of a Fly-back Switching Mode Power Supply

$$\Delta \tilde{Y}(s) = \begin{bmatrix} F_{U11} & F_{U12} \\ F_{U21} & F_{U22} \end{bmatrix} \begin{bmatrix} \tilde{v}_i(s) \\ \tilde{i}_o(s) \end{bmatrix} - \begin{bmatrix} F_{D1} \\ F_{D2} \end{bmatrix} F_M [F_V \ F_C] \tilde{Y}(s) \quad (98)$$

$$\left\{ \Delta I + \begin{bmatrix} F_{D1} \\ F_{D2} \end{bmatrix} F_M [F_V \ F_C] \right\} \tilde{Y}(s) = \begin{bmatrix} F_{U11} & F_{U12} \\ F_{U21} & F_{U22} \end{bmatrix} \begin{bmatrix} \tilde{v}_i(s) \\ \tilde{i}_o(s) \end{bmatrix} \quad (99)$$

Therefore,

$$\begin{bmatrix} \Delta + F_{D1}F_VF_M & F_{D1}F_C F_M \\ F_{D2}F_VF_M & \Delta + F_{D2}F_C F_M \end{bmatrix} \begin{bmatrix} \tilde{v}_o(s) \\ \tilde{i}_p(s) \end{bmatrix} = \begin{bmatrix} F_{U11} & F_{U12} \\ F_{U21} & F_{U22} \end{bmatrix} \begin{bmatrix} \tilde{v}_i(s) \\ \tilde{i}_o(s) \end{bmatrix} \quad (100)$$

Note that the negative power of s is not allowed in LISA 360, so the equations must be rationalized. Thus,

$$\begin{bmatrix} D(s) [\Delta + F_{D1}F_VF_M] & D(s) [F_{D1}F_C F_M] \\ D(s) [F_{D2}F_VF_M] & D(s) [\Delta + F_{D2}F_C F_M] \end{bmatrix} \begin{bmatrix} \tilde{v}_o(s) \\ \tilde{i}_p(s) \end{bmatrix} = \begin{bmatrix} D(s) F_{U11} \\ D(s) F_{U21} \end{bmatrix} \tilde{v}_i(s) \quad (101)$$

assume that $\tilde{i}_o(s) = 0$.

$$\begin{bmatrix} D(s) [\Delta + F_{D1}F_VF_M] & D(s) [F_{D1}F_C F_M] \\ D(s) [F_{D2}F_VF_M] & D(s) [\Delta + F_{D2}F_C F_M] \end{bmatrix} \begin{bmatrix} \tilde{v}_o(s) \\ \tilde{i}_p(s) \end{bmatrix} = \begin{bmatrix} D(s) F_{U12} \\ D(s) F_{U22} \end{bmatrix} \tilde{i}_o(s) \quad (102)$$

assume that $\tilde{v}_i(s) = 0$.

where $D(s) = s [1 + (sR_4 C_1 C_3) / (C_1 + C_3)] (1 + sR_5 C_2)$

The form of the above equations meets the input requirement of LISA 360 for the matrix option. Once the power supply parameters and operating conditions are given, each coefficient in the nonzero elements of the above matrices must be calculated. Then, following the command descriptions and directions, each nonzero element of the matrices should be coded into the LISA simulation program.

5.2.2 Simulation Results of Audio-susceptibility and Output Impedance

A Bode plot establishing the gain and phase of each particular transfer function is shown. The gain and phase plots for the audio-susceptibility and output impedance analysis employ the following power supply parameters and operating conditions. The simulation can be performed by substituting these parameters into equation (101) and (102).

$V_i = 130V$	$C_1 = 0.06\mu F$
$V_o = 6V$	$C_2 = 0$
$R_p = 0.3 \text{ ohm}$	$C_3 = 120pF$
$N_p = 68 \text{ Turns}$	$R_1 = 1K \text{ ohm}$
$N_s = 3 \text{ Turns}$	$R_2 = 5K \text{ ohm}$
$R_s = 0.01 \text{ ohm}$	$R_3 = 4.7K \text{ ohm}$
$R_c = 0.0175 \text{ ohm}$	$R_4 = 22K \text{ ohm}$
$C = 1880\mu F$	$R_5 = 0$
$R_L = 0.75 \text{ ohm}$	$R_{SW} = 250 \text{ ohm}$
$T_p = 16.67\mu S$	$n = 120 \text{ Turns}$
$L_p = 2.929mH$	$D = 0.5$
$L_s = 6.239\mu H$	$D' = 0.5$

Figure 19 illustrates the Bode plot for audio-susceptibility, and Figure 20 illustrates the Bode plot for output impedance. Moreover, the detailed expressions for calculation of coefficients in each element of matrices, a FORTRAN program designed to accept the circuit parameters and then to calculate those coefficients, and the LISA

AUDIOSUSCEPTIBILITY = VO/VI

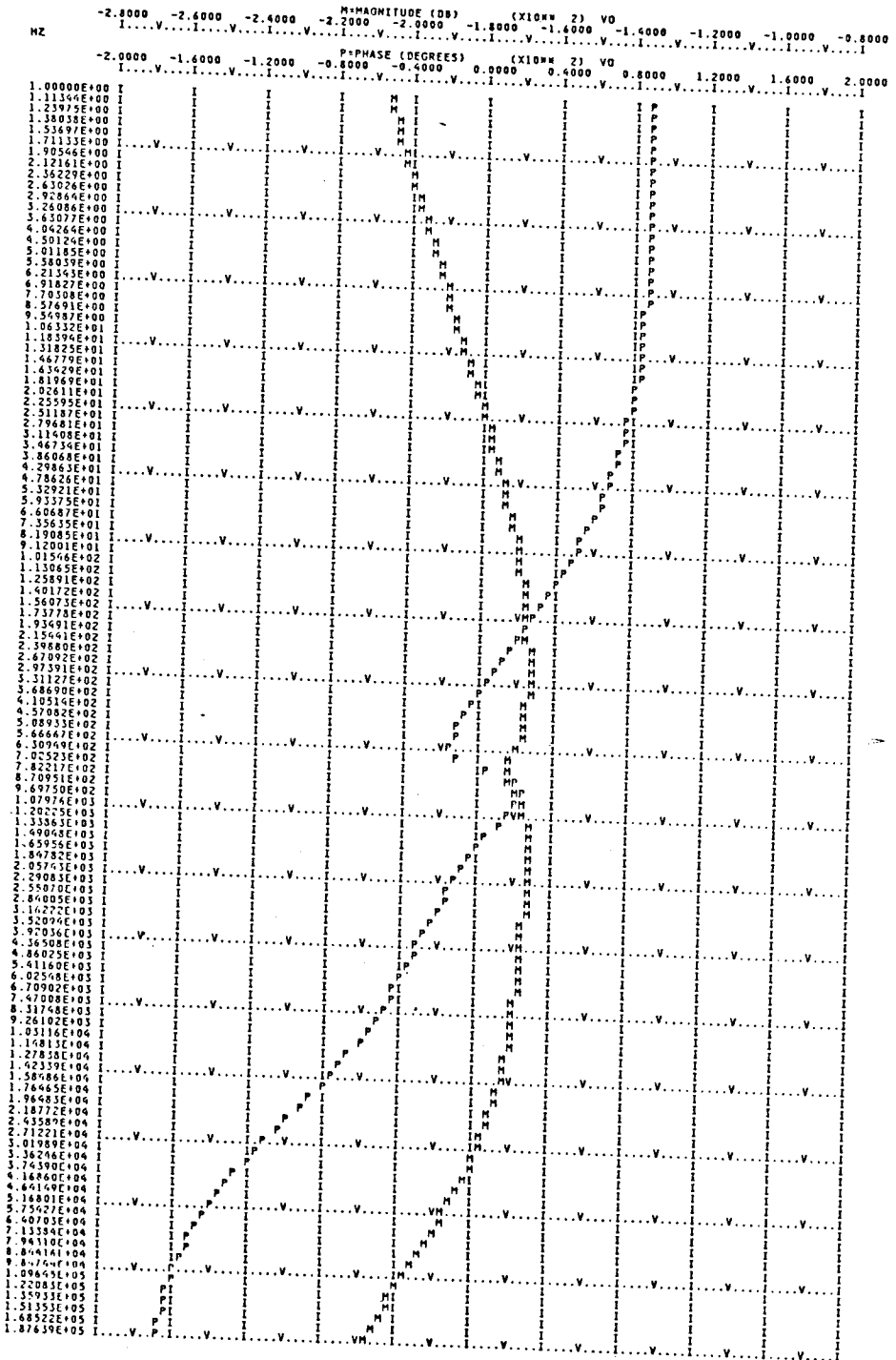


Figure 19. Bode Plot for Audio-susceptibility

OUTPUT IMPEDANCE = VO/I0

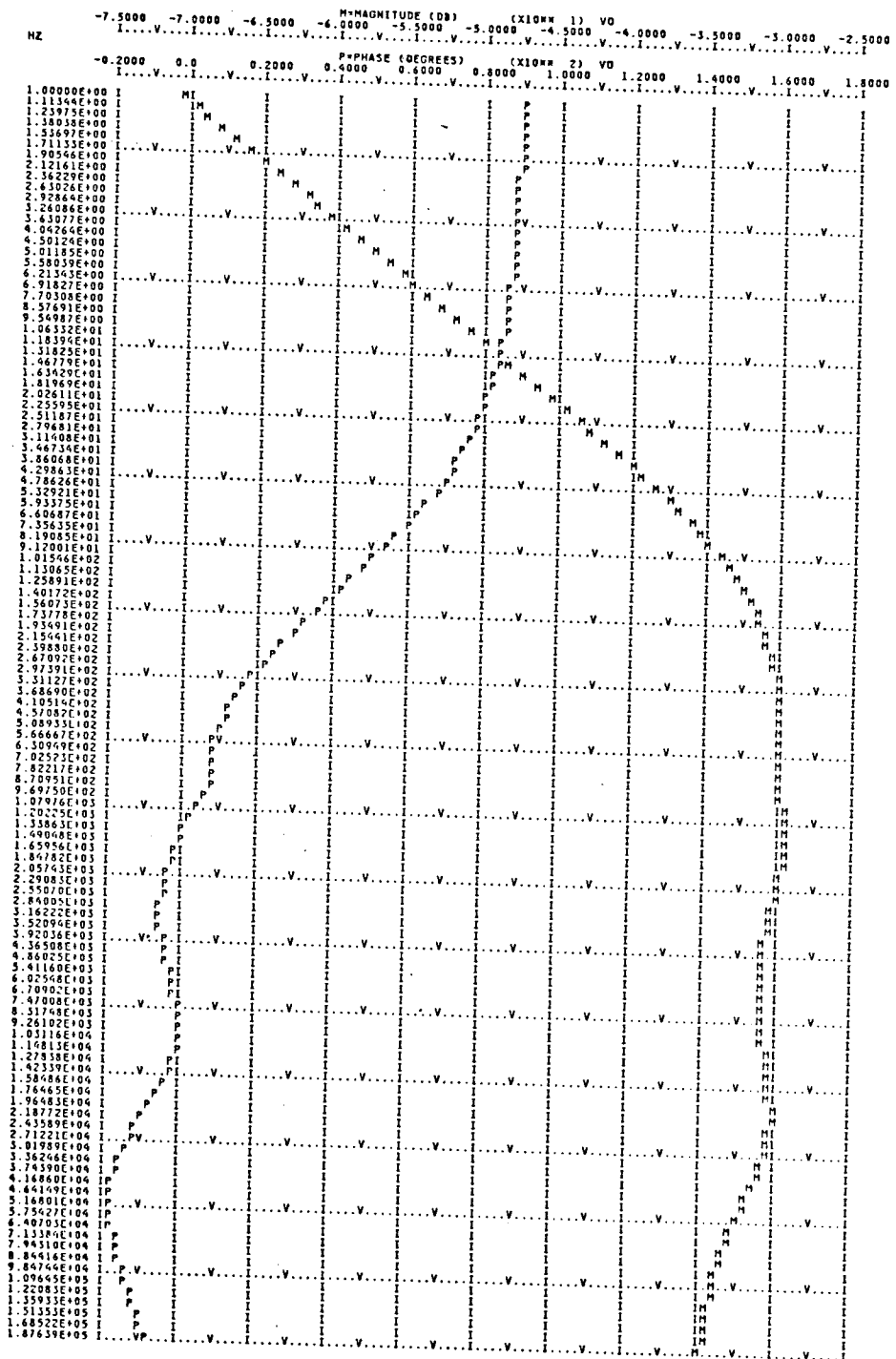


Figure 20. Bode Plot for Output Impedance
 Note that $Z_0 (\Omega) = \text{Anti-log} [M (\text{DB}) / 20]$

simulation program are presented in Appendix C.

5.3 The System Loop Gain Characteristics

The system loop gain characterizes the power supply's stability. Because of the multiple feedback paths of this power supply, the loop gain that is defined at the pulse width modulator, which is the common part to all the feedback paths, is a unique loop. Figure 21 shows the block diagram for the system loop gain, and the equation of the system loop gain can be derived. The resultant equation is given below:

$$T = \frac{1}{\Delta} F_M (F_V F_{D1} + F_C F_{D2}) \quad (103)$$

Substituting the circuit parameters and operating conditions of power supply into the above equation, each coefficient in the numerator and the denominator of the system loop gain, T , can be obtained. Then, according to the command description and direction of "READ function name" in LISA 360, those coefficients are coded into the LISA simulation program. The detailed expression and LISA program are shown in Appendix C.

After simulation, the pole and zero locations of the system loop gain are given below:

Zeros:

$$\begin{array}{ll} -7.311477E2 & -9.394725E4 + j1.356394E5 \\ -1.578442E4 & -9.394725E4 - j1.356394E5 \end{array}$$

Poles:

0.0	-1.857252E3 + j4.226668E3
-3.795455E5	-1.857252E3 - j4.226668E3

Total multiplier = 1.90810

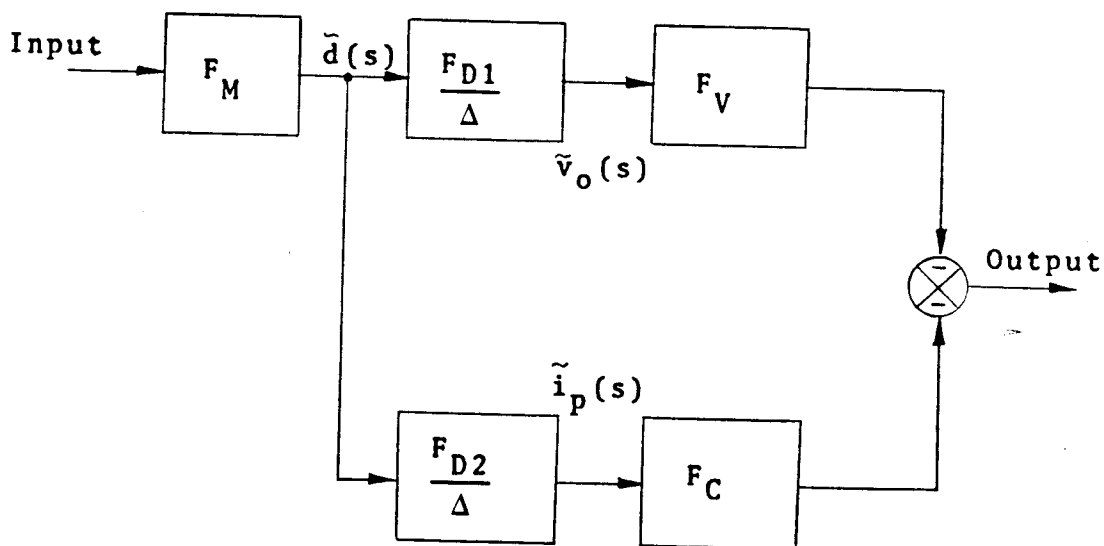


Figure 21. Block Diagram for The System Loop Gain

Figure 22 shows the Bode plot of the system loop gain. From this plot, it is interesting to point out that high gain, wide-bandwidth, and stable operation could be accomplished simultaneously. This characteristic has made the multiple

loop control unique in comparison with the single loop control in switching mode power supply.

THE SYSTEM LOOP GAIN = TS

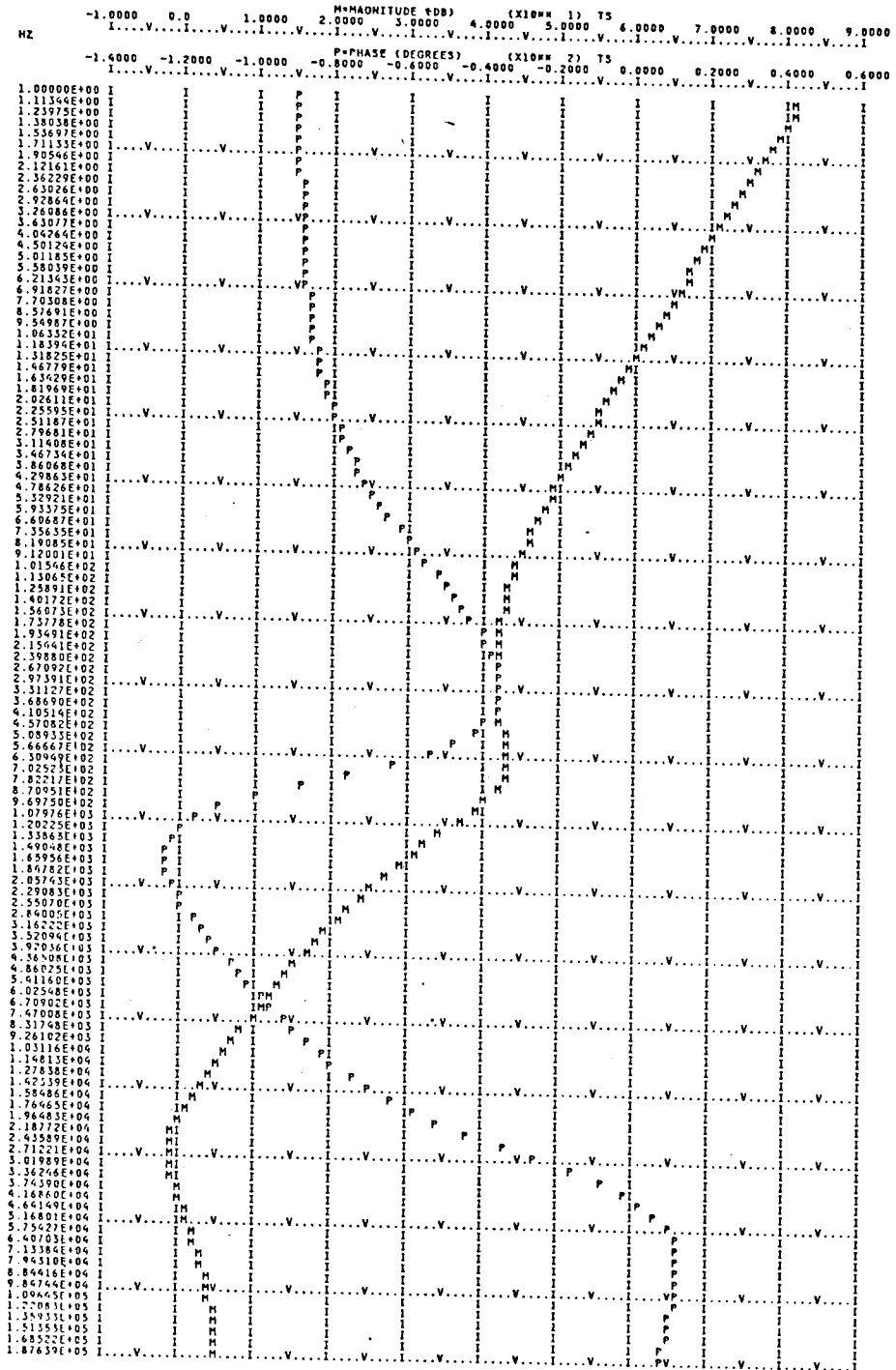


Figure 22. Bode Plot for The System Loop Gain

CHAPTER 6

MEASUREMENT

6.1 Loop Gain Measurement And Analog Modulation Technique[9]

To analyze the dynamics of a switching mode power supply, the system loop gain method has been widely used because the system loop gain can directly compute the characteristic roots of the system. It is easy to derive the loop gain of a system from a system block diagram or an equivalent circuit model, and the loop gain can provide physical insight into the closed loop system. The stability can be determined by applying the Nyquist criterion, and it is easy to shape the Bode Plots of the loop gain for design purposes to achieve better stability and dynamics of a system.

Even though the most attractive feature is that the loop gain can be measured accurately and quickly in laboratory, the conventional measuring method still has some difficulties to perform within a switching mode power supply employing multi-loop control. For this power supply, loop gains become rather complicated functions, and each loop gain is not uniquely defined. Therefore, the adequacy and accuracy of the loop gain measurement become a very important concern.

The conventional loop gain measurement technique, analog modulation scheme, has been widely used in various types of linear feedback system. In the analog modulation

scheme, a sinusoidal disturbance signal, V_z , is inserted in the feedback loop and the forward and returned signals, V_x and V_y respectively, are measured as shown in Figure 23. The loop gain is then determined by the ratio of the forward and returned signals at the frequency of the inserted signal.

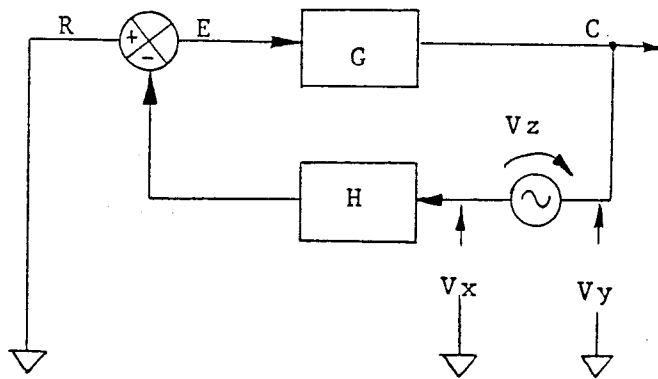


Figure 23. Conventional Analog Modulation Scheme

Because the analog modulation technique inserts and measures the analog signal, its application is limited to the case for which the waveform of the disturbance is smooth and well behaved. In the switching mode power supply, the waveform of the disturbance is of a discontinuous nature and is pulse width modulated. In this case, an analog disturbance signal cannot be inserted into the digital signal for loop gain measurement. In addition, when a PWM ripple component from the ESR of the output filter capacitors is superimposed on the inserted sinusoidal disturbance, the analog modulation scheme gives inaccurate results.

6.2 Consideration of Loop Gain Measurement in Switching Power Supply

In the switching power supply employing multiple loop control, not only the derivations of the loop gain are complex, but also the interpretations of the loop gain are not obvious as for a single loop system. However, switching power supply feedback systems are unique in that because the duty cycle is the only control input, all the feedback loops must meet at one point, the duty cycle modulator. The loop gain that is defined at the duty cycle modulator is a unique loop in this multiple loop switching power supply.

6.3 Digital Modulation Technique

The conventional analog modulation scheme has some limitations when a sinusoidal disturbance is inserted into the feedback loop at the point where the waveform is not smooth and well behaved. These limitations can be overcome by inserting, instead, a digital modulation signal that directly modulates the switching power supply's duty cycle. Similar to the analog modulation technique in which a disturbance signal is inserted in the feedback path to generate the forward and returned signals, the digital modulator inserts a digitally modulated disturbance, dz , into the digital signal feedback path while maintaining the loop closed, as shown in Figure 24. Then the KVL satisfies

$$dz = dx + dy \tag{104}$$

and the loop gain is given by: $T = dy / dx$

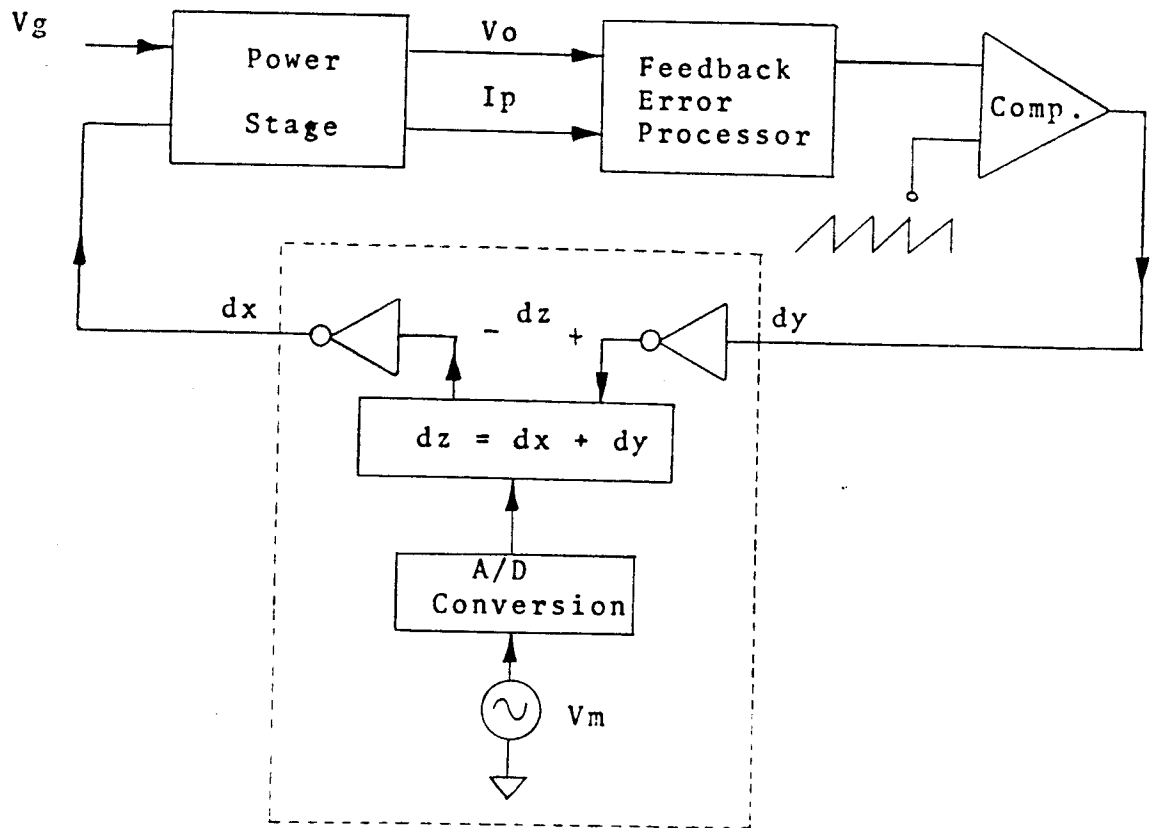


Figure 24. Digital Modulation Scheme

6.3.1 The Digital Modulator

The schematic for the digital modulator is shown in Figure 25. The functional description with the important waveforms in Figure 26 is given as follows.

The modulator accepts one or two inputs, dy_A and dy_B , depending on whether the duty cycle modulator under test is single-ended or push-pull. These signals are buffered by comparators IC_1 and IC_2 which invert and wire-or the inputs. When either of the inputs go high, JK flip-flop IC_{3a} and IC_{7b} are clocked and set. The inverted output of these flip-flops are the input to the open collector

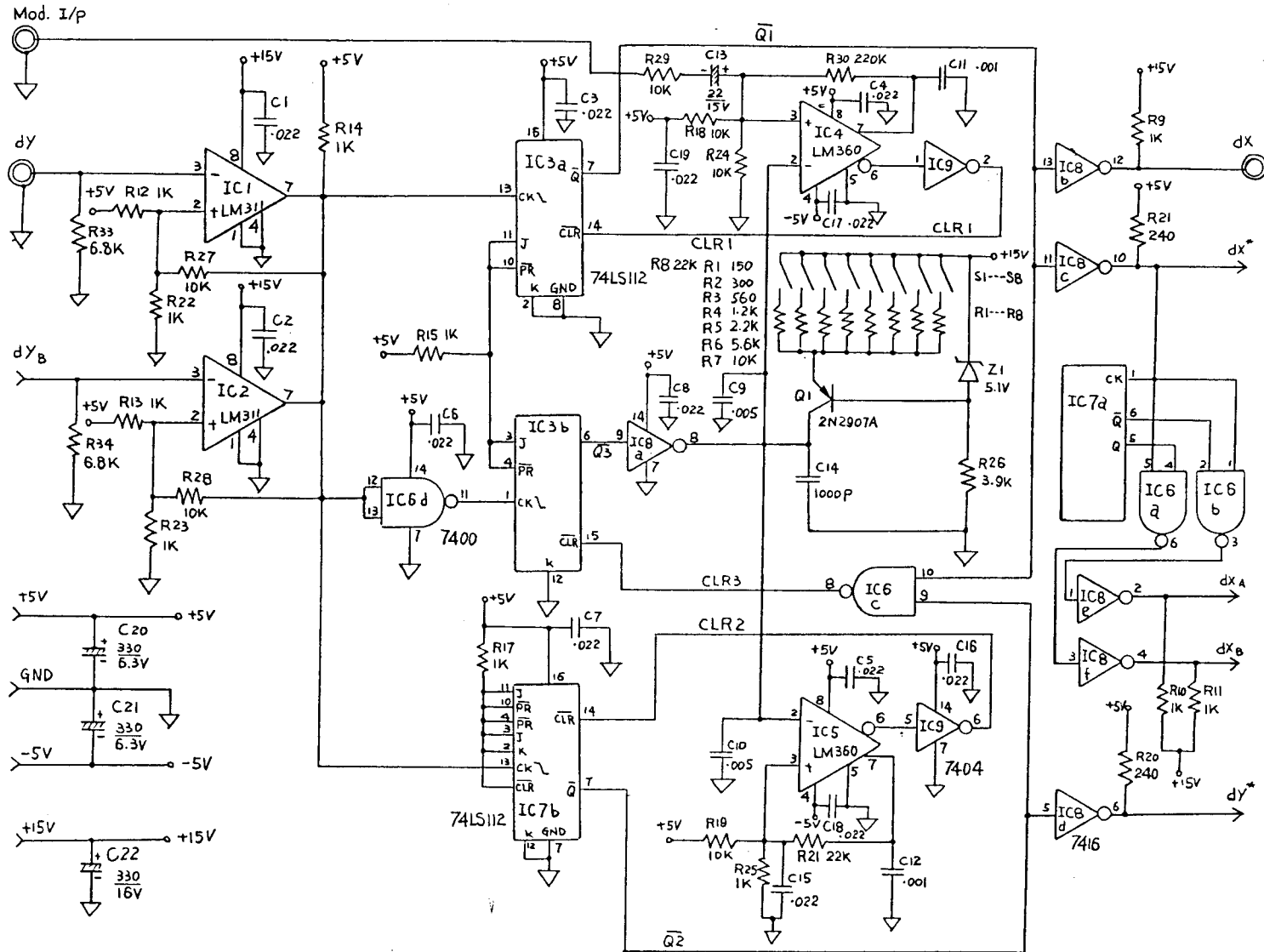


Figure 25. Schematic of The Digital Modulator

inverters IC_{8b}, IC_{8c}, and IC_{8d}. The outputs of these inverters supply the drive signal, dx, of the power stage in switching mode power supply and provide the two measurement signals, dx* and dy*.

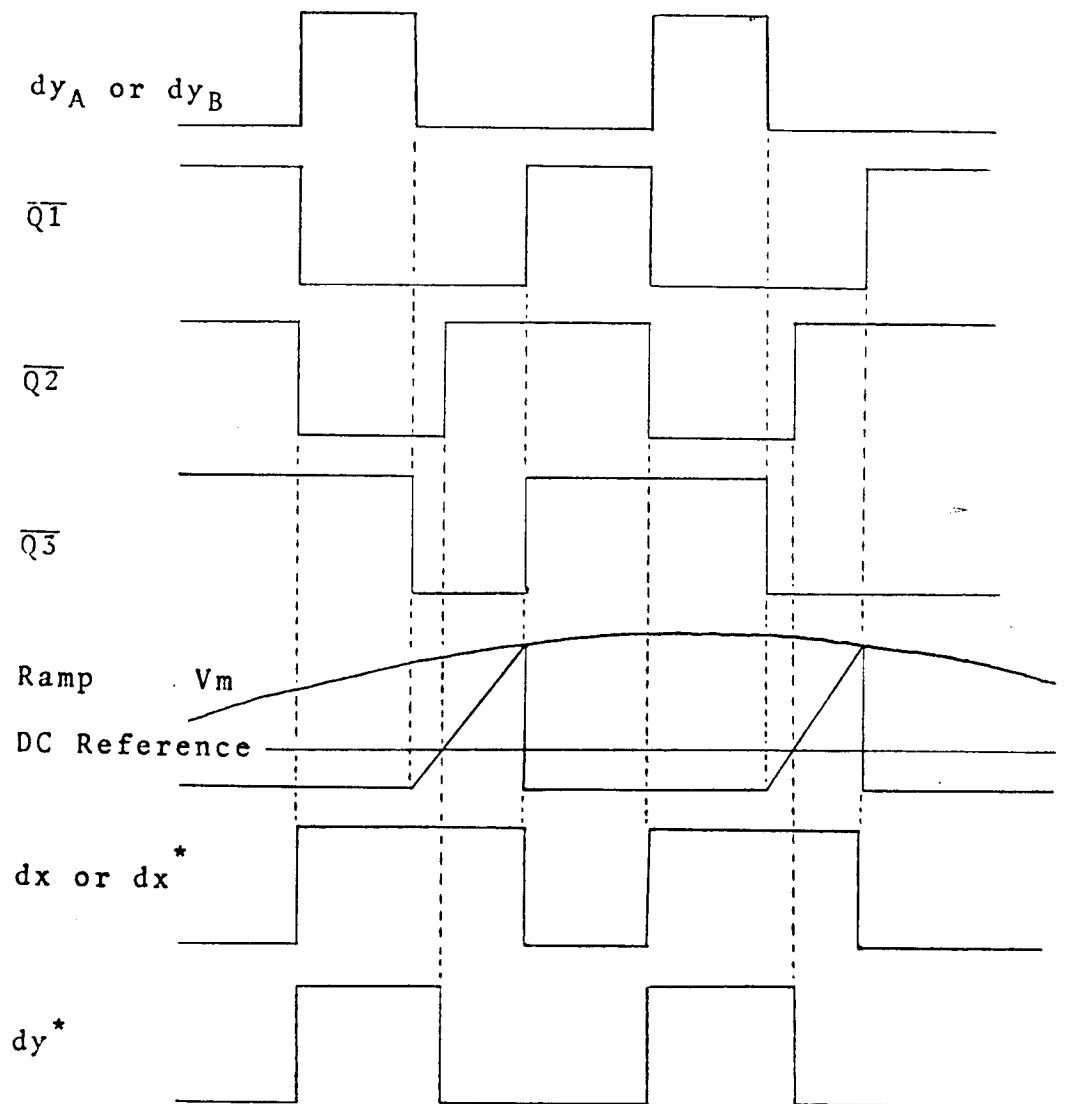


Figure 26. Waveforms in The Circuit Schematic of Figure 25

When the input signal from the duty cycle modulator goes low again, flip-flop IC_{3b} is clocked and set, initiating a linear ramp at the collector of Q₁. The amplitude of this ramp is compared to a DC reference by comparator IC₅, and to a modulated reference by comparator IC₄. When the amplitude of the ramp exceeds the value of the modulated reference, the inverted output of IC₄ goes high, flip-flop IC_{3a} is cleared, and the output signals dx and dx* are set low. When the ramp intersects the DC reference, the inverted output of IC₅ goes high, flip-flop IC_{7b} is cleared, and the output signal dy* is set low. When both IC_{3a} and IC_{7b} have been cleared, the signal CLR3 goes low, flip-flop IC_{3b} is cleared, and the ramp is terminated.

The digital modulator provides an output dy*, which is a pulse equal to the input pulse dy_A or dy_B plus a DC delay, and the outputs dx and dx* which are pulses equal to the input pulse plus a modulated delay which is proportional to the sinusoidal modulated signal. The output dx* also drives flip-flop IC_{7a} and gates IC_{6a} and IC_{6b}, providing push-pull output signals dx_A and dx_B.

The amount of modulation is adjustable by varying the resistance at the emitter of Q₁ or by changing the amplitude of the sinusoidal modulated signal input. Since the introduction of the digital modulator introduces a delay into the power supply control loop, there will be an extra phase delay at higher frequencies. Although this is compensated for in the measurement by using the delayed signal dy* instead of dy, it may cause a high-bandwidth,

small phase margin system to go unstable. The amount of DC delay should therefore be kept as small as possible for the amount of modulation required.

6.3.2 The Digital Demodulator

Because both dx^* and dy^* are the sinusoidal modulated pulses, it is difficult to calculate the loop gain, T . Therefore, the sinusoidal waveforms, V_x and V_y , must be extracted from dx^* and dy^* and restored respectively. The schematic for the digital demodulator is shown in Figure 27. The functional description with the important waveforms in Figure 28 are given as follows.

The demodulator accepts one of the measurement signals dx^* or dy^* from the digital modulator. When the input signal goes high, a timing ramp is initiated at the collector of Q1, which times out an interval slightly shorter than the minimum pulse width of the input to the demodulator. After this interval, a second linear ramp is initiated at the collector of Q2. When the input pulse goes low, this ramp is held constant, since the output of IC_{5c} no longer drives the base of Q2. The value of the ramp voltage at this point is then proportional to the pulse width of the input signal, and this value is sampled and held by IC₈ and IC₉, and the collector of Q2 is then grounded by IC_{5b}. This process is repeated for each input pulse to the demodulator. The resulting output waveform is then a sinusoid at the modulation frequency, sampled at the switching frequency of

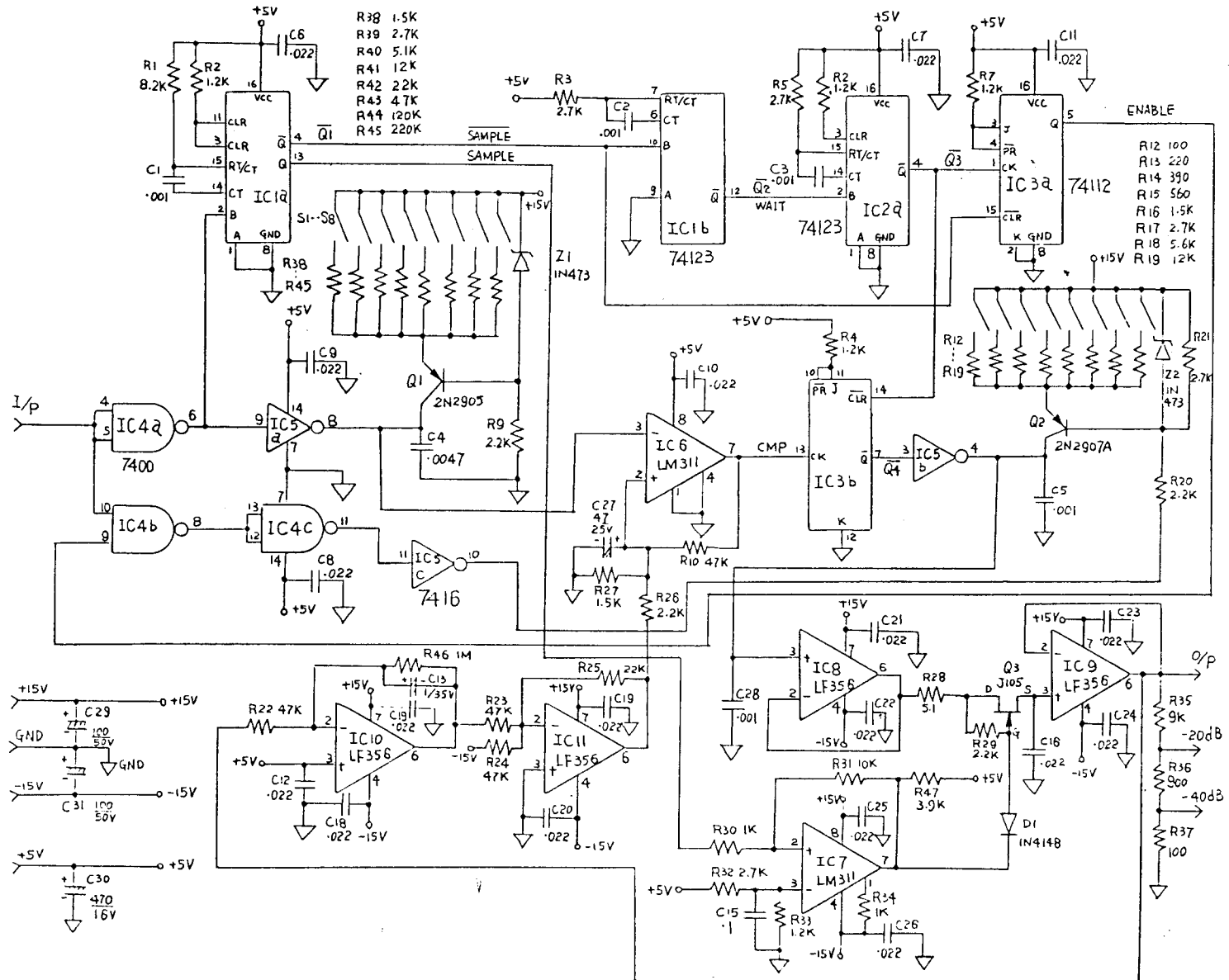


Figure 27. Schematic of The Digital Demodulator

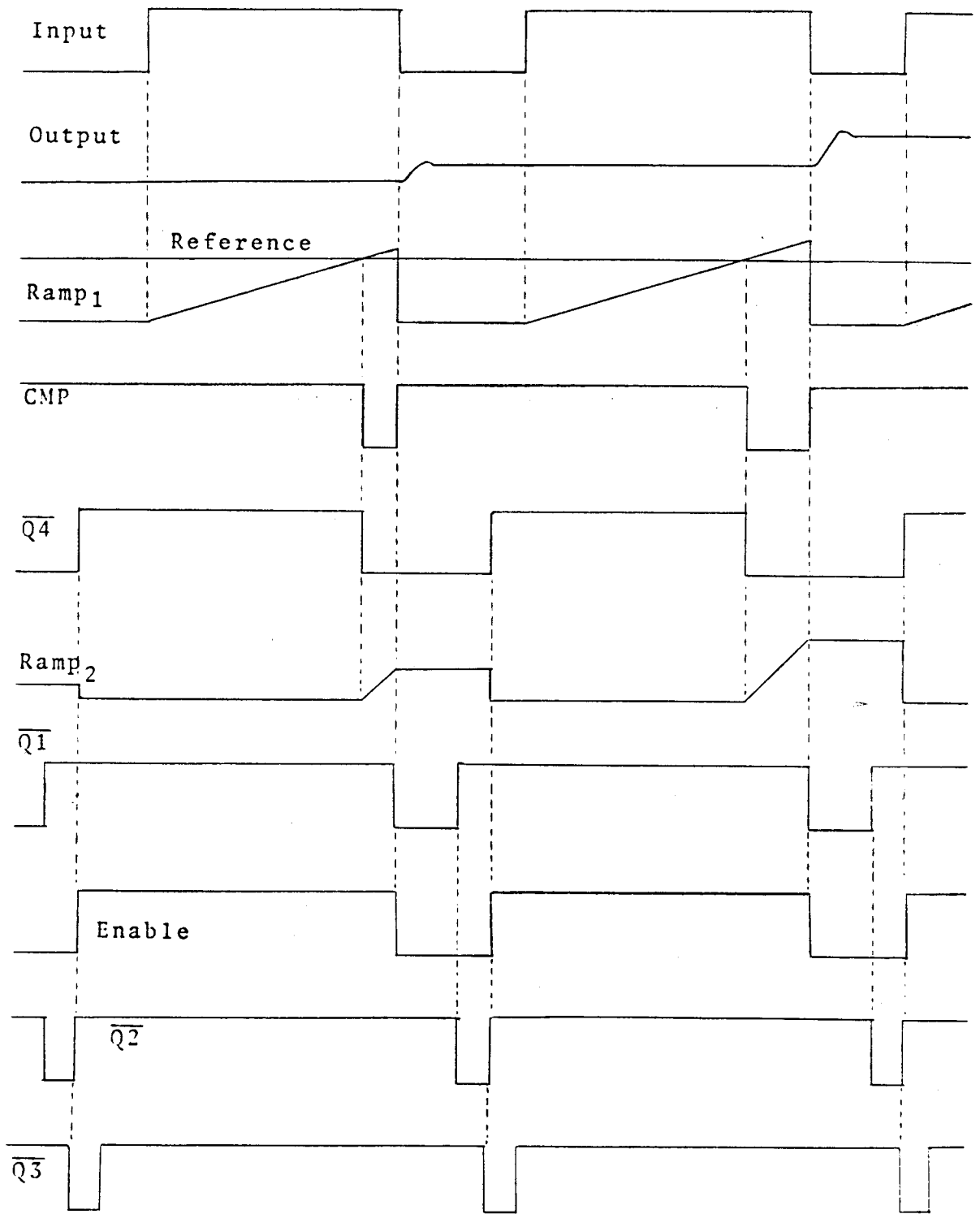


Figure 28. Waveforms in The Circuit Schematic of Figure 27

the input waveform. The gain of this circuit is determined by the slope of the ramp at the collector of Q_2 which can be adjusted by changing the emitter resistance.

The reference voltage for IC_6 is generated by sensing the output voltage, extracting the DC component of it and comparing with a 5V reference. If the delay from the input going high to the initiation of the second ramp is too short, the output voltage will increase its DC level above 5V. The output sensing circuit will detect this shift and increase the reference level to IC_6 , and hence increase the time delay before the second ramp is initiated. This feedback mechanism eliminates the necessity of manual adjustment, and allows the circuit to have a steep timing ramp and hence high gain.

6.4 Loop Gain Measurement With Digital Modulation Technique

In the measurement of loop gain, one digital modulator and two identical demodulators, one for dx^* and one for dy^* , are required. The application of the digital modulation technique for measurement of the loop gain of a switching power supply is shown in Figure 29. In this application, the original closed loop circuit topology is retained, and the proper DC operating conditions are maintained the same. Note that the signals V_x and V_y are phasors, and it is not necessary to demodulate the dz to the sinusoidal waveform. Because the KVL must be satisfied, then V_z is given by

$$V_z = V_x + V_y \quad (105)$$

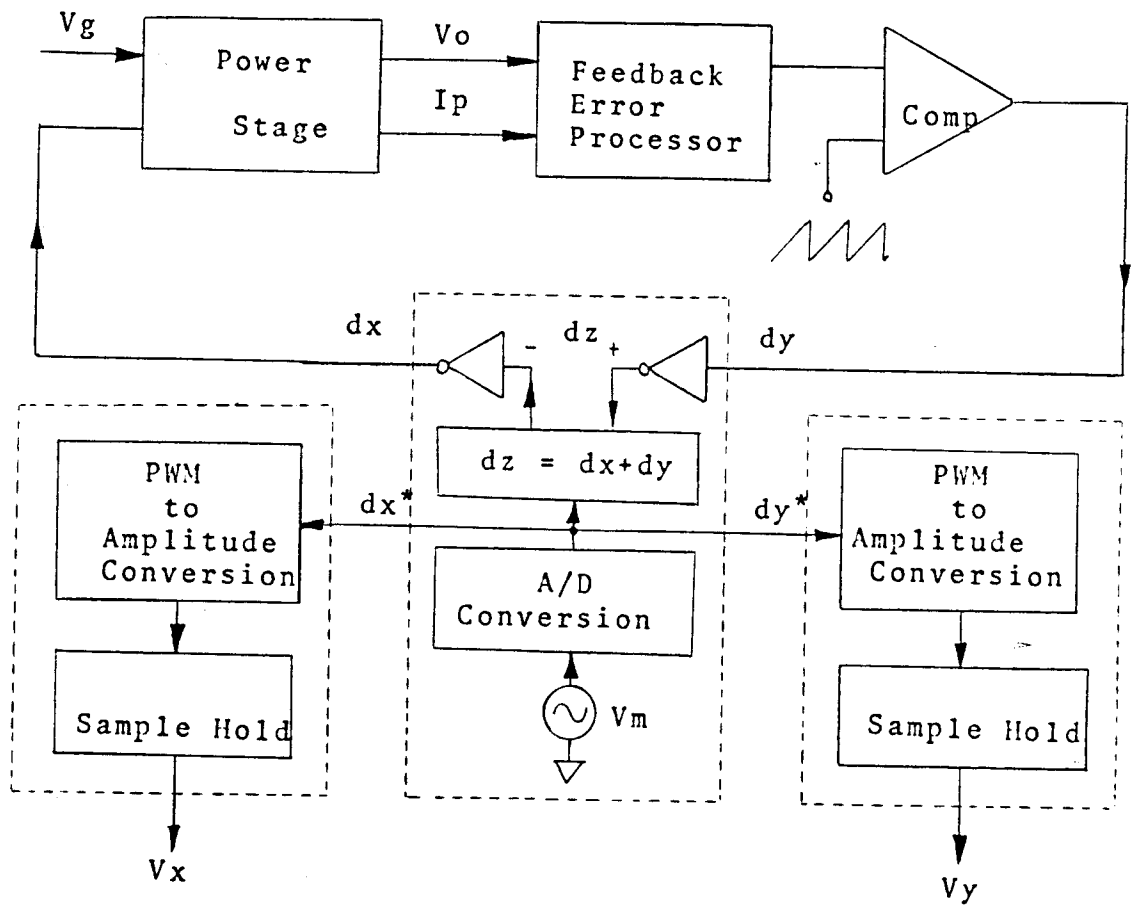


Figure 29. Application of The Digital Modulation Technique for Loop Gain Measurement with a Switching Power Supply

6.4.1 Determination of T Without Amplifier

By definition, the loop gain is given by

$$T = V_y / V_x \tag{106}$$

At any frequency, one measures not only the magnitude $|V_x|$ and $|V_y|$ to give

$$|T| = |V_y| / |V_x| \quad (107)$$

but also the magnitude $|V_z|$ of the third phasor, so that by trigonometric solution of phasor triangle one obtains

$$\angle T = \pm \cos^{-1} \left[\frac{|V_z|^2 - (|V_x|^2 + |V_y|^2)}{2 |V_x| |V_y|} \right] \quad (108)$$

or equivalently,

$$\angle T = \pm 2 \cos^{-1} \frac{|V_z|^2 - (|V_x| - |V_y|)^2}{4 |V_x| |V_y|} \quad (109)$$

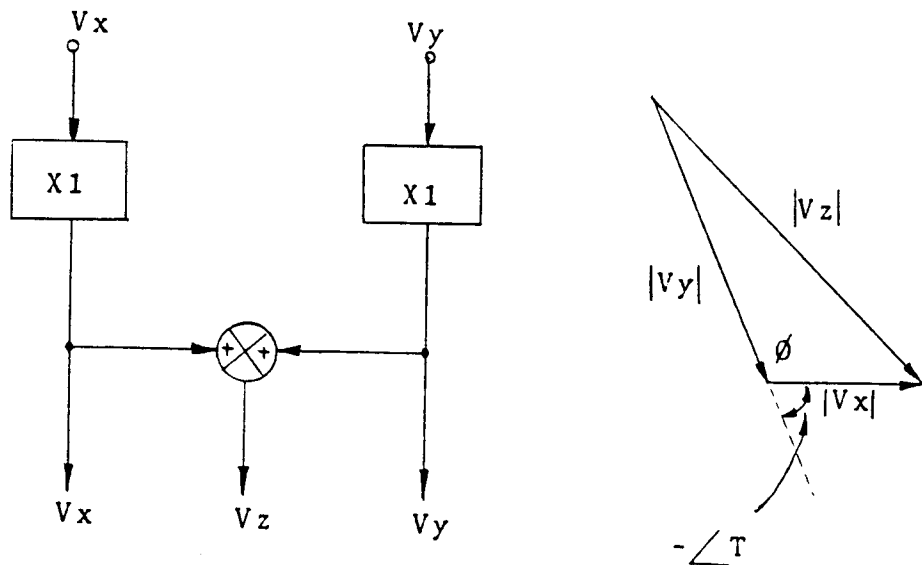


Figure 30. Determination of T , by The Measurement of The Three Magnitude $|V_x|$, $|V_y|$ and $|V_z|$

The above formulas for determination of angle $\angle T$ are derived from the law of Cosines and half angle relation.

$$\text{Law of Cosines : } |V_z|^2 = |V_x|^2 + |V_y|^2 - 2|V_x||V_y| \cos \phi$$

Half angle relation:

$$\cos \frac{\phi}{2} = \pm \sqrt{\frac{1 + \cos \phi}{2}} \quad (110)$$

From the phasor diagram in Figure 30, angle $\angle T$ is given by

$$\angle T = 180^\circ - \phi \quad (111)$$

and

$$\cos (180^\circ - \phi) = -\cos \phi = \cos (\angle T) \quad (112)$$

From law of Cosines,

$$\cos \phi = \frac{|V_x|^2 + |V_y|^2 - |V_z|^2}{2 |V_x| |V_y|} \quad (113)$$

hence

$$\cos \angle T = \frac{|V_z|^2 - (|V_x|^2 + |V_y|^2)}{2 |V_x| |V_y|} \quad (114)$$

$$\angle T = \pm \cos^{-1} \left[\frac{|V_z|^2 - (|V_x|^2 + |V_y|^2)}{2 |V_x| |V_y|} \right] \quad (115)$$

From the half angle relation

$$\cos \left(\frac{\angle T}{2} \right) = \pm \sqrt{\frac{1 + \cos (\angle T)}{2}} \quad (116)$$

$$\cos \left(\frac{\angle T}{2} \right) = \pm \sqrt{\frac{|V_z|^2 - (|V_x|^2 - 2|V_x||V_y| + |V_y|^2)}{4 |V_x| |V_y|}} \quad (117)$$

$$\cos \left(\frac{\angle T}{2} \right) = \pm \sqrt{\frac{|Vz|^2 - (|Vx| - |Vy|)^2}{4 |Vx| |Vy|}} \quad (118)$$

hence

$$\begin{aligned} \angle T &= \pm 2 \cos^{-1} \left[\cos \left(\frac{\angle T}{2} \right) \right] \\ &= \pm 2 \cos^{-1} \left[\sqrt{\frac{|Vz|^2 - (|Vx| - |Vy|)^2}{4 |Vx| |Vy|}} \right] \end{aligned} \quad (119)$$

Although the sign given by the above equation is ambiguous, proper choice is usually obvious from the qualitative nature of the magnitude response and known properties of the loop. The above formula applies when $\angle T$ is in the range $0^\circ < \pm \angle T < 180^\circ$; for the range $180^\circ < \pm \angle T < 360^\circ$, the appropriate form is $\angle T = \pm (360^\circ - \theta)$, where θ is the first or second quadrant angle given by the above equation.

6.4.2 Determination of T With Amplifier

The above equation of $\angle T$ gives an accurate result for loop gain phase angle in the important frequency range in the neighbourhood of loop gain crossover, when $|T| = 1$. However, it is not accurate when either $|T| \gg 1$ or $|T| \ll 1$, since then either $|Vx| \gg |Vy|$ and $|Vz| = |Vy|$, or $|Vx| \gg |Vy|$ and $|Vz| = |Vx|$. This condition is immediately obvious in graphical terms from the phasor diagram illustrated in Figure 30, drawn for $|T| > 1$, it is clear that some small errors in the measurement of the magnitude $|Vy|$ or $|Vz|$ can lead to large errors in $\angle T$.

The undesirable defect in the phase measurement of Figure 30 can easily be overcome by use of unequal gains for V_x and V_y , as shown in Figure 31. To the extent that the gains A_x and A_y have zero (or the same) phase, the angle between $A_y V_y$ and $A_x V_x$ determined from the three magnitudes $|A_x V_x|$, $|A_y V_y|$ and $|V_{zz}| = |A_x V_x + A_y V_y|$ is the same as the angle between V_y and V_x , namely $\angle T$; thus the equation of phase angle , for example, becomes

$$\angle T = \pm 2 \cos^{-1} \left[\frac{\sqrt{|V_{zz}|^2 - (|A_x V_x| - |A_y V_y|)^2}}{4 |A_x V_x| |A_y V_y|} \right] \quad (120)$$

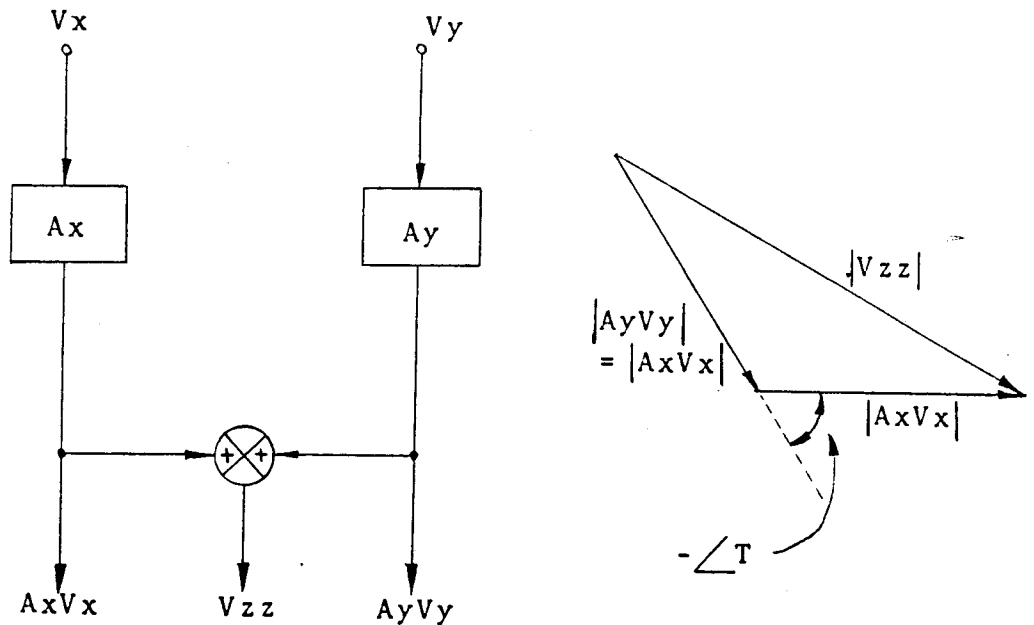


Figure 31. Determination of $\angle T$ by The Measurement of The Scaled Magnitude $|A_x V_x| = |A_y V_y|$ and $|V_{zz}|$

and can be made well-conditioned at all frequencies by adjustment of the gains A_x and A_y so that all three measured magnitudes are of comparable size. In fact, an additional condition simplifies the procedure considerably: one merely

adjusts A_x and A_y so that the magnitudes $|A_x V_x|$ and $|A_y V_y|$ are equal. Let the corresponding magnitude of the summed signal be $|V_{zz}|$ when $|A_x V_x| = |A_y V_y|$; then the above equation of $\angle T$ reduces to

$$\angle T = \pm \cos^{-1} \left[\frac{|V_{zz}|}{2 |A_x V_x|} \right] \quad (121)$$

The practical procedure is therefore to adjust A_x and A_y until equal $|A_x V_x|$ and $|A_y V_y|$ are obtained, and then to measure the corresponding phasor sum $|V_{zz}| = |A_x V_x + A_y V_y|$ for use in the above equation. It is not necessary to know either A_x or A_y . As shown in Figure 31, this procedure scales the two largest phasor magnitudes until they are comparable with the smallest phasor magnitudes, without changing the required loop gain angle $\angle T$. The required loop gain magnitude $|T|$ is of course obtained by setting the two gain equal $A_x = A_y = A$, and measuring $|A V_x|$ and $|A V_y|$ so that $|T| = |A_y V_y| / |A_x V_x| = |V_y| / |V_x|$.

6.5 Results of Loop Gain Measurements

The system loop gain measurements are taken by using the digital modulation technique. The disturbance insertion point is the output of the threshold detector which is the only location common to voltage feedback and current feedback loops. Figure 32 shows the measurement and simulation results of the system loop gain characteristics. The Bode plot of simulation results are represented by the

"M" sign for gain and the "P" sign for phase, and the gain and the phase measurements are denoted by the "x" sign and the "o" sign respectively.

COMPUTER SIMULATION FOR MULTI-LOOP CONTROL FLY-BACK SMPS

BODE

THE SYSTEM LOOP GAIN = TS

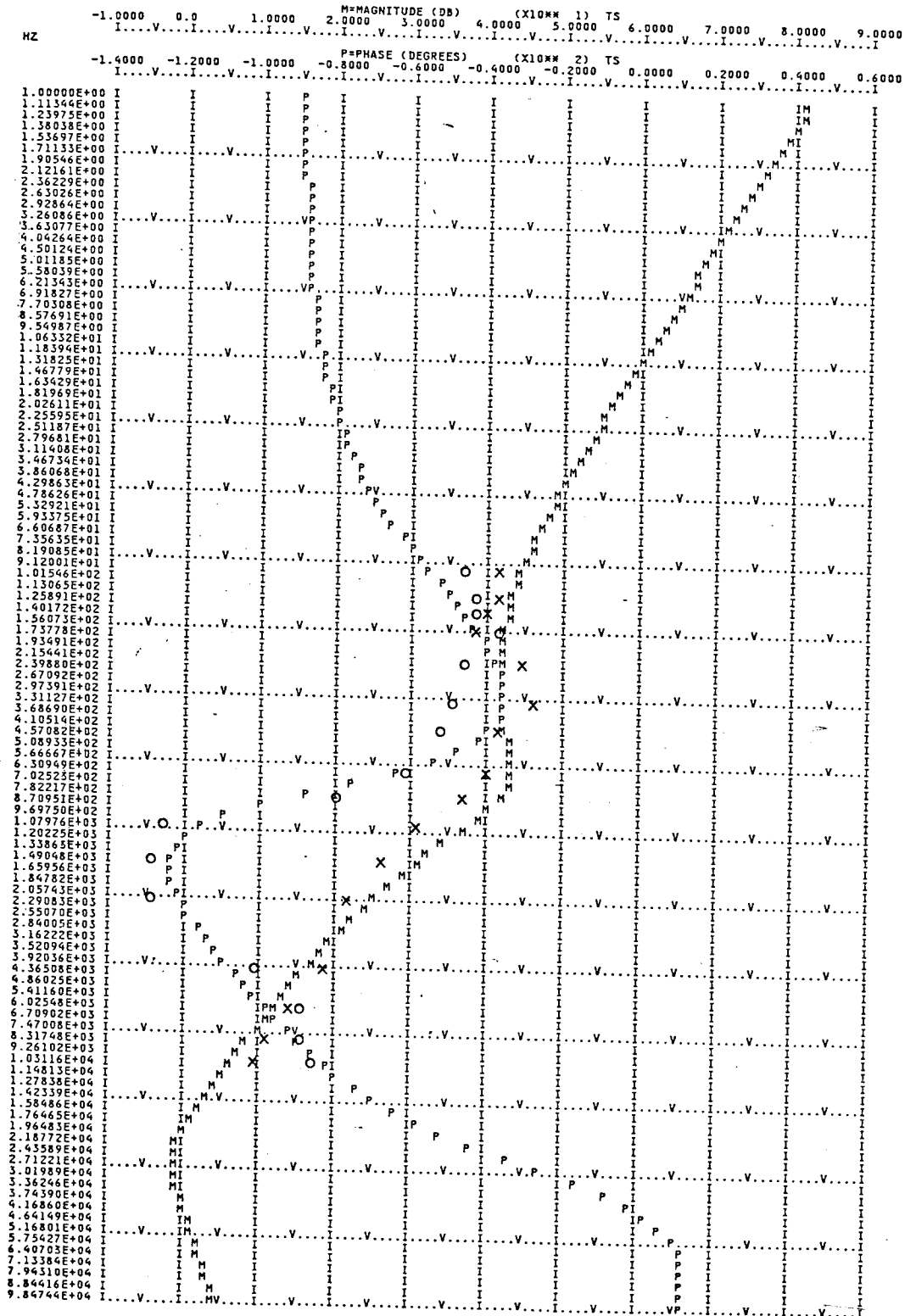


Figure 32. Measurement and Simulation Bode Plot of The System Loop Gain

CHAPTER 7

CONCLUSION

Modeling, analysis, simulation and measurement of a fly-back switching mode power supply employing multiple loop control is presented. The objectives are to examine the small-signal dynamic performances and to provide an adequate measurement method of the fly-back switching mode power supply which is operated in continuous MMF mode and at a constant frequency.

To gain insights to the performance characteristics of this power supply, this power supply is modeled according to the three basic function blocks: fly-back power stage, error processor, and pulse width modulator. Models of these blocks are presented in Chapter 2, Chapter 3, and Chapter 4, respectively. In Chapter 5, the small-signal model for each block is assembled. Employing this small-signal model and LISA 360 program package, the following performance characteristics are simulated:

- (a) the audio-susceptibility characteristics
- (b) the output impedance characteristics
- (c) the system loop gain characteristics

An adequate measurement method, digital modulation technique, and the experimental verifications of the system loop gain is provided in Chapter 6 with good correlations between the measurement and the simulation results. Besides, it is interesting to point out that high gain,

wide-bandwidth, and stable operation could be simultaneously accomplished in this power supply. This characteristic has made the multiple loop control unique in comparison with the single loop control in switching mode power supply.

APPENDIX A

Derivations of State-space Equations

The derivations will begin with the basic KVL and KCL equations and apply matrix notation to form the A1, A2, B1, B2, C1, C2, E1, and E2 in the Chapter 2.

During T_{on} (refer to Figure 9) the KVL equation on the primary side is:

$$d\phi/dt = (v_i/N_P) - (R_P/N_P) i_p$$

$$i_p = (N_P/L_P) \phi$$

Therefore,

$$d\phi/dt = (v_i/N_P) - (R_P/L_P) \phi$$

KVL equations for the secondary side are:

$$-v_C - R_C C (dv_C/dt) + [-C (dv_C/dt) + i_o] R_L = 0$$

$$dv_C/dt = \{-1/[(R_C + R_L)C]\} v_C + \{R_L/[(R_C + R_L)C]\} i_o$$

The output equations are of the following form:

$$v_o = (i_1 - i_2) R_L$$

$$= (-C dv_C/dt + i_o) R_L$$

$$= R_L C \{1/[(R_C + R_L)C]\} v_C - R_L C \{R_L/[(R_C + R_L)C]\} i_o + R_L i_o$$

$$= [R_L/(R_C + R_L)] v_C + [R_C R_L/(R_C + R_L)] i_o$$

$$= [R_C/(R_C + R_L)] v_C + (R_C//R_L) i_o$$

The matrix form of the state equations format $\dot{\underline{x}} = A\underline{1}\underline{x} + B\underline{u}$ and $\underline{y} = C\underline{1}\underline{x} + E\underline{u}$ is :

$$\begin{bmatrix} d\phi/dt \\ dv_C/dt \end{bmatrix} = \begin{bmatrix} -R_P/L_P & 0 \\ 0 & -1/[(R_C+R_L)C] \end{bmatrix} \cdot \begin{bmatrix} \phi \\ v_C \end{bmatrix} +$$

$$\begin{bmatrix} 1/N_P & 0 \\ 0 & R_L/[(R_C+R_L)C] \end{bmatrix} \cdot \begin{bmatrix} v_i \\ i_o \end{bmatrix}$$

$$\begin{bmatrix} v_o \\ i_p \end{bmatrix} = \begin{bmatrix} 0 & R_L/(R_C+R_L) \\ N_P/L_P & 0 \end{bmatrix} \cdot \begin{bmatrix} \phi \\ v_C \end{bmatrix} +$$

$$\begin{bmatrix} 0 & R_C/R_L \\ 0 & 0 \end{bmatrix} \cdot \begin{bmatrix} v_i \\ i_o \end{bmatrix}$$

During T_{F1} (refer to Figure 9) KVL equations for i_1 , i_2 , and i_3 are:

$$v_s = i_1 R_S + (i_1 - i_2)R_C + v_C$$

$$\begin{aligned} v_C &= (i_2 - i_1)R_C + (i_2 - i_3)R_L \\ &= i_2(R_C + R_L) - i_1R_C + i_oR_L \end{aligned}$$

$$i_3 = - i_o$$

Simplifying the above equations results in the following:

$$v_s = (R_S+R_C)i_1 - [R_C/(R_C+R_L)] \cdot [v_C+R_Ci_1-R_Li_o] + v_C$$

$$i_2 = (v_C+R_Ci_1-R_Li_o)/(R_C+R_L)$$

From Figure 9 the following equations can be derived:

$$i_1 = i_s = N_S \phi / L_S$$

$$\begin{aligned} d\phi/dt &= -v_c / N_S \\ &= (-1/N_S) \{ (R_S + R_C) i_1 - [R_C (v_c + R_C i_1 - R_L i_o)] / (R_C + R_L) + v_c \} \\ &= (-1/N_S) \{ (R_S + R_C) (N_S \phi / L_S) - [R_C / (R_C + R_L)] \cdot [v_c + R_C \\ &\quad (N_S \phi / L_S) - R_L i_o] + v_c \} \\ &= -\{ [(R_S + R_C) / L_S - R_C^2 / ((R_C + R_L) L_S)] \phi \\ &\quad + [1 - R_C / (R_C + R_L)] \cdot (1/N_S) v_c \\ &\quad + [R_C R_L / ((R_C + R_L) N_S)] i_o \} \\ &= -\{ (R_S + R_C // R_L) / L_S \} \phi - \{ R_L / [(R_C + R_L) N_S] \} v_c \\ &\quad - \{ (R_C // R_L) / N_S \} i_o \end{aligned}$$

From Figure 9 it can be seen that:

$$i_c = i_1 - i_2 = C dv_c / dt \quad \text{and} \quad i_1 = N_S \phi / L_S$$

Then,

$$\begin{aligned} dv_c / dt &= (i_1 - i_2) / C \\ &= (1/C) \cdot \{ (N_S \phi / L_S) - [(v_c + R_C i_1 - R_L i_o) / (R_C + R_L)] \} \\ &= \{ (R_L N_S) / [(R_C + R_L) L_S C] \} \phi - \{ 1 / [(R_C + R_L) C] \} v_c \\ &\quad + \{ R_L / [(R_C + R_L) C] \} i_o \end{aligned}$$

The output equations are of the following form:

$$\begin{aligned} v_o &= R_L (i_2 - i_3) = R_L \{ [(v_c + R_C i_1 - R_L i_o) / (R_C + R_L)] + i_o \} \\ &= [R_L / (R_C + R_L)] \cdot [v_c + (R_C N_S / L_S) \phi - R_L i_o] + R_L i_o \\ &= [R_L / (R_C + R_L)] v_c + [(R_C // R_L) N_S / L_S] \phi + [R_C // R_L] i_o \end{aligned}$$

$$i_p = 0$$

In matrix form, $\dot{\underline{x}} = A_2 \underline{x} + B_2 \underline{u}$ and $\underline{y} = C_2 \underline{x} + E_2 \underline{u}$ are expressed in the following form:

$$\begin{bmatrix} d\phi/dt \\ dv_C/dt \end{bmatrix} = \begin{bmatrix} \frac{-[R_S + (R_C // R_L)]}{L_S} & \frac{-R_L}{N_S (R_C + R_L)} \\ \frac{R_L N_S}{L_S C (R_C + R_L)} & \frac{-1}{C (R_C + R_L)} \end{bmatrix} \cdot \begin{bmatrix} \phi \\ v_C \end{bmatrix} + \begin{bmatrix} 0 & -(R_C // R_L) / N_S \\ 0 & R_L / [(R_C + R_L) C] \end{bmatrix} \cdot \begin{bmatrix} v_i \\ i_o \end{bmatrix}$$

$$\begin{bmatrix} v_o \\ i_p \end{bmatrix} = \begin{bmatrix} [(R_C // R_S) N_S] / L_S & R_L / (R_C + R_L) \\ 0 & 0 \end{bmatrix} \cdot \begin{bmatrix} \phi \\ v_C \end{bmatrix} +$$

$$\begin{bmatrix} 0 & R_C // R_L \\ 0 & 0 \end{bmatrix} \cdot \begin{bmatrix} v_i \\ i_o \end{bmatrix}$$

APPENDIX B

Derivations of Transfer Functions for Fly-back Power Stage

In Appendix B a detailed formulation for the steady state (DC) transfer function, the input-to-output transfer function, and the duty cycle-to-output transfer function is presented.

B.1 Derivation for \underline{Y}

$$\underline{Y} = \begin{bmatrix} V_o \\ I_p \end{bmatrix} = (E - CA^{-1}B)\underline{U}$$

$$= \left\{ \begin{bmatrix} 0 & R_C \\ 0 & 0 \end{bmatrix} - \frac{1}{\omega_o^2 \left(\frac{R_S + D'R_C}{D'^2 R_L} + 1 \right)} \begin{bmatrix} \frac{N_S R_C}{L_e D'} & 1 \\ DN_p & 0 \end{bmatrix} \right\} \cdot \begin{bmatrix} \frac{-1}{R_L C} & \frac{D'}{N_S} \\ \frac{-N_S \omega_o^2}{D'} & \frac{-DR_p}{L_p} - D' \left(\frac{R_S + R_C}{L_S} \right) \end{bmatrix} \cdot \begin{bmatrix} \frac{D}{N_p} & \frac{-D'R_C}{N_S} \\ 0 & 1/C \end{bmatrix} \cdot \begin{bmatrix} V_i \\ 0 \end{bmatrix}$$

$$\underline{Y} = \frac{1}{\omega_o^2 \left[\frac{R_S + D'R_C}{D'^2 R_L} + 1 \right]} \cdot \begin{bmatrix} \frac{\omega_o^2 N_S D}{D' N_P} \cdot \frac{R_C}{R_L} + 1 \\ \frac{D^2}{L_P R_L C} \end{bmatrix} \cdot V_i$$

Assume that

$$\frac{R_S + D'R_C}{D'^2 R_L} \ll 1 \quad \text{and} \quad \frac{R_C}{R_L} \ll 1$$

Therefore,

$$\underline{Y} = \begin{bmatrix} \frac{D N_S}{D' N_P} \\ \frac{D^2}{\omega_o^2 L_P R_L C} \end{bmatrix} \cdot V_i = \begin{bmatrix} \frac{D N_S}{D' N_P} \\ \frac{D^2 L_e}{L_P R_L} \end{bmatrix} \cdot V_i$$

B.2 Derivation of The Input-to-output Transfer Function

$$\tilde{Y}(s) = \left[C(SI - A)^{-1} B + E \right] \tilde{u}(s)$$

$$(sI - A) = \begin{bmatrix} s + \frac{R_S + D'R_C}{L_e D'^2} & D'/N_S \\ -(N_S \omega_o^2)/D' & s + 1/(R_L C) \end{bmatrix}$$

$$(sI - A)^{-1} = \frac{1}{s^2 + \left[\frac{R_S + D'R_C}{L_e D'^2} + \frac{1}{RLC} \right] s + \left[\frac{(R_S + D'R_C) \omega_o^2}{D'^2 R_L} + \omega_o^2 \right]}$$

$$\cdot \begin{bmatrix} s + \frac{1}{RLC} & -D'/N_S \\ \frac{N_S \omega_o^2}{D'} & s + \frac{R_S + D'R_C}{L_e D'^2} \end{bmatrix}$$

Let

$$\zeta = \frac{\omega_o}{2} \left[\frac{L_e}{R_L} + (R_e + \frac{R_C}{D'}) C \right] \quad \text{and} \quad \frac{R_S + D'R_C}{D'^2 R_L} \ll 1$$

$$(sI - A)^{-1} = \frac{1}{s^2 + 2\zeta\omega_o s + \omega_o^2} \begin{bmatrix} s + \frac{1}{RLC} & -D'/N_S \\ \frac{N_S \omega_o^2}{D'} & s + \frac{R_S + D'R_C}{L_e D'^2} \end{bmatrix}$$

Thus,

$$\tilde{Y}(s) = \begin{bmatrix} \frac{1}{s^2 + 2\zeta\omega_o s + \omega_o^2} \frac{N_S R_C}{L_e D'^2} \\ \frac{D N_P}{L_P} \end{bmatrix} \begin{bmatrix} 1 \\ 0 \end{bmatrix} \cdot \begin{bmatrix} s + \frac{1}{RLC} & \frac{-D'}{N_S} \\ \frac{N_S \omega_o^2}{D'} & s + \frac{R_S + D'R_C}{L_e D'^2} \end{bmatrix}$$

$$\cdot \begin{bmatrix} \frac{D}{N_P} & \frac{-D'R_C}{N_S} \\ 0 & 1/C \end{bmatrix} + \begin{bmatrix} 0 & R_C \\ 0 & 0 \end{bmatrix} \left. \vphantom{\begin{bmatrix} \frac{D}{N_P} & \frac{-D'R_C}{N_S} \\ 0 & 1/C \end{bmatrix}} \right\} \begin{bmatrix} v_i(s) \\ i_o(s) \end{bmatrix}$$

Because $1 + R_C/R_L \approx 1$,

$$\tilde{y}(s) = \frac{1}{s^2 + 2\zeta\omega_0 s + \omega_0^2}$$

$$\begin{bmatrix} \frac{N_S \omega_0^2 D}{D' N_P} (s R_C C + \frac{R_C}{R_L} + 1) & R_C \left[s^2 + \left(2\zeta\omega_0 - \frac{R_C}{L_e} + \frac{1}{R_C C} \right) s + \omega_0^2 \left(\frac{R_e}{R_C} + \frac{D}{D'} \right) \right] \\ \frac{D^2}{L_P} \left(s + \frac{1}{R_L C} \right) & - \frac{D D' N_P}{L_P N_S C} (s R_C C + 1) \end{bmatrix} \begin{bmatrix} \tilde{v}_i(s) \\ \tilde{i}_o(s) \end{bmatrix}$$

Then,

$$\tilde{y}(s) = \frac{\begin{bmatrix} \frac{N_S \omega_0^2 D}{D' N_P} (s R_C C + 1) & R_C (s^2 + z_1 s + \omega_0^2 z_2) \\ \frac{D^2}{L_P} \left(s + \frac{1}{R_L C} \right) & - \frac{D D' N_P}{L_P N_S C} (s R_C C + 1) \end{bmatrix} \begin{bmatrix} v_i(s) \\ i_o(s) \end{bmatrix}}{s^2 + 2\zeta\omega_0 s + \omega_0^2}$$

where $z_1 = 2\zeta\omega_0 - \frac{R_C}{L_e} + \frac{1}{R_C C}$, and $z_2 = (R_e/R_C) + (D/D')$

B.3 Derivation of The Duty Cycle-to-output Transfer Function

$$\tilde{y}(s) = \left\{ C(sI-A)^{-1} \left[(A1-A2)\underline{x} + (B1-B2)\underline{u} \right] + \left[(C1-C2)\underline{x} + (E1-E2)\underline{u} \right] \right\} \tilde{d}(s)$$

$$\underline{x} = -A^{-1}BU$$

$$= \frac{V_i}{\omega_o^2 \left[\frac{R_S + D'RC}{D'^2 R_L} + 1 \right]} \cdot \begin{bmatrix} \frac{D}{R_L C N_P} \\ \frac{N_S \omega_o^2 D}{N_P D'} \end{bmatrix}$$

Because $\frac{R_S + D'RC}{D'^2 R_L} \ll 1$, $V_o = \frac{DN_S}{D'N_P} V_i$, and $V_i = \frac{D'N_P}{DN_S} V_o$

Hence

$$\underline{x} = \begin{bmatrix} \frac{DL_e}{R_L N_P} \\ \frac{N_S D}{N_P D'} \end{bmatrix} V_i = \begin{bmatrix} \frac{D' L_e}{N_S R_L} \\ 1 \end{bmatrix} V_o$$

$$C(sI - A)^{-1} = \frac{1}{s^2 + 2\zeta\omega_o s + \omega_o^2}$$

$$\begin{bmatrix} \frac{N_S R_C}{L_e D'} \left(s + \frac{1}{R_L C} \right) + \frac{N_S \omega_o^2}{D'} & s + \frac{R_S + D'RC}{L_e D'^2} - \frac{R_C}{L_e} \\ \frac{DN_P}{L_P} \left(s + \frac{1}{R_L C} \right) & - \frac{DD'N_P}{N_S L_P} \end{bmatrix}$$

$$(A1 - A2)\underline{x} + (B1 - B2)\underline{u} =$$

$$\begin{bmatrix} \frac{D' R_C L_e}{L_S N_S R_L} + \frac{1}{N_S} + \frac{D' N_P}{N_P D N_S} \\ - \frac{D' L_e}{L_S C R_L} \end{bmatrix} V_o = \begin{bmatrix} \frac{1}{N_S D} + \frac{R_C}{N_S D' R_L} \\ - \frac{1}{D' C R_L} \end{bmatrix} \cdot V_o$$

Because $R_C / (N_S D' R_L) \ll 1$, then

$$(A1 - A2)\underline{X} + (B1 - B2)\underline{U} = \begin{bmatrix} 1/(N_S D) & -1/(D' C R_L) \end{bmatrix}^T$$

$$(C1 - C2)\underline{X} + (E1 - E2)\underline{U} = (C1 - C2)\underline{X}$$

$$= \begin{bmatrix} -R_C / (D' R_L) \\ \frac{D' L_e N_P}{L_P N_S R_L} \end{bmatrix} \cdot V_o$$

Since $L_S / L_P = N_S^2 / N_P^2$, so

$$(C1 - C2)\underline{X} = \begin{bmatrix} -R_C / (D' R_L) \\ \frac{N_S}{N_P R_L D'} \end{bmatrix} \cdot V_o$$

$$\frac{\tilde{Y}(s)}{\tilde{d}(s)} = C(sI - A)^{-1} \left[(A1 - A2)\underline{X} + (B1 - B2)\underline{U} \right] + \left[(C1 - C2)\underline{X} + (E1 - E2)\underline{U} \right]$$

$$= \frac{V_o \left[\begin{array}{l} \frac{w_o^2}{DD'} (sR_C C + 1) \cdot \left\{ 1 - \frac{D}{R_L (sR_C C + 1)} \cdot \left[\frac{R_C}{w_o^2} s^2 + \left(\frac{2R_C \zeta}{w_o} + L_e \right) s + \left(R_e + \frac{R_C}{D'} \right) \right] \right\} \\ \frac{N_S}{N_P R_L} \left\{ \frac{1}{CL_S} (sR_L C + 1 + D) + \frac{1}{D'} (s^2 + 2\zeta w_o s + w_o^2) \right\} \end{array} \right]}{s^2 + 2\zeta w_o s + w_o^2}$$

APPENDIX C

Data Provision of Simulation and Computer Simulation Program

In Appendix C a detailed expression for calculation of coefficients in each element of matrices which represent the small-signal model of fly-back power supply and meet the input requirements of LISA 360 program, a FORTRAN program designed to accept the circuit parameters and then to calculate those coefficients, and the LISA simulation program for this power supply are presented.

C.1 Expressions for Coefficient Calculation

From Chapter 5 each entry of dynamics matrices are listed below:

$$\begin{aligned} \Delta + F_{D1}F_VF_M &= s^2 + 2\zeta\omega_0s + \omega_0^2 + \{[\omega_0^2/(DD')](sR_C C+1) \\ &\quad - [\omega_0^2/(R_L D')][(R_C/\omega_0^2)s^2 + ((2R_C\zeta/\omega_0)+L_e)s \\ &\quad + (R_e+(R_C/D'))]\}.V_0F_M \cdot (1+sR_4C_1)[1+sC_2((R_5GQ+ \\ &\quad 1)/GQ)][GQ/(C_1+C_3)]\{s[1+(sR_4C_1C_3)/(C_1+C_3)]\} \cdot \\ &\quad (1+sR_5C_2)\}^{-1} \end{aligned}$$

$$\begin{aligned} F_{D1}F_C F_M &= \{(\omega_0^2/DD')(sR_C C+1) - (\omega_0^2/R_L D')[(R_C/\omega_0^2)s^2 \\ &\quad + ((2R_C\zeta/\omega_0)+L_e)s + R_e + (R_C/D')]\} F_C F_M V_0 \end{aligned}$$

$$\begin{aligned} F_{D2}F_VF_M &= \{[N_S/(N_P R_L C L_S)](sR_L C+1+D) + [N_S/(N_P D' R_L)] \\ &\quad (s^2+2\zeta\omega_0s+\omega_0^2)\}.V_0F_M(1+sR_4C_1)[1+sC_2((R_5GQ+1) \\ &\quad /GQ)].[GQ/(C_1+C_3)].\{s[1+(sR_4C_1C_3)/(C_1+C_3)] \\ &\quad (1+sR_5C_2)\}^{-1} \end{aligned}$$

$$\Delta + F_{D2}F_C F_M = s^2 + 2\zeta w_0 s + w_0^2 + \{ [N_S / (N_P R_L C L_S)] \cdot (s R_L C + 1 + D) + [N_S / (N_P D' R_L)] (s^2 + 2\zeta w_0 s + w_0^2) \} \cdot F_C F_M V_0$$

$$F_{U11} = [(N_S w_0^2 D) / (D' N_P)] (s R_C C + 1)$$

$$F_{U12} = R_C (s^2 + z_1 s + w_0^2 z_2)$$

$$F_{U21} = (D^2 / L_P) [s + 1 / (R_L C)]$$

$$F_{U22} = -[(D D' N_P) / (L_P N_S C)] (s R_C C + 1)$$

Note that

$$z_1 = 2w_0 + (1/R_C C) - (R_C/L_e) \quad ; \quad L_e = L_S/D'^2$$

$$z_2 = (R_e/R_C) + (D/D') \quad ; \quad R_e = R_S/D'^2$$

$$\zeta = (w_0/2) \{ (L_e/R_L) + [R_e + (R_C/D')] C \}$$

$$w_0^2 = (L_e C)^{-1}$$

$$GQ = \{ [1 + (R_3/R_1) + (R_3/R_2)] R_1 \}^{-1}$$

$$D(s) = s [1 + s R_4 (C_1 C_3) / (C_1 + C_3)] (1 + s R_5 C_2)$$

Let

$$A_1 = 2\zeta w_0 \quad A_2 = w_0^2 \quad A_3 = R_C C$$

$$A_4 = R_C / w_0^2 \quad A_5 = L_e + (2R_C \zeta / w_0)$$

$$A_6 = R_e + (R_C / D') \quad B_1 = R_4 C_1 C_3 / (C_1 + C_3)$$

$$B_2 = R_5 C_2 \quad D_1 = R_4 C_1$$

$$D_2 = C_2 [(R_5 G Q + 1) / G Q] \quad E_1 = R_L C$$

$$K_1 = w_o^2 / (D D') \quad K_2 = w_o^2 / (R_L D')$$

$$K_3 = G Q / (C_1 + C_3) \quad K_4 = N_S / (N_P R_L C L_S)$$

$$K_5 = N_S / (N_P R_L D') \quad K_6 = 1 + D$$

$$K_7 = N_S w_o^2 D / (N_P D') \quad K_8 = D^2 / L_P$$

$$K_9 = -D D' N_P / (L_P N_S C)$$

$$F_M = 2 n L_P V_o / (V_i R_{SW} T_P) \quad F_C = R_{SW} / n$$

Therefore,

$$\begin{aligned} D(s) [\Delta + F_{D1} F_V F_M] &= B_1 B_2 s^5 + [A_1 B_1 B_2 + (B_1 + B_2) - \\ &D_1 D_2 K_2 A_4 K_3 F_M] s^4 + \{A_2 B_1 B_2 + A_1 (B_1 + B_2) + 1 + \\ &[D_1 D_2 (K_1 A_3 - K_2 A_5) - K_2 A_4 (D_1 + D_2)] F_M K_3\} s^3 + \\ &\{A_2 (B_1 + B_2) + A_1 + [D_1 D_2 (K_1 - K_2 A_6) + (D_1 + D_2) \\ &(K_1 A_3 - K_2 A_5) - K_2 A_4] F_M K_3\} s^2 + \{A_2 + [K_1 A_3 - \\ &K_2 A_5 + (D_1 + D_2) (K_1 - K_2 A_6)] F_M K_3\} s + (K_1 - K_2 A_6) F_M K_3 \end{aligned}$$

$$\begin{aligned} D(s) F_{D1} F_C F_M &= -F_C F_M (K_2 A_4 B_1 B_2) s^5 + [B_1 B_2 (K_1 A_3 - K_2 A_5) \\ &- K_2 A_5) - K_2 A_4 (B_1 + B_2)] F_C F_M s^4 + [B_1 B_2 (K_1 - K_2 A_6) + \\ &(B_1 + B_2) (K_1 A_3 - K_2 A_5) - K_2 A_4] F_C F_M s^3 + [(B_1 + B_2) \\ &(K_1 - K_2 A_6) + (K_1 A_3 - K_2 A_5)] F_C F_M s^2 + (K_1 - K_2 A_6) F_C F_M s \end{aligned}$$

$$\begin{aligned} D(s) F_{D2} F_V F_M &= K_3 F_M D_1 D_2 K_5 s^4 + [K_5 (D_1 + D_2) + D_1 D_2 \\ &(K_4 E_1 + K_5 A_1)] K_3 F_M s^3 + [K_5 + (D_1 + D_2) (K_4 E_1 + K_5 A_1) \\ &+ D_1 D_2 (K_4 K_6 + A_2 K_5)] K_3 F_M s^2 + [(K_4 E_1 + K_5 A_1) + (D_1 + D_2) \\ &(K_4 K_6 + A_2 K_5)] K_3 F_M s + [K_4 K_6 + A_2 K_5] K_3 F_M \end{aligned}$$

Let $G_1 = B_1 B_2$, $G_2 = B_1 + B_2$, $G_3 = 1 + K_5 F_C F_M$,

$$G_4 = A_1 + (K_4 E_1 + K_5 A_1) F_C F_M, \quad G_5 = A_2 + (K_4 K_6 + K_5 A_2) F_C F_M$$

Then,

$$D(s) (\Delta + F_{D2} F_C F_M) = G_3 G_1 s^5 + (G_1 G_4 + G_2 G_3) s^4 + (G_1 G_5 + G_2 G_4 + G_3) s^3 + (G_2 G_5 + G_4) s^2 + G_5 s$$

$$D(s) F_{U11} = K_7 A_3 B_1 B_2 s^4 + \{K_7 [B_1 B_2 + A_3 (B_1 + B_2)]\} s^3 + K_7 (B_1 + B_2 + A_3) s^2 + K_7 s$$

$$D(s) F_{U21} = K_8 B_1 B_2 s^4 + \{(K_8 / E_1) [B_1 B_2 + E_1 (B_1 + B_2)]\} s^3 + (K_8 / E_1) (B_1 + B_2 + E_1) s^2 + (K_8 / E_1) s$$

$$D(s) F_{U12} = R_C B_1 B_2 s^5 + R_C (z_1 B_1 B_2 + B_1 + B_2) s^4 + R_C [w_0^2 z_2 B_1 B_2 + z_1 (B_1 + B_2) + 1] s^3 + R_C [w_0^2 z_2 (B_1 + B_2) + z_1] s^2 + R_C w_0^2 z_2 s$$

$$D(s) F_{U22} = K_9 A_3 B_1 B_2 s^4 + \{K_9 [B_1 B_2 + A_3 (B_1 + B_2)]\} s^3 + K_9 (B_1 + B_2 + A_3) s^2 + K_9 s$$

The system loop gain is given below:

$$T = \frac{1}{\Delta} F_M (F_V F_{D1} + F_C F_{D2})$$

Let

$$G_7 = -K_2 A_4 D_1 D_2$$

$$G_8 = [D_1 D_2 (K_1 A_3 - K_2 A_5) - K_2 A_4 (D_1 + D_2)]$$

$$G_9 = [(D_1 + D_2) (K_1 A_3 - K_2 A_5) + D_1 D_2 (K_1 - K_2 A_6) - K_2 A_4]$$

$$G_{10} = [(K_1 A_3 - K_2 A_5) + (D_1 + D_2) (K_1 - K_2 A_6)]$$

$$G_{11} = K_1 - K_2 A_6$$

$$G_{O1} = K_5 B_1 B_2$$

$$G_{O2} = K_5 (B_1 + B_2) + B_1 B_2 (K_4 E_1 + K_5 A_1)$$

$$G_{O3} = K_5 + (K_4 E_1 + K_5 A_1) (B_1 + B_2) + B_1 B_2 (K_4 K_6 + K_5 A_2)$$

$$G_{O4} = K_4 E_1 + K_5 A_1 + (B_1 + B_2) (K_4 K_6 + K_5 A_2)$$

$$G_{O5} = K_4 K_6 + K_5 A_2$$

Then, the numerator of T is:

$$F_M \{ (F_C G_{O1}) s^5 + [F_C G_{O2} + K_3 G_7] s^4 + [F_C G_{O3} + K_3 G_8] s^3 \\ + [F_C G_{O4} + K_3 G_9] s^2 + [F_C G_{O5} + K_3 G_{10}] s + G_{11} K_3 \}$$

and the denominator of T is:

$$B_1 B_2 s^5 + [A_1 B_1 B_2 + (B_1 + B_2)] s^4 + [A_2 B_1 B_2 + A_1 (B_1 + B_2) + 1] \\ s^3 + [A_2 (B_1 + B_2) + A_1] s^2 + A_2 s + 0$$

C.2 FORTRAN Program for Coefficients Calculation

```

C
C THIS PROGRAM IS DESIGNED TO ACCEPT THE CIRCUIT PARAMETERS AND THEN TO
C GENERATE THE ELEMENTS OF THE NODE MATRIX AND INPUT VECTOR FOR LISA 360
C PROGRAM.
C
C THE UNITS OF THOSE PARAMETERS ARE : RESISTANCE IN OHM, CAPACITANCE IN FARD,
C INDUCTANCE IN H, CURRENT IN AMP, VOLTAGE IN VOLT, FREQUENCIES IN HZ, PHASE
C IN DEGREE, AND TIME IN SEC.
C
C THIS PROGRAM IS CODED BY CROWN-SEN SHIEH, EE DEPT., YSU, OH 44555
C
C
C THE CIRCUIT PARAMETERS ARE VI, VO, RP, NP, NS, RS, RC, C, RL, TP, LP,
C LS, D, DPL(THESE COME FROM FLY-BACK POWER STAGE), C1, C2, C3, R1, R2, R3
C R4, R5, RSW AND N (THESE COME FROM ERROR PROCESSOR).
C
C
REAL VI, VO, RP, NP, NS, RS, RC, C, RL, TP, LP, LS, D, DPL
REAL C1, C2, C3, R1, R2, R3, R4, R5, RSW, N, LE, RE, WO2
REAL WO, Z1, Z2, ZATA, GQ, FC, FM, A1, A2, A3, A4, A5, A6
REAL B1, B2, D1, D2, E1, K1, K2, K3, K4, K5, K6, K7, K8, K9
REAL G1, G2, G3, G4, G5, G6, G7, G8, G9, G10, G11, GO1, GO2, GO3, GO4, GO5
READ(1, *) VI, VO, RP, NP, NS, RS, RC, C, RL, TP, LP, LS, D, DPL
READ(1, *) C1, C2, C3, R1, R2, R3, R4, R5, RSW, N
LE=LS/(DPL*DPL)
RE=RS/(DPL*DPL)
WO2=1/(LE*C)
WO=SQRT(WO2)
Z1=2*WO+(1/(RC*C))-(RC/LE)
Z2=(RE/RC)+(D/DPL)
ZATA=(WO/2)*((LE/RL)+(RE+(RC/DPL))*C)
GQ=1/((1+(R3/R1)+(R3/R2))*R1)
FC=RSW/N
FM=(2*N*LP*VO)/(VI*RSW*TP)
A1=2*ZATA*WO
A2=(WO)**2
A3=RC*C
A4=RC/(WO**2)
A5=LE+((2*RC*ZATA)/WO)
A6=RE+(RC/DPL)
B1=(R4*C1*C3)/(C1+C3)
B2=R5*C2
D1=R4*C1
D2=C2*((R5*GQ+1)/GQ)
E1=RL*C
K1=(WO**2)/(D*DPL)
K2=(WO**2)/(RL*DPL)
K3=GQ/(C1+C3)
K4=NS/(NP*RL*C*LS)
K5=NS/(NP*DPL*RL)
K6=1+D
K7=(NS*(WO**2)*D)/(DPL*NP)
K8=(D**2)/LP
K9=-(D*DPL*NP)/(LP*NS*C)
C
C
C COMPUTE EACH ENTRY OF THE NODE MATRIX IN SEQUENCE AS: ENM11, ENM12, ENM21
C AND ENM22.
C
C ENM11 = (ENM11A)*S**5 + (ENM11B)*S**4 + (ENM11C)*S**3 + (ENM11D)*S**2 +

```

```

C          (ENM11E)*S**1 + (ENM11F)*S**0
C
ENM11A=B1*B2
ENM11B=(A1*B1*B2)+B1+B2-(D1*D2*K2*A4*K3*FM)
ENM11X=(A2*B1*B2)+(A1*(B1+B2))+1
ENM11C=ENM11X+((D1*D2*(K1*A3-K2*A5)-K2*A4*(D1+D2))*FM*K3)
ENM11Y=A2*(B1+B2)+A1
ENM11Z=D1*D2*(K1-K2*A6)
ENM11D=ENM11Y+((ENM11Z+(D1+D2)*(K1*A3-K2*A5)-K2*A4)*FM*K3)
ENM11E=A2+((K1*A3-K2*A5+(D1+D2)*(K1-K2*A6))*FM*K3)
ENM11F=(K1-K2*A6)*FM*K3
C
C
C ENM12 = (ENM12A)*S**5 + (ENM12B)*S**4 + (ENM12C)*S**3 + (ENM12D)*S**2 +
C          (ENM12E)*S**1 + (ENM12F)*S**0
C
ENM12A=FC*FM*(-K2*A4*B1*B2)
ENM12B=(B1*B2*(K1*A3-K2*A5)-K2*A4*(B1+B2))*FC*FM
ENM12C=(B1*B2*(K1-K2*A6)+(B1+B2)*(K1*A3-K2*A5)-K2*A4)*FC*FM
ENM12D=((B1+B2)*(K1-K2*A6)+(K1*A3-K2*A5))*FC*FM
ENM12E=(K1-K2*A6)*FC*FM
ENM12F=0.0
C
C
C ENM21 = (ENM21A)*S**4 + (ENM21B)*S**3 + (ENM21C)*S**2 + (ENM21D)*S**1 +
C          (ENM21E)*S**0
C
ENM21A=K3*FM*D1*D2*K5
ENM21B=(K5*(D1+D2)+D1*D2*(K4*E1+K5*A1))*K3*FM
ENM21C=(K5+(D1+D2)*(K4*E1+K5*A1)+D1*D2*(K4*K6+A2*K5))*K3*FM
ENM21D=((K4*E1+K5*A1)+(D1+D2)*(K4*K6+A2*K5))*K3*FM
ENM21E=(K4*K6+A2*K5)*K3*FM
C
C ENM22 = (ENM22A)*S**5 + (ENM22B)*S**4 + (ENM22C)*S**3 + (ENM22D)*S**2 +
C          (ENM22E)*S**1 + (ENM22F)*S**0
C
G1=B1*B2
G2=B1+B2
G3=1+(K5*FC*FM)
G4=A1+((K4*E1+K5*A1)*FC*FM)
G5=A2+((K4*K6+K5*A2)*FC*FM)
ENM22A=G1*G3
ENM22B=G1*G4+G2*G3
ENM22C=G1*G5+G2*G4+G3
ENM22D=G2*G5+G4
ENM22E=G5
ENM22F=0.0
WRITE(2,10)
10  FORMAT(3X,'THE COEFFICIENTS OF ENM11 ARE : '//)
WRITE(2,*) ENM11A, ENM11B, ENM11C, ENM11D, ENM11E, ENM11F
WRITE(2,20)
20  FORMAT(3X,'THE COEFFICIENTS OF THE ENM12 ARE : '//)
WRITE(2,*) ENM12A, ENM12B, ENM12C, ENM12D, ENM12E, ENM12F
WRITE(2,30)
30  FORMAT(3X,'THE COEFFICIENTS OF THE ENM21 ARE : '//)
WRITE(2,*) ENM21A, ENM21B, ENM21C, ENM21D, ENM21E
WRITE(2,40)
40  FORMAT(3X,'THE COEFFICIENTS OF THE ENM22 ARE : '//)
WRITE(2,*) ENM22A, ENM22B, ENM22C, ENM22D, ENM22E, ENM22F
C

```

```

C
C COMPUTE THE INPUT VECTOR OF VI, EU11 AND EU21
C
C EU11 = (EU11A)*S**4 + (EU11B)*S**3 + (EU11C)*S**2 + (EU11D)*S**1 + (EU11E)
C
      EU11A=K7*A3*B1*B2
      EU11B=K7*(B1*B2+A3*(B1+B2))
      EU11C=K7*(B1+B2+A3)
      EU11D=K7
      EU11E=0.0
C
C
C
C EU21 = (EU21A)*S**4 + (EU21B)*S**3 + (EU21C)*S**2 + (EU21D)*S**1 + (EU21E)
C
      EU21A=K8*B1*B2
      EU21B=(K8/E1)*(B1*B2+E1*(B1+B2))
      EU21C=(K8/E1)*(B1+B2+E1)
      EU21D=K8/E1
      EU21E=0.0
C
C
C
C COMPUTE THE INPUT VECTOR OF IO, EU12 AND EU22
C
C EU12 = (EU12A)*S**5 + (EU12B)*S**4 + (EU12C)*S**3 + (EU12D)*S**2 +
C      (EU12E)*S**1 + (EU12F)*S**0
C
C
      EU12A=RC*B1*B2
      EU12B=RC*(Z1*B1*B2+B1+B2)
      EU12C=RC*(WO2*Z2*B1*B2+Z1*(B1+B2)+1)
      EU12D=RC*(WO2*Z2*(B1+B2)+Z1)
      EU12E=RC*WO2*Z2
      EU12F=0.0
C
C
C
C EU22 = (EU22A)*S**4 + (EU22B)*S**3 + (EU22C)*S**2 + (EU22D)*S**1 + (EU22E)
C
      EU22A=K9*A3*B1*B2
      EU22B=K9*(B1*B2+A3*(B1+B2))
      EU22C=K9*(B1+B2+A3)
      EU22D=K9
      EU22E=0.0
      WRITE(2,50)
50  FORMAT(3X,'THE INPUT VECTOR OF VI ARE EU11 AND EU21. THE COEFFICIENTS
C OF THE EU11 ARE: '//)
      WRITE(2,*) EU11A,EU11B,EU11C,EU11D,EU11E
      WRITE(2,60)
60  FORMAT(3X,'THE COEFFICIENTS OF THE EU21 ARE: '//)
      WRITE(2,*) EU21A,EU21B,EU21C,EU21D,EU21E
      WRITE(2,70)
70  FORMAT(3X,'THE INPUT VECTORS OF IO ARE EU12 AND EU22. THE COEFFICIENTS
C OF THE EU12 ARE: '//)
      WRITE(2,*) EU12A,EU12B,EU12C,EU12D,EU12E,EU12F
      WRITE(2,80)
80  FORMAT(3X,'THE COEFFICIENTS OF THE EU22 ARE: '//)
      WRITE(2,*) EU22A,EU22B,EU22C,EU22D,EU22E
C
C
C

```

```

C
C
C COMPUTE THE COEFFICIENTS OF SYSTEM LOOP GAIN: T=(1/DELTA)*FM*(FV*FD1+FC*FD2)
C
C THE COEFFICIENTS OF THE NUMERATOR OF THE SYSTEM LOOP GAIN IS ETN.
C THE COEFFICIENT FORMAT: SCALE FACTOR, DEGREE, COEFFICIENTS IN DESCENDING
C ORDER.
C
C
G7=-K2*A4*D1*D2
G8=(D1*D2*(K1*A3-K2*A5)-K2*A4*(D1+D2))
G9=((D1+D2)*(K1*A3-K2*A5)+D1*D2*(K1-K2*A6)-K2*A4)
G10=((K1*A3-K2*A5)+(D1+D2)*(K1-K2*A6))
G11=K1-K2*A6
GO1=K5*B1*B2
GO2=K5*(B1+B2)+B1*B2*(K4*E1+K5*A1)
GO3=K5+(K4*E1+K5*A1)*(B1+B2)+B1*B2*(K4*K6+K5*A2)
GO4=(K4*E1+K5*A1)+(B1+B2)*(K4*K6+K5*A2)
GO5=K4*K6+K5*A2
ETNA=FM
ETNB=5.0
ETNC=FC*GO1
ETND=FC*GO2+K3*G7
ETNE=FC*GO3+K3*G8
ETNF=FC*GO4+K3*G9
ETNG=FC*GO5+K3*G10
ETNH=G11*K3
C
C THE COEFFICIENTS OF THE DENOMINATOR OF THE SYSTEM LOOP GAIN ARE ETD.
C
C THE COEFFICIENTS FORMAT IS THE SAME AS THAT OF NUMERATOR.
C
ETDA=1.0
ETDB=5.0
ETDC=B1*B2
ETDD=A1*B1*B2+(B1+B2)
ETDE=A2*B1*B2+A1*(B1+B2)+1
ETDF=A2*(B1+B2)+A1
ETDG=A2
ETDH=0.0
WRITE(2,90)
90 FORMAT(3X,'THE COEFFICIENTS OF THE NUMERATOR OF T ARE: (IN DESCENDING ORDER)')
WRITE(2,*)ETNA,ETNB,ETNC,ETND,ETNE,ETNF,ETNG,ETNH
WRITE(2,100)
100 FORMAT(3X,'THE COEFFICIENTS OF THE DENOMINATOR OF T ARE: (IN DESCENDING ORDER)')
WRITE(2,*)ETDA,ETDB,ETDC,ETDD,ETDE,ETDF,ETDG,ETDH
END

```

C.3 LISA Simulation Program

```
TITLE, COMPUTER SIMULATION FOR MULTI-LOOP CONTROL FLY-BACK SMPS
READ, MATRIX
  1, 1, 4, 0. 263472975E-05, -0. 191525459, 34090. 0234, ...
    0. 212994227E+10, 0. 157952246E+13
  1, 2, 4, -0. 199417718E-05, -0. 705040455, 23137. 0234, ...
    0. 131362534E+10, 0. 0
  2, 1, 3, 3. 02852154, 195575. 437, 404625920. 0, ...
    0. 195606807E+12
  2, 2, 4, 0. 766206995E-05, 3. 23873711, 125975. 062, ...
    183992208. 0, 0. 0
  1, 3, 4, 0. 461077647E-07, 0. 192948468E-01, 684. 457275, ...
    1225560. 0, 0. 0
  2, 3, 3, -0. 892036041E-04, -36. 5681763, -1029083. 56, ...
    0. 0
DEFINE, VO=V(1)
DEFINE, DETYS=X(0)
DEFINE, NS=X(1)
COMPUTE, POLY, VO, DETYS, NS
COMPUTE, BODE, VO
DATA, FREQUENCY=1, 10. 0E6, 150, HZ, LOG
PLOT
LABEL, OUTPUT IMPEDANCE = VO/IO
CHANGE, MATRIX, ADD
  1, 3, 3, 0. 815099629E-04, 33. 4142456, 940327. 000, ...
    0. 0
  2, 3, 3, 0. 224883028E-03, 85. 5128479, 60534. 2969, ...
    0. 0
COMPUTE, POLY, VO, DETYS, NS
COMPUTE, BODE, VO
DATA, FREQUENCY=1, 10. 0E6, 150, HZ, LOG
PLOT
LABEL, AUDIOSUSCEPTIBILITY = VO/VI
READ, TS
  COEFF, 7. 78507328, 4, 0. 645766931E-06, ...
    0. 132001162, 19591. 8281, 291751168. 0, 0. 202891264E+12
  COEFF, 1. 0, 4, 0. 263472975E-05, ...
    1. 00978661, 3770. 66235, 21314080. 0, 0. 0
COMPUTE, POLY, TS
COMPUTE, BODE, TS
DATA, FREQUENCY=1, 10. 0E6, 150, HZ, LOG
PLOT
LABEL, THE SYSTEM LOOP GAIN = TS
EXIT
```

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